

IEEE Std P1532

A New Standard for 1149.1-based In System Configuration

Neil G. Jacobson, Chair



Historical Perspective

- ISP (In System Programming) first developed in 1993 using proprietary bus & protocol
- Simultaneous demand for boundary-scan and ISP leads to general adoption of JTAG bus & protocol
- Similar but different implementations result in custom tool environment



Historical Perspective

- Inaugural meeting April, 1996
 - Attended by semiconductor manufacturers, tool developers, ATE manufacturers and system designers
- E-mail reflector established
- Meetings held quarterly
- Draft developed for review



Mission

To define, document and promote the use of a standardized process and methodology for implementing programming capabilities...utilizing (and compatible with) the 1149.1 communication protocol.



Benefits

- Serve as development model for new devices
- Build on existing, well-supported and understood standard (1149.1, BSDL)
- Standardize tool, development system, test and manufacturing interfaces to provide “instant” device support
- Facilitate innovation and the development of new application areas
- Enable “concurrent programming” capabilities



P1532 Application Space

- It is the intention of P1532 to be applicable, usable and practical for:

- FPGA's
- CPLD's
- PROM's

I.E., ANY PROGRAMMABLE DEVICE

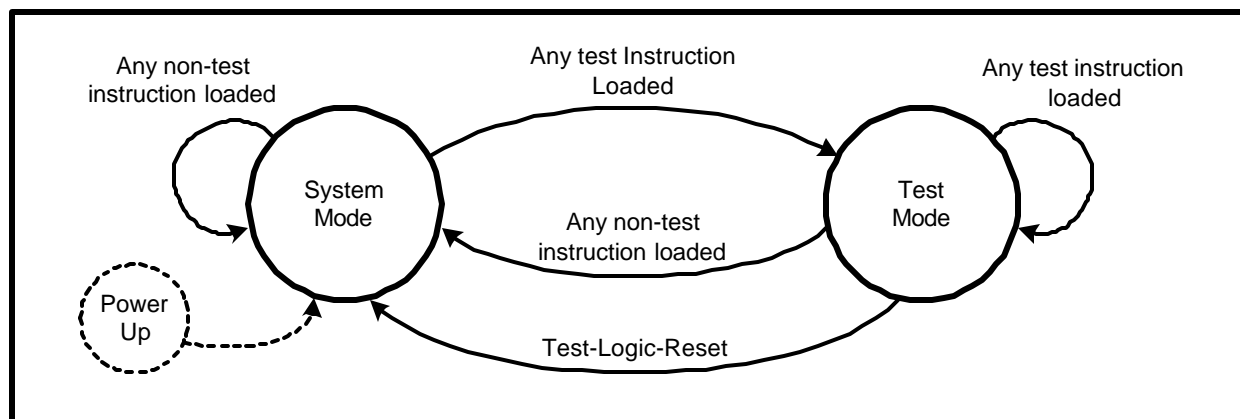


Progress so far...

- Description of silicon implementation requirements completed and proceeding to ballot.
- Description of BSDL extensions continuing to be filed as a supplement to the standard.

1149.1 System Modal States

- System Mode
- Test Mode

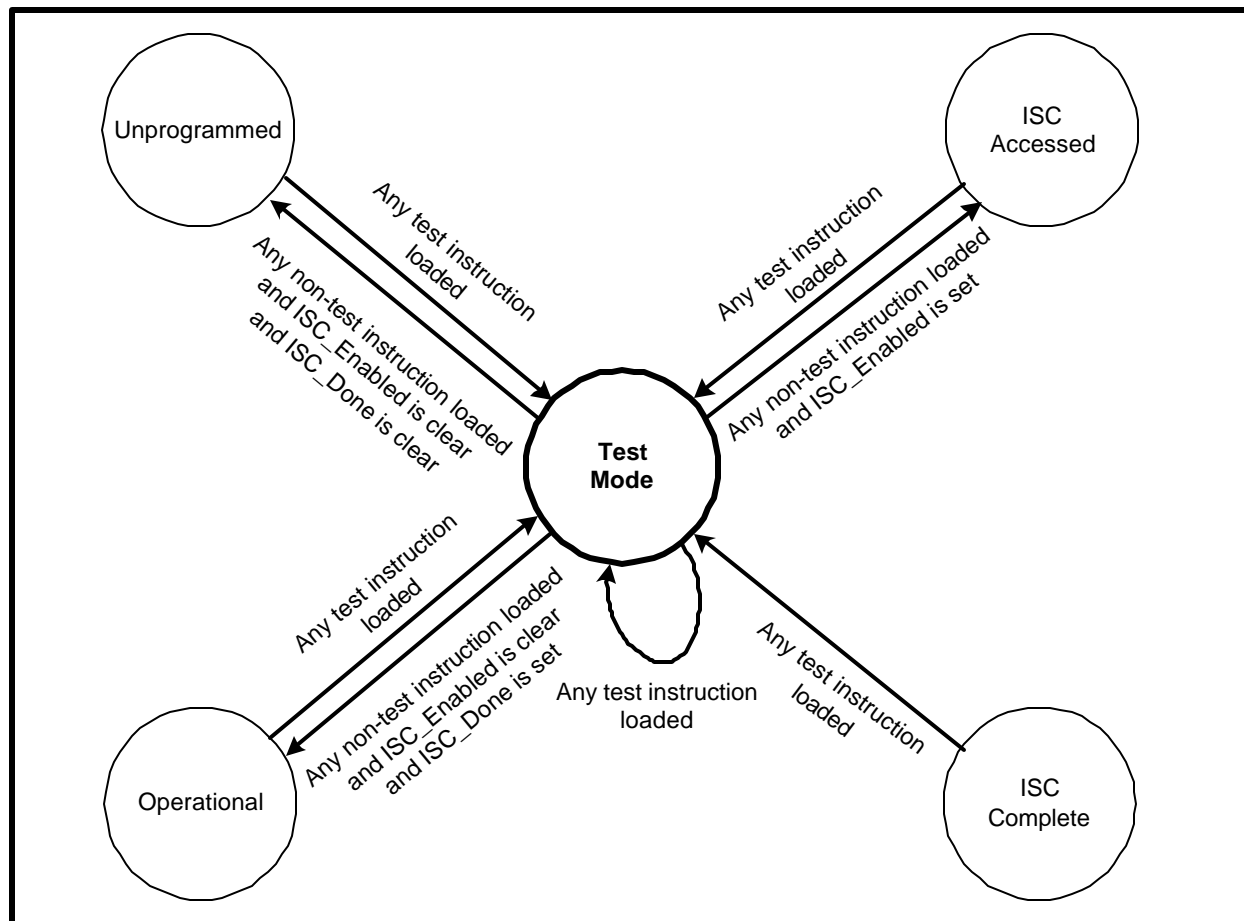




P1532 System Modal States

- Unprogrammed Mode
- ISC Accessed Mode
- ISC Complete Mode
- Operational Mode

P1532 System Modes





P1532 Instruction Set

- Support Basic ISC Functionality
 - Concurrent Operations
 - Well-defined System Behaviour
 - Mandatory Instructions
 - ISC_ENABLE
 - ISC_PROGRAM
 - ISC_DISABLE
 - ISC_NOOP

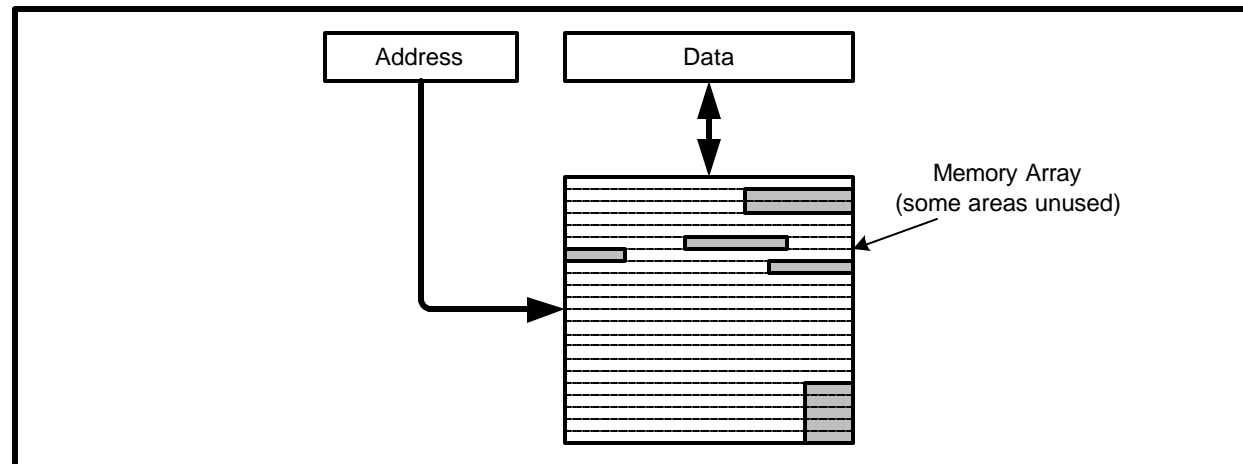


P1532 Instruction Set

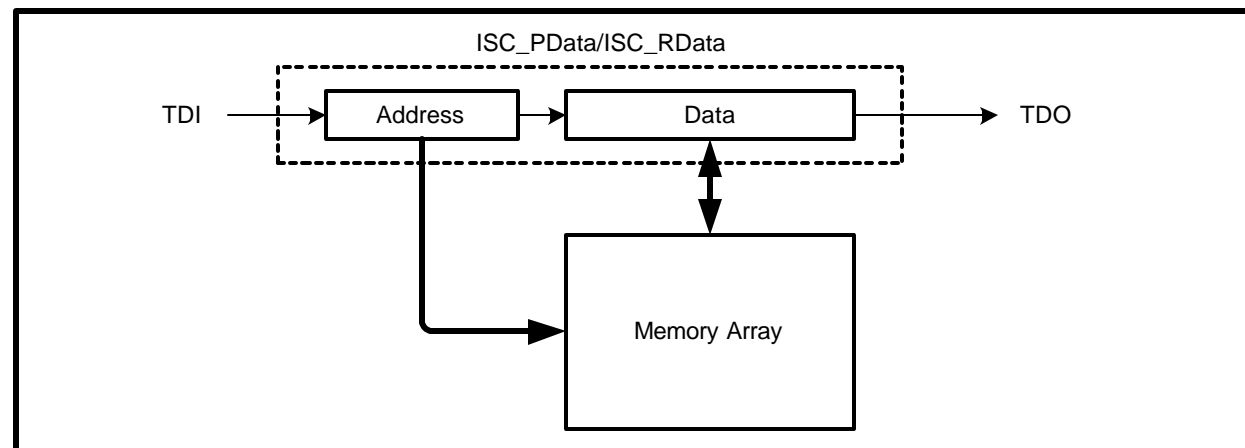
- Support Additional Access Mechanisms
 - ISC_DISCHARGE
 - ISC_SETUP
 - ISC_PROGRAM_DONE
 - ISC_ERASE_DONE
 - ISC_DATA_SHIFT
 - ISC_ADDRESS_SHIFT
 - ISC_INCREMENT

P1532 Memory Model

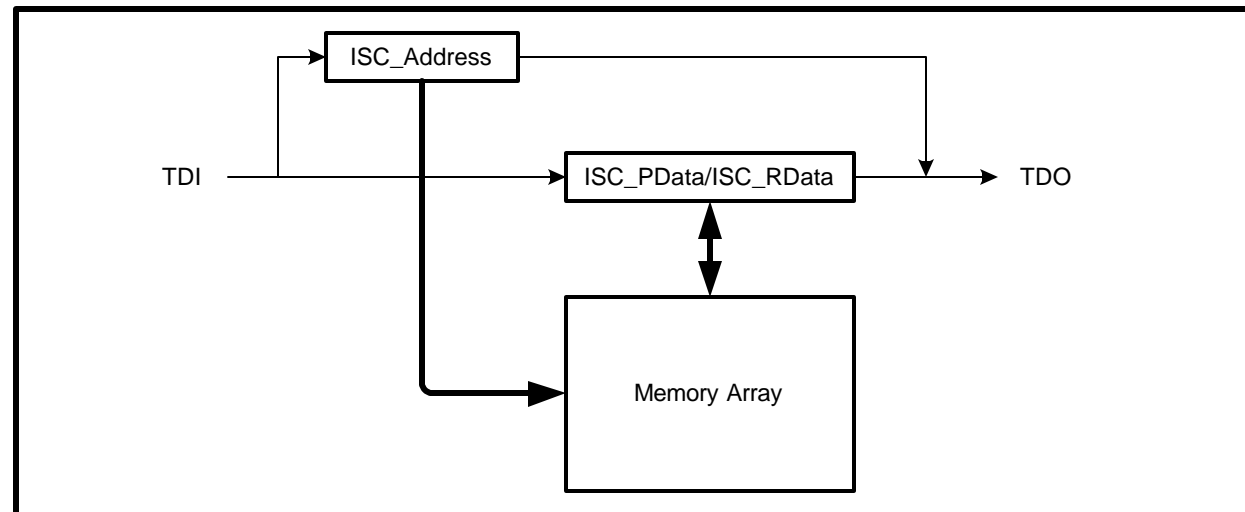
Basic Structure



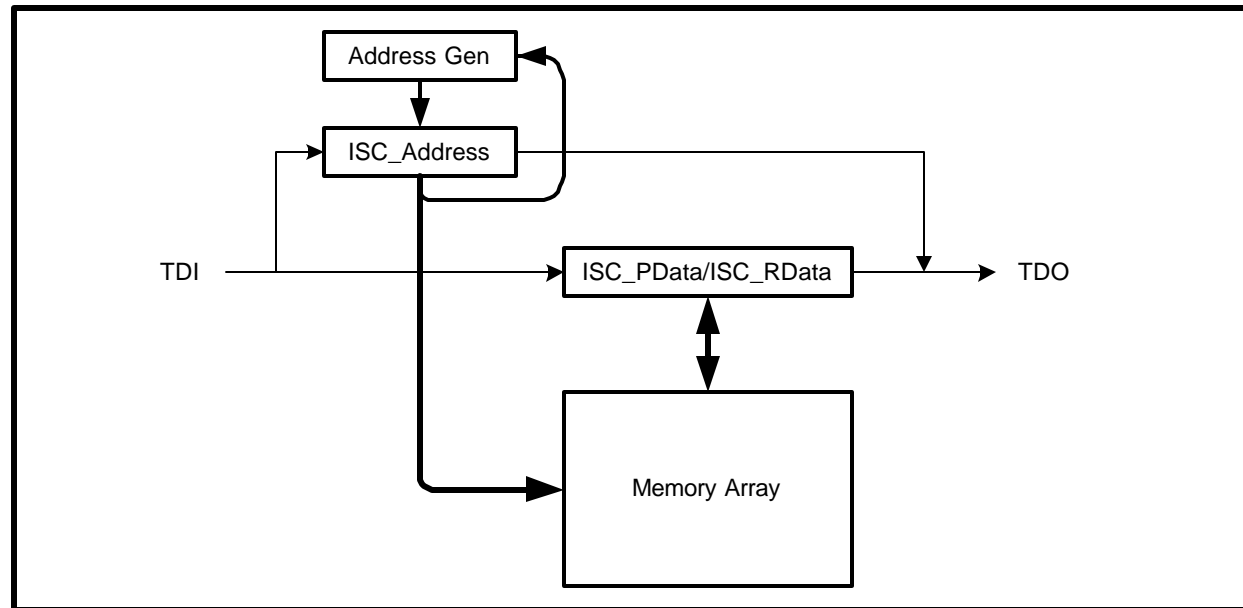
P1532 Memory Model Variation 1



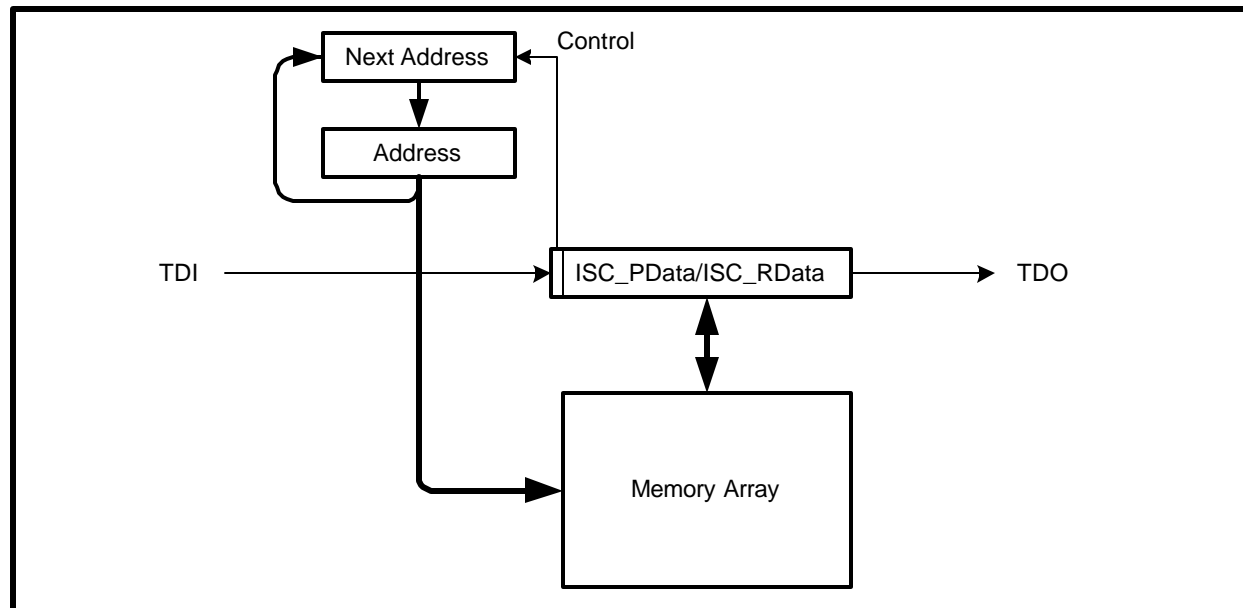
P1532 Memory Model Variation 2



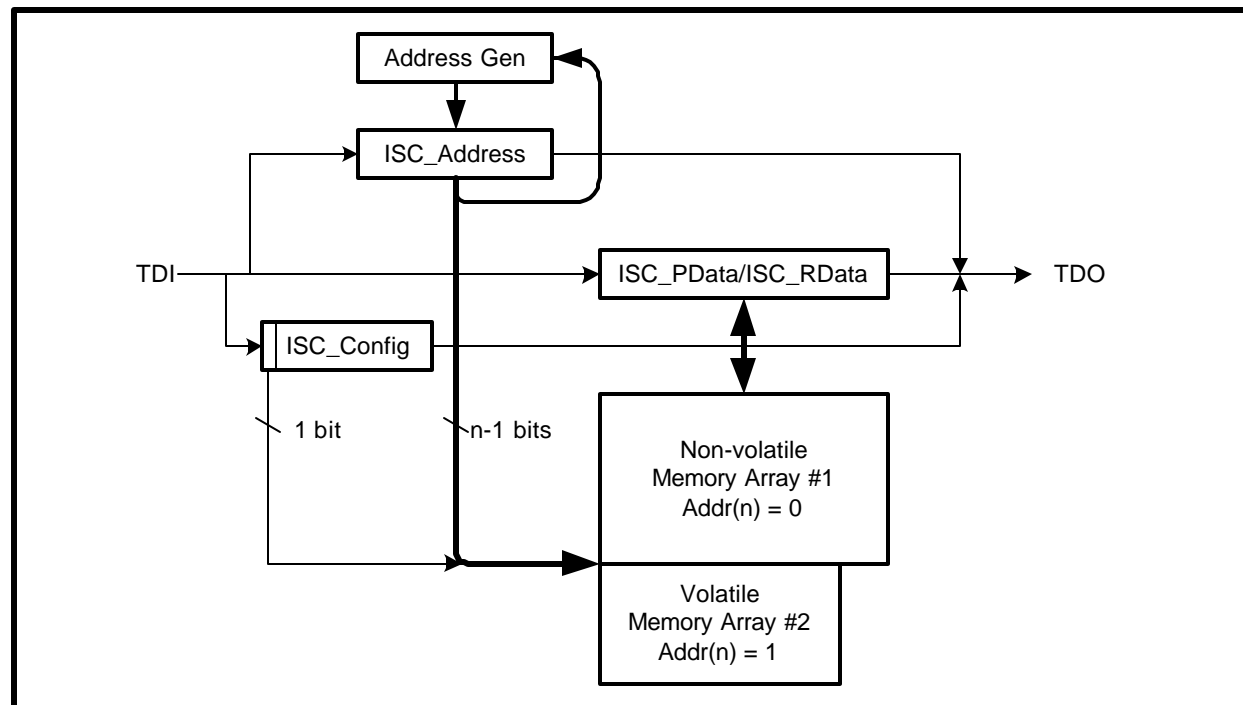
P1532 Memory Model Variation 3



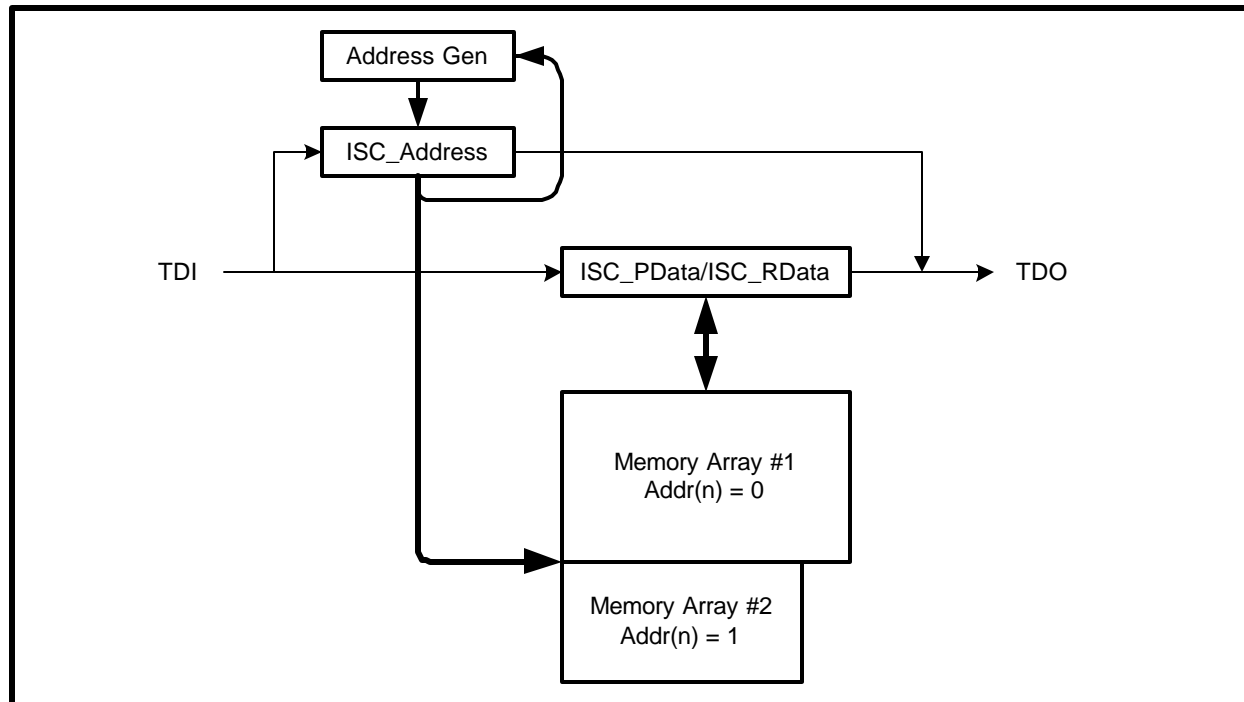
P1532 Memory Model Variation 4



P1532 Memory Model Variation 5



P1532 Memory Model Variation 6

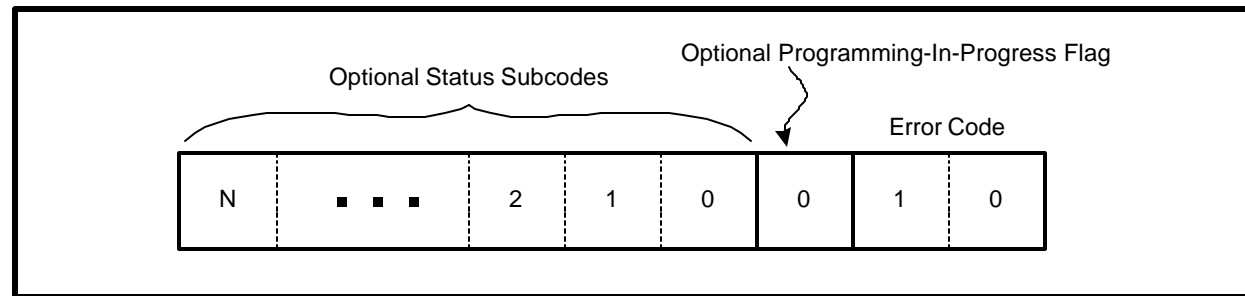




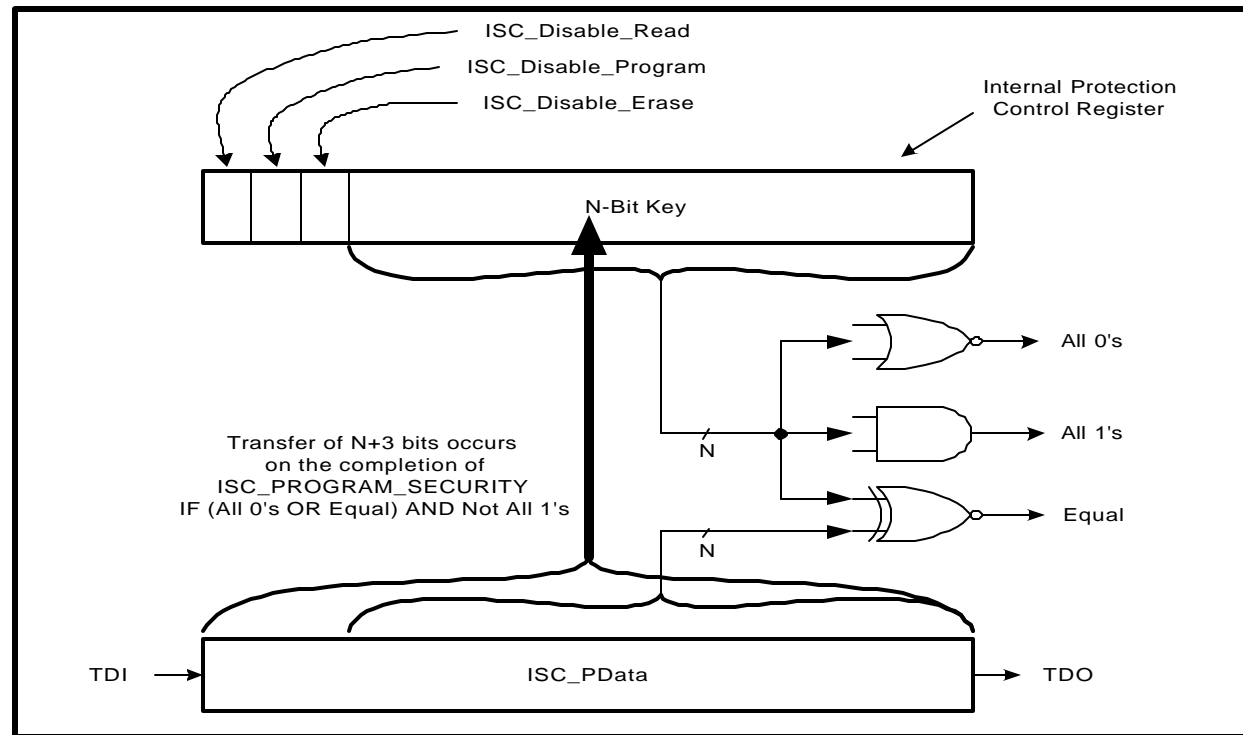
P1532 Instruction Set

- Support Advanced ISC Functionality
 - ISC_ERASE
 - ISC_READ
 - ISC_READ_INFO
 - ISC_PROGRAM_SECURITY
 - ISC_PROGRAM_START
 - ISC_PROGRAM_STOP

P1532 Optional Status Mechanism



P1532 Optional Security Mechanism





P1532 BSDL

- Supported through BSDL EXTENSION
- Description sufficient to indicate:
 - Device ISC Capabilities
 - Allowable Mode Transitions
 - Operational Flows



Joining the Ballot Group

- You must be a member of the IEEE-SA.
- You must be committed to reading, understanding and returning the ballot document.
- Submit your contact information to me - now!



Joining the Working Group

- Meetings are scheduled at least 4 weeks in advance
- They are 2 days in length and generally in the San Jose area
- To become a voting member, you must:
 - Attend two consecutive meetings.
 - Express an interest in joining.



Information Sources

■ Executive Committee

- Neil Jacobson, Chair
 - neil.jacobson@xilinx.com
- Dave Bonnett, Vice Chair
 - dbonnett@asset-intertech.com
- Ted Eaton, Secretary
 - ted_eaton@sun.com
- Ken Parker, Technical Editor
 - parker@lvld.hp.com



Information Sources

- Invitation to Ballot Group
 - Contact Neil Jacobson
 - neil.jacobson@xilinx.com
- E-mail Reflector
 - stds-1532-wg@ieee.org
 - Contact Neil Jacobson to join
- Web Page
 - <http://grouper.ieee.org/groups/1532/index.html>