

**P1581: New Hope of Success?  
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Script to accompany slides

Slide 1: Outline

Slide 2: A review of the traditional connectivity test problem between random logic.

Slide 3: A review of the 1149.1 solution of adding a test layer of logic to solve the problem.

Slide 4: A review of the problem confronted by P1581.

Slide 5: A review of the initial P1581 solution.

Slide 6: A review of the alternative P1581 solution apparently in the public domain..

Slide 7: See explanation of Slide 15.

Slide 8: Illustrates how TTM may be included in the test layer. Note mode line unnecessary.

Slide 9: Lists benefits of TTM, as noted above.

Slide 10: A review of the three operational states of a typical memory device: (1) unpowered, (2) after power is applied and outputs (if enabled) are unknown (X) and (3) after a write has been performed when the outputs of at least one addressed location are known (non-X).

Slide 11: Illustrates the three operational states of a similar memory device, to which P1581 and TTM have been added. The second state is different in how output values are determined, when driven. Instead of reflecting the unknown contents of an unwritten memory location, the output values are determined by the P1581 test logic. Note that the test operation concludes as a write is performed.

Slide 12: Illustrates the relationship of the test and functional layers. Note that the functional layer always responds to input stimulus, even when the test layer is driving the outputs. Note also that the functional layer controls the outputs as soon as a write operation is sensed. In this case, the term "write detected" means that any write configuration has been detected at the inputs, not that a write has actually occurred. That is, the switchover takes place in advance of completing a write operation. For simplicity, the inability to switch back to test mode, although shown in slides 11 and 13, has not been illustrated here. The test mode occurs only after power up and before the functional mode has been selected.

Slide 13: Illustrates that a memory device having P1581 with TTM works just as well in a board environment where the designer ignores the test capability of the device, as it does in a board environment where the designer plans on 1149.1/P1581 testing. In the former situation, the designer need be concerned neither that the test mode has been activated after power up nor that stimulus to deactivate test mode be provided. The test mode is active only when the memory device would have otherwise been in an unknown state and it is automatically deactivated before a known state might have been entered. The test mode, therefore, does not interfere with device functionality.

Slide 14: Summarizes the benefits of using TTM for P1581.

Slide 15: Like slide 7, included only for effect in the presentation, which was one of a series of "elevator talks" at the workshop. The two slides are included here only so the workshop slide set would match the set posted, or soon to be posted, on Ben Bennett's [www.dft.co.uk/BTW2004](http://www.dft.co.uk/BTW2004).

Some operational details are not shown in the slides. For example, in the case of a board which is to use 1149.1/P1581 testing (but not in the case of boards which are not), it is necessary to ensure a write configuration isn't presented at the inputs of the memory device prematurely. This can be done with careful application of boundary scan patterns to surrounding devices beginning immediately after power up or with other circuitry. Also, a delay must be built into the TTM "write detector" to avoid switching to functional mode before the surrounding devices have initialized. There are other details missing from this brief explanation, the objective being to present the essence of the technique.