Emulation Circuitry Adds P1581 to an Off-the-Shelf SRAM

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P1581 Working Group may or may not agree with content.

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Outline

• Developments Since BTW 2006
• P1581 Standard / Optional Operations
• Testmode Control Without Added Pins
• Comparison of P1581 & 1149.1 for Memory Devices
• P1581 Emulation Goals & General Concept
• Emulation Circuitry Details
• Conclusion: Emulation Allows First Silicon Success
Developments Since BTW 2006

• Device ID Added
  – Standard 1149.1 Format (Extensions Possible)
  – P1581 Now Includes Key Features of 1149.1

• Emulation Method Devised
  – Means to Avoid First (Etc.) Silicon Errors
  – Significant Advantage Over 1149.1

• Emulation Demo Board
  – Proof of Concept
  – Supports Device / Tool Development
  – Design Available Without Charge
P1581 Continuity Test Concept
Continuity Test Gating - IAX

(12 Address, 4 Data Bits)
Device Identification Option

Gates (Continuity) — Device ID Reg. — Decoder

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Non-Functional Stimulus Mode Control

Test Mode Control from Existing PCB BScan Circuitry
(No additional DFT)
P1581 / 1149.1 Comparison

Memory Device w/ P1581
- Functional Circuitry
  - (Memory Cells, Etc.)
  - P1581 Test Circuitry
    - Continuity
    - Options:
      - Device ID
      - BIST, Etc.

Memory Device w/ 1149.1
- Functional Circuitry
  - (Memory Cells, Etc.)
  - 1149.1 Test Circuitry
    - Continuity
    - Options:
      - Device ID
      - BIST, Etc.
P1581 Features Summary

• Equivalent to 1149.1:
  – Continuity Test
  – Device ID Option
  – BIST Option
  – Other Public / Private Options

• Improvements over 1149.1
  – No Testpins Required
  – Same Device Usable in Legacy (non-P1581) and P1581 Board Applications

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P1581 Emulation Goals

• Allow Off-the-Shelf Memory Devices to be Adapted for P1581 Design / Development Operations

• Run At or Near Speed for Board Level Substitution

• Support Test Jig Operation
  – Device Design Debug
  – Test & Test Tool Development

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Emulation for Demo

- Cypress CY62157EV30 TSOP I
- Chosen for Complexity
- Dual Configuration: 1Meg x 8 / 512K x 16
- Emulator Must Work for All Board Applications
- BYTE* Tied H / L for 16 / 8 Bit Operation
- Data Pin Doubles as Address Pin (Potential Issue Because P1581 Uses Address Pins as Inputs, Data Pins as Outputs)
- Note: TSOP I Version Different Than Others

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Emulation Environment
P1581 Emulation Concept
Bank Emulation Example
Emulation - Simple Memory

P1581 EMULATION LOGIC DESIGN USING NPS
TEST MODE CONTROL FOR 4M X 4 STATIC RAM

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Summary

• Enhancements Since BTW 2006
• P1581 Basic Operation
• P1581 Options (Device ID, BIST, Public, Private)
• NFS Mode Control (No Dedicated Testpins)
• P1581 Vs. 1149.1 for Memory Devices
• Emulation Goals & General Concept
• Emulation Circuitry Details
Conclusion

- P1581 Includes Key 1149.1 Features
- Emulation Facilitates First Silicon Success
- P1581 Preferable to 1149.1 for Some Memory Devices

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Further Information

- IEEE P1581 Working Group Website: http://grouper.ieee.org/groups/1581/

- Sit In on WG Telephone Conference

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