IEEE P1581
Enhancements/Status

Bob Russell
(r.russell@ieee.org)

P1581 Working Group may or may not agree with content.

RJR BTW 17 SEP 2008
Outline

• P1581 Refresher
• Emulation Results & Status
• Simulation Results
• Future Plans

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1149.1 Problem

Memory Device w/ 1149.1

- Functional Circuitry
- (Memory Cells, Etc.)
- 1149.1 Test Circuitry
  - Continuity
  - Options:
    - Device ID
    - BIST, Etc.

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Ideal Solution

- Functional Circuitry
  - (Memory Cells, Etc.)

- Test Circuitry
  - Continuity
  - Options:
    - Device ID
    - BIST, Etc.

DATA & CONTROL

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P1581 Continuity Test Concept

Device(s) w/ 1149.1

Memory Device w/ P1581

From TDI

Address

Control

Data

Functional Logic

To TDO

Functional (Cells)

Test Gates (P1581)

Mode Control

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Continuity Test Gating - IAX

(12 Address, 4 Data Bits)
# Test Pattern Partitioning

<table>
<thead>
<tr>
<th>12 Address Bits</th>
<th>Unpartitioned</th>
</tr>
</thead>
<tbody>
<tr>
<td>XXXXXXXXXXXXXX</td>
<td>4096 Continuity</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Partitioned</th>
</tr>
</thead>
<tbody>
<tr>
<td>All 0's/1's</td>
</tr>
<tr>
<td>One 0/1</td>
</tr>
<tr>
<td>Two 0's/1's</td>
</tr>
<tr>
<td>1110000XXXXX</td>
</tr>
<tr>
<td>101010XXXXXX</td>
</tr>
<tr>
<td>010101XXXXXX</td>
</tr>
</tbody>
</table>
Device Identification Option
BIST & Device ID Options
# Test Mode Entry / Exit Options

## Test Mode Entry & Exit Methods

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Method</th>
<th>Description of Test Mode Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>NFS</td>
<td>Non-Functional Stimulus</td>
<td>Device inputs driven by stimulus not possible in functional operation, but easily accomplished during board test operations (e.g., boundary scan, ICT, board level BIST).</td>
</tr>
<tr>
<td>CKF</td>
<td>Clock Frequency</td>
<td>Device clock input frequency altered (e.g., static) by board level control of the clock driver device.</td>
</tr>
<tr>
<td>CDE</td>
<td>Code Selection</td>
<td>Device codes not required for functional operation (e.g., read, write) are assigned to test mode control.</td>
</tr>
<tr>
<td>ANL</td>
<td>Analog Level</td>
<td>One or more device inputs are driven to a non-logical level for a duration not possible during functional operation.</td>
</tr>
<tr>
<td>TPN</td>
<td>Testpin</td>
<td>A dedicated device input is used for test mode control.</td>
</tr>
</tbody>
</table>

## Initial Dependence on Powerup Timing

<table>
<thead>
<tr>
<th>Acronym</th>
<th>Method</th>
<th>Description of Test Mode Control</th>
</tr>
</thead>
<tbody>
<tr>
<td>PST</td>
<td>Powerup Selection</td>
<td>A short delay after powerup certain device inputs are monitored for presence of states that would be avoided through customary board design (e.g., write and chip select both active). Various exit means.</td>
</tr>
<tr>
<td>PDT</td>
<td>Powerup Default</td>
<td>Test mode occurs at powerup. Exit occurs at beginning of first write unless other exit means chosen.</td>
</tr>
</tbody>
</table>

## Summary of Test Mode Entry/Exit Methods.
Non-Functional Stimulus Mode Control

Test Mode Control from Existing PCB BScan Circuitry
(No additional DFT)

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P1581 Vs. 1149.1

Comparison of Features - P1581 vs. 1149.1
Legacy Compatibility
(Transparency)

With P1581

Functional Circuitry
(Memory Cells, Etc.)

P1581 Test Circuitry
- Continuity
- Options:
  - Device ID
  - BIST, Etc.

Without P1581

Functional Circuitry
(Memory Cells, Etc.)

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Emulation Benefits

- Proof of Concept
- “First Silicon Success” for New / Revised Memory Devices
- Test Tool Development
  - BScan Testers
  - ICT
  - Device Testers
- Test Code Development
Emulation Benefits (cont.)

Memory Device

TCK  TMS  TDI  TDO

TCK  LOGIC ZERO  TMS  TDI  TDO

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Emulation Status

• SRAM – Done / Demo @ BTW

• FLASH – Done / Demo @ BTW

• DRAM – In Design (Goepel Hardware Ready)

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P1581 Emulation Concept
FLASH Emulation
Simulation Results - SRAM

- Alcatel-Lucent Test Bench Simulator
- Michele Portolan / Brad Van Treuren
- Used Standard Model of Emulated SRAM
- No Problems Found
- Proved No Data Lost During Board Functional Write Operation to a P1581 Memory Device Inadvertently Left in Test Mode. (Test Mode Terminates.)
- March 2008
Working Group Future Plans

- Memory Device Manufacturer Involvement
- D I T T O ! ! ! ! ! ! ! !
- DRAM Emulation Completion for ITC Demo
- Simulate P1581 DRAM Device
- Develop Description Language
- Recruit an Editor
- Complete Draft and Ballot

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Conclusion

• P1581 Includes Key 1149.1 Features

• Emulation Facilitates First Silicon Success

• P1581 Preferable to 1149.1 for Some Memory Devices
Further Information

- IEEE P1581 Working Group Website: http://grouper.ieee.org/groups/1581/
- Sit In on WG Phone Conference – Oct. 10, 10:30 EDT
- Contact Author: r.russell@ieee.org
- Discuss This Evening w/ H. Ehrenberg
- Common Questions Part of Presentation Thursday

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