IEEE P1581 revisited

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Objective

- P1581 Emulation Board
- Example Test Flow
- Compare Test Methods

Disclaimer: P1581 Working Group may or may not agree with content.
P1581 – A quick review

• Simple Test Logic Implementation for Memory Devices *(and possibly other complex, slave-type components)*

• No extra pins required

• Not relying on complex Memory Access Cycles

• Fast test execution, small test vector set

• Usable with any access methodology *(BScan, functional, embedded, even ICT)*
P1581 Concept

Normal Mode

controlling device (e.g. Boundary Scan)

Data Bus
Address Bus
Control Signals

/CE

P1581 Circuitry

Memory
P1581 Concept

P1581 Test Mode

controlling device (e.g. Boundary Scan)

Data Bus

Address Bus

Control Signals

Logic

P1581 Circuitry

Memory

/CE
P1581 Emulation Board

BScan TAP
XH500

Memory Controller (FPGA)
U500

P1581 Emulator (FPGA)
U202

Fault Simulation Switches
S300

for alternative access to memory device pins

Memory Module

ISP TAP
XH200
sEEEPROM U200
P1581 Emulation Board

- Memory Controller (BScan Device)
- Memory Module (holding SRAM)
- Fault Switches
P1581 sequence

TMode A:
OE* inactive, WE*, CE1*, CE2 and either BYTE* or both BLE* and BHE* simultaneously and continuously active for more than 150 µs

TMode B:
apply OE*, WE*, CE1*, and CE2 simultaneously

Apply command (using address signals) and read 32 bit device ID (bit-wise or 8 bit word-wise)

Apply stimulus pattern on address signals (inputs) and observe and evaluate response pattern on data signals (outputs), linked through P1581 test logic

Apply command (using address signals) and toggle control signals N times, then read out counter values

Apply command (using address signals) and execute optional test functions/algorithms (e.g. BIST, initialization, etc.)

Test mode resets immediately with functional write access and with special command (A18 through A01 driven with a binary value of 1111100000111111, while A00 transitions from a logic zero to a logic 1)
SRAM Results

Number of Response Vectors

SVF Test File Size [KByte]

Number of DRShifts

- BScan Memory Access Test (with Diagnostics)
- BScan Memory Access Test (without Diagnostics)
- P1581 Continuity Test (with Diagnostics)

{Less is better in all four graphs.}

P1581 Demo Board discussion and demonstration – Board Test Workshop 2008
In summary ...

• Are there alternative methods for testing connections to memories?

• Would you like to see P1581 become reality?

http://grouper.ieee.org/groups/1581