Benefits of board and system level memory cluster test with IEEE P1581

Heiko Ehrenberg, GOEPEL Electronics
Kenneth P. Parker, Agilent Technologies
Bradford Van Treuren, Lucent Technologies
Purpose

• Illustrate the use of IEEE P1581 in memory
• Value proposition for IEEE P1581:
  – Benefits for board level manufacturing test
  – Benefits for system test and embedded test
Outline

• What problems does IEEE P1581 solve?

• Memory test applications without and with P1581

• Who benefits from IEEE P1581?
Types of Memory Cluster Tests

• **Memory without Test Mode:**
  
  – **Software based functional test:**
    
    *functional access by firmware*
    
    ➔ Manual test development;
    ➔ What if board/system does not boot up?

  
  – **IEEE 1149.1 based cluster test:**
    
    *access from IEEE 1149.1 in memory host device*
    
    ➔ Long test programs;
    ➔ Timing problems;

  
  – **Hardware based BIST:**
    
    *functional access by BIST hardware in memory host device*
    
    ➔ Not widely available;
Types of Memory Cluster Tests

• Memory with Test Mode:
  – IEEE P1581 built in:  
    combinational test logic in memory
    » Automated test development;
    » Test access from IEEE 1149.1 devices or through probes;
    » Memory core is bypassed, no timing issues;
    » Few test vectors;
  
  – IEEE 1149.1 built in:  
    memory pins tested in interconnect test
    » No special cluster test required;
    » Four extra pins (IEEE 1149.1 Test Access Port)
IEEE P1581 principle

External access to memory device pins (e.g. from Boundary Scan device pins)

IEEE P1581 device

Memory Controller

Test Ctrl. or TTM

Memory Cells

Combinatorial Test Logic

Input bus

Output bus

Test pin (if no TTM)

Benefits of board and system level memory cluster test with IEEE P1581

http://grouper.ieee.org/groups/1581/
IEEE P1581 principle

Boundary Scan device (IEEE 1149.1)

Input bus

Output bus

IEEE P1581 device

Memory Controller

TTM

Memory Cells

Combinatorial Test Logic
IEEE P1581 principle

In-Circuit Tester (bed-of-nail fixture)

IEEE P1581 device

Memory Controller

TTM

Memory Cells

Combinatorial Test Logic

Input bus

Output bus

Benefits of board and system level memory cluster test with IEEE P1581

http://grouper.ieee.org/groups/1581/
IEEE P1581 principle

- BIST or functional access
  (e.g. embedded into FPGA)

Diagram:
- IEEE P1581 device
  - Memory Controller
  - TTM
  - Memory Cells
  - Combinatorial Test Logic

Input bus: x
Output bus: y

Benefits of board and system level memory cluster test with IEEE P1581
http://grouper.ieee.org/groups/1581/
SDRAM Cluster Test – BScan only

• Functional write and read access to RAM
• Requires control over SDRAM clock
• Example:
  – scan chain of 1900 cells, TCK = 10 MHz (typ. less!)
  – Memory cluster test comprises 1840 Shift-DR cycles
  – Total shift time: 350 milliseconds
  – Actual test execution time: ~ 2 sec ... 10 sec(or more)
  – File size: ~ 10 kByte (binary) ... 100+ kByte (ASCII)
SDRAM Cluster Test – with P1581

- Utilizing combinatorial test logic embedded in RAM
- No timing problems
- Example:
  - scan chain of 1900 cells, TCK = 10 MHz (typ. less!)
  - Memory cluster test comprises 48 Shift-DR cycles
  - Total shift time: 9 milliseconds
  - Actual test execution time: << 1 sec
  - File size: << 1 kByte (binary) ... <10 kByte (ASCII)
FLASH EEPROM – BScan only

(a) Check ID codes only

(b) Read and compare known good data

(c) Test of FLASH EEPROM based on write and read access:
   – Multiple erase cycles
   – Very time consuming
   – May not be possible
FLASH EEPROM – with P1581

- Combinatorial test logic embedded in FLASH
- No erase required
- First practical test method for FLASH EEPROM
Conclusion

• IEEE P1581 provides real benefits:
  – Enabling new test applications
  – Improving existing test applications
  – Simple implementation, little overhead
  – Simple test pattern
  – Small test programs (embedded test)

• Need input from Chip vendors

http://grouper.ieee.org/groups/1581/