P1581 – Recent Enhancements Expand Applicability

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Includes methods under development by P1581 Working Group

RJR BTW 14 SEP 2006

Outline

- Brief History of Memory Test
- ETTM Overview (Enhanced Transparent Test Mode
- Review of P1581 Purpose & General Approach
- ETTM Testmode Entry / Exit / Operations
- Detailed Testmode Entry / Exit Examples
- Continuity Test Circuit Example
- ETTM Command Structure / Examples
- Conclusion
- Quiz

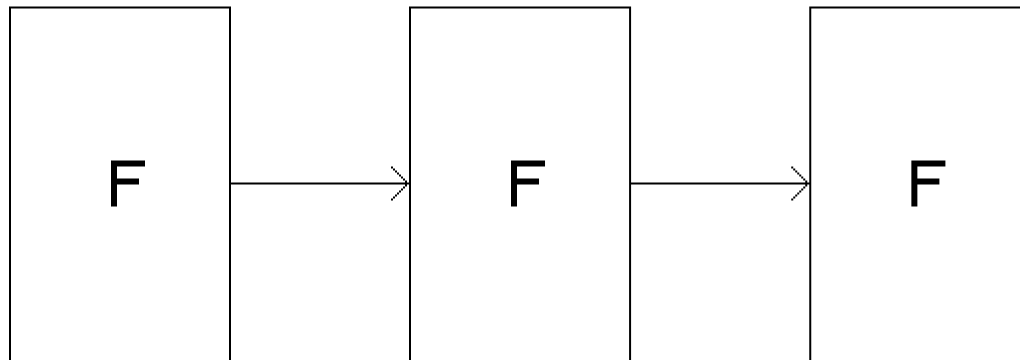
Memory Test History – Myopic View

- Functional Test Performed
- 4 Testpin IEEE 1149.1 Announced
- Tacitly Ignored by Memory Industry
- 1 Testpin P1581 Proposed (early version)
- Also Tacitly Ignored
- 0 Testpin P1581 Proposed (ETTM - 6/2006)
- Response TBD

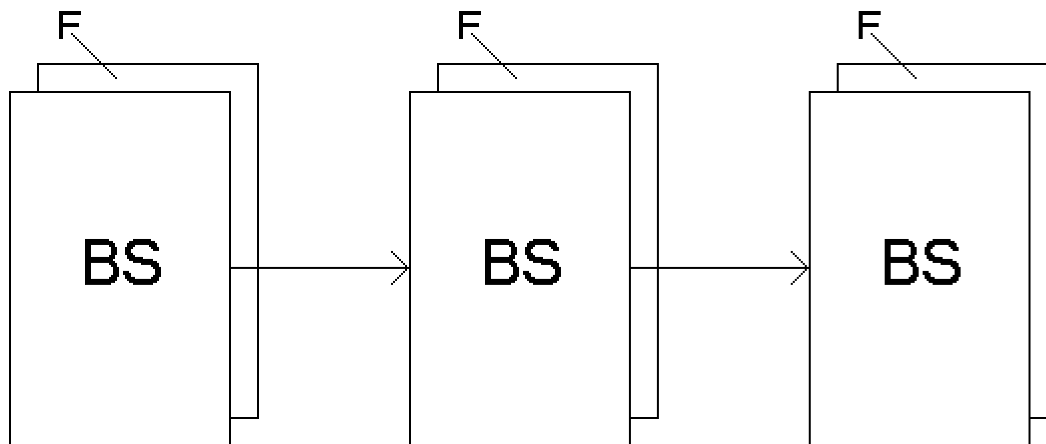
Enhanced Transparent Test Mode

- No Testpins
- Applicable to All Memory Types
  (Volatile, Non-Volatile, Read-Only)
- Package Compatibility w/ Non-P1581 Devices
- Functional Compatibility w/ Non-P1581 Devices
- Supports Continuity Test (Mandatory)
- Supports Options Selected by Designer
  (BIST, Self-Repair, Public, Proprietary)
- No Testpins Required for Option Support
- Unlimited Testmode Entry / Exit

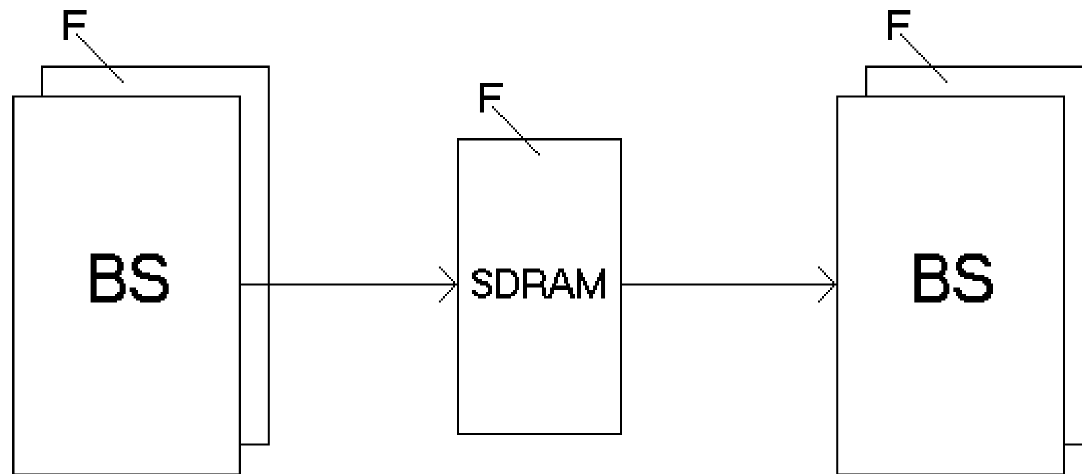
PWB Connectivity Test Challenge



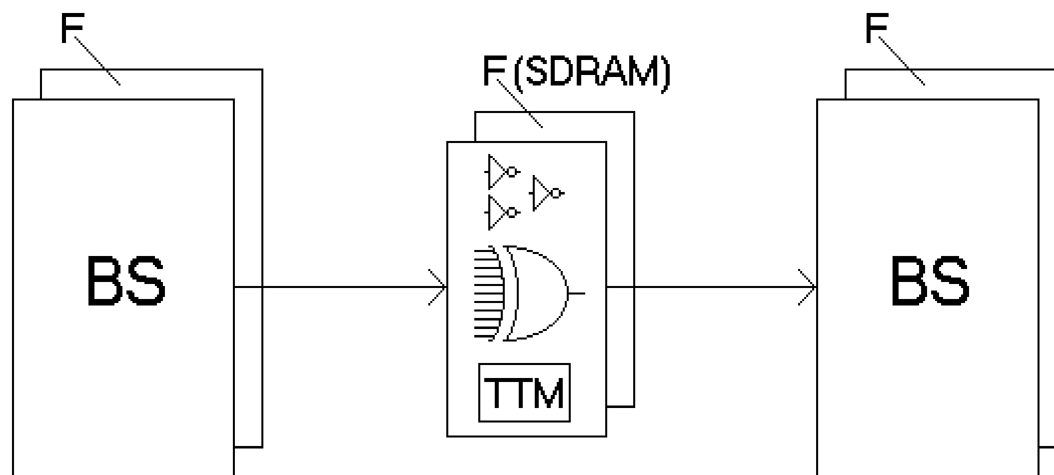
PWB Connectivity Test Solution



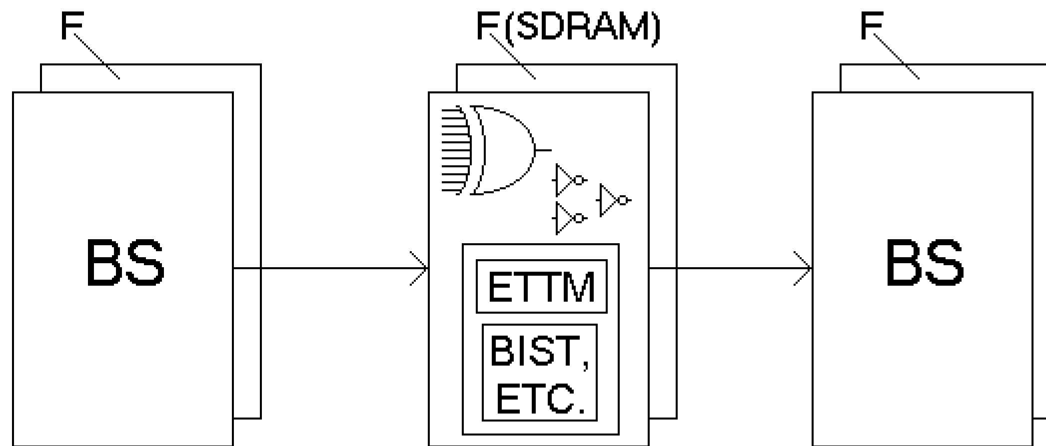
PWB w/ Memory Challenge



PWB w/ Memory Solution



Enhanced Solution (ETTM)



ETTM Test Mode Entry Options (Selected by Device Designer)

- * BScan Stimulus (Non-Functional)
- * Analog Level
- Clock Frequency Shift
- Input State(s) at Power Up
- Always at Power Up

* = Examples Follow

ETTM Test Mode Exit Options (Selected by Device Designer)

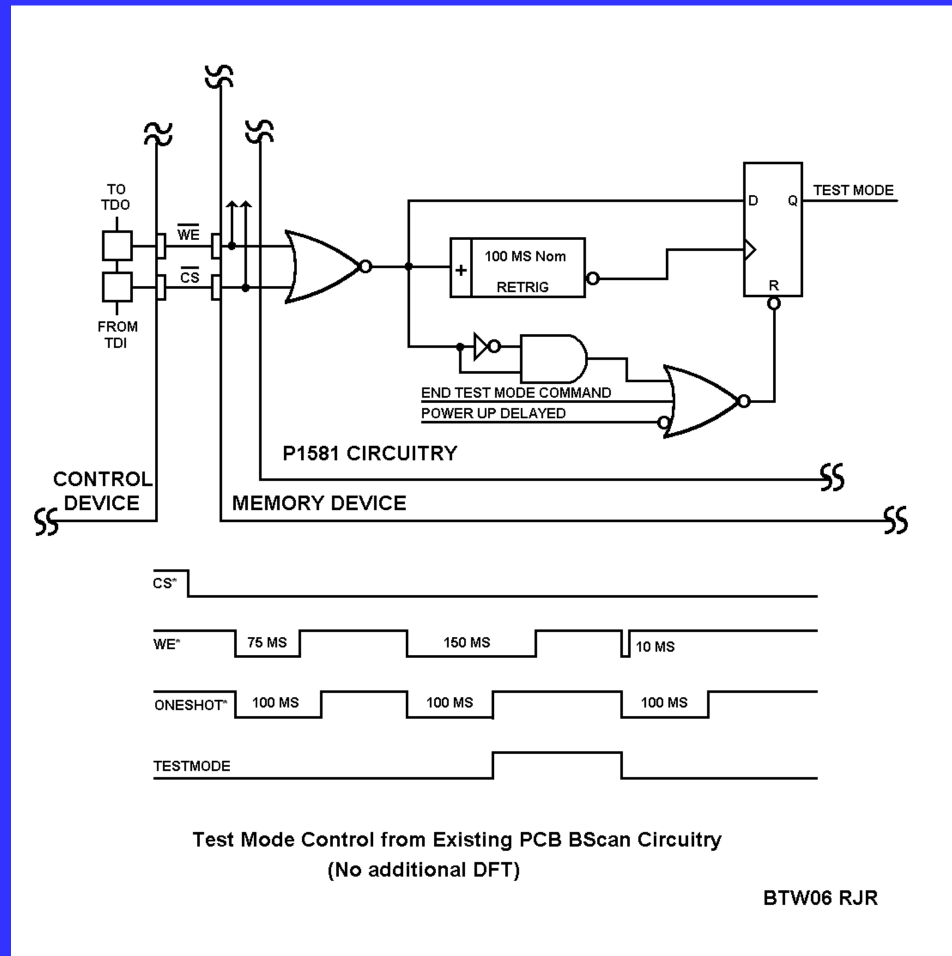
- * BScan or Functional Stimulus
- * Analog Level
- Clock Frequency Shift
- Timeout
- Write
- Command

* = Examples Follow

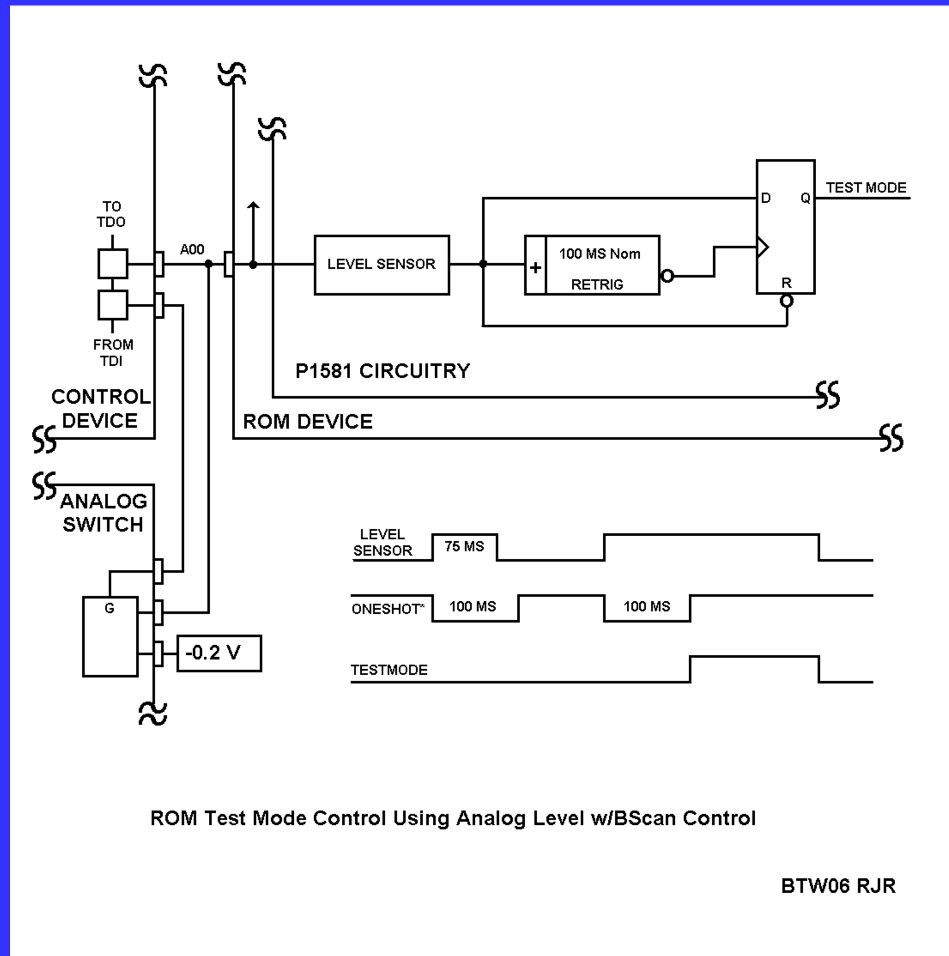
ETTM Test Mode Operations (Selected by Device Designer)

- Continuity Test (Mandatory)
- BIST
- Self - Repair
- Exit Testmode
- Testmode Reactivation Control
- Other
- Device Mfr. – Public, Proprietary

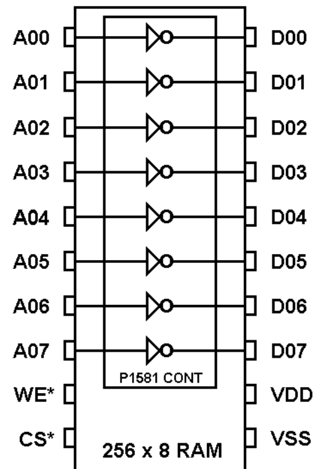
ETTM Control via BScan Stimulus



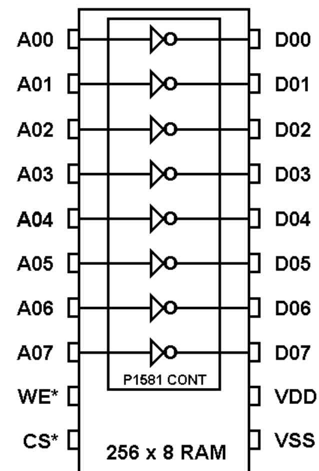
ETTM Control via Analog Level



Continuity Test Gating Example



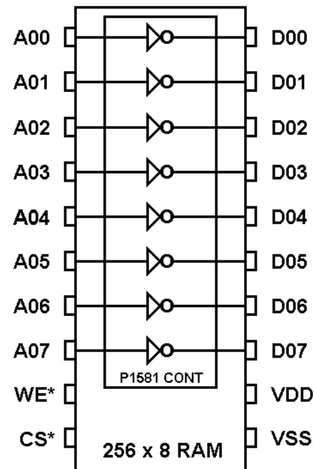
Test Pattern Breakdown



TEST PATTERNS
AVAILABLE

2 - ALL 0/1
16 - 1 @ 0/1
56 - 2 @ 0/1
112 - 3 @ 0/1
70 - 4 @ 0/1
256

Patterns – Necessary vs. Spare



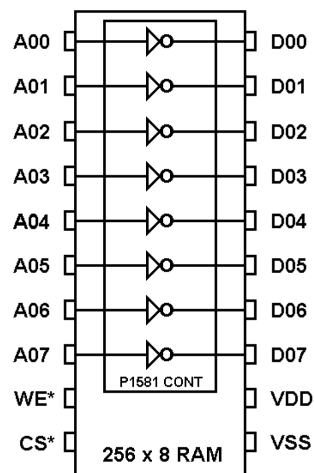
NECESSARY
TEST PATTERNS

2 - ALL 0/1
16 - 1 @ 0/1
56 - 2 @ 0/1

SPARE
TEST PATTERNS

112 - 3 @ 0/1
70 - 4 @ 0/1

Command Examples



EXAMPLE COMMANDS

A00 … A07

Codes	Command
00000111 10000111	- START BIST
00001011 10001011	- STOP BIST, REPORT
00001101 10001101	- OUTPUT ERROR ADDR
00111000 10111000	- ACTIVATE REPAIR GP0
00110100 10110100	- DEACTIVATE GP0
00110010 10110010	- REPORT GP0 ADDR
01110000 11110000	- END TEST MODE

Conclusion

- Memory Test Methods Prior to 6/2006 Discussed
- ETTM Benefits Explained
- ETTM Compatibility, No Testpins Emphasized Ad Nauseum
- Overall Purpose of P1581 Reviewed
- Overview of ETTM Testmode Entry / Exit / Operations
- Detailed Examples of ETTM Testmode Control
- Command Derivation from Test Patterns Explained
- Command Examples Discussed

Quiz

How many package pins must be added in implementing P1581 as part of the redesign of an existing memory device?

A. 0

B. 1

C. 2.5

D. 4