P1581 – Recent Enhancements
Expand Applicability

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Includes methods under development by P1581 Working Group

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Outline

- Brief History of Memory Test
- ETTM Overview (Enhanced Transparent Test Mode)
- Review of P1581 Purpose & General Approach
- ETTM Testmode Entry / Exit / Operations
- Detailed Testmode Entry / Exit Examples
- Continuity Test Circuit Example
- ETTM Command Structure / Examples
- Conclusion
- Quiz

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Memory Test History – Myopic View

• Functional Test Performed
• 4 Testpin IEEE 1149.1 Announced
• Tacitly Ignored by Memory Industry
• 1 Testpin P1581 Proposed (early version)
• Also Tacitly Ignored
• 0 Testpin P1581 Proposed (ETTM - 6/2006)
• Response TBD

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Enhanced Transparent Test Mode

- No Testpins
- Applicable to All Memory Types
  (Volatile, Non-Volatile, Read-Only)
- Package Compatibility w/ Non-P1581 Devices
- Functional Compatibility w/ Non-P1581 Devices
- Supports Continuity Test (Mandatory)
- Supports Options Selected by Designer
  (BIST, Self-Repair, Public, Proprietary)
- No Testpins Required for Option Support
- Unlimited Testmode Entry / Exit

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PWB Connectivity Test Challenge
PWB Connectivity Test Solution
PWB w/ Memory Challenge

BS -> SDRAM -> BS
PWB w/ Memory Solution
Enhanced Solution (ETTM)
ETTM Test Mode Entry Options
(Selected by Device Designer)

- * BScan Stimulus (Non-Functional)
- * Analog Level
- Clock Frequency Shift
- Input State(s) at Power Up
- Always at Power Up

* = Examples Follow

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ETTM Test Mode Exit Options
(Selected by Device Designer)

• * BScan or Functional Stimulus
• * Analog Level
• Clock Frequency Shift
• Timeout
• Write
• Command

* = Examples Follow

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ETTM Test Mode Operations
(Selected by Device Designer)

• Continuity Test (Mandatory)
• BIST
• Self - Repair
• Exit Testmode
• Testmode Reactivation Control
• Other
• Device Mfr. – Public, Proprietary

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ETTM Control via BScan Stimulus

Test Mode Control from Existing PCB BScan Circuitry
(No additional DFT)

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ETTM Control via Analog Level

ROM Test Mode Control Using Analog Level w/ iBScan Control

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Continuity Test Gating Example

Diagram of a 256 x 8 RAM circuit with labels for A00 to A07, D00 to D07, WE*, and CS*.
Test Pattern Breakdown

- Available test patterns:
  - 2 - ALL 0/1
  - 16 - 1 @ 0/1
  - 56 - 2 @ 0/1
  - 112 - 3 @ 0/1
  - 70 - 4 @ 0/1
  - 256
Patterns – Necessary vs. Spare

- **NECESSARY TEST PATTERNS**
  - 2 - ALL 0/1
  - 16 - 1 @ 0/1
  - 56 - 2 @ 0/1

- **SPARE TEST PATTERNS**
  - 112 - 3 @ 0/1
  - 70 - 4 @ 0/1

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Command Examples

![Diagram of 256 x 8 RAM with example commands]

**EXAMPLE COMMANDS**

<table>
<thead>
<tr>
<th>A00</th>
<th>A07</th>
</tr>
</thead>
<tbody>
<tr>
<td>00000111</td>
<td>- START BIST</td>
</tr>
<tr>
<td>10000111</td>
<td>- STOP BIST, REPORT</td>
</tr>
<tr>
<td>00001101</td>
<td>- OUTPUT ERROR ADDR</td>
</tr>
<tr>
<td>10001101</td>
<td>- ACTIVATE REPAIR GP0</td>
</tr>
<tr>
<td>00110100</td>
<td>- DEACTIVATE GP0</td>
</tr>
<tr>
<td>10110100</td>
<td>- REPORT GP0 ADDR</td>
</tr>
<tr>
<td>00110010</td>
<td>- END TEST MODE</td>
</tr>
</tbody>
</table>

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Conclusion

• Memory Test Methods Prior to 6/2006 Discussed
• ETTM Benefits Explained
• ETTM Compatibility, No Testpins Emphasized Ad Nauseum
• Overall Purpose of P1581 Reviewed
• Overview of ETTM Testmode Entry / Exit / Operations
• Detailed Examples of ETTM Testmode Control
• Command Derivation from Test Patterns Explained
• Command Examples Discussed

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Quiz

How many package pins must be added in implementing P1581 as part of the redesign of an existing memory device?

A. 0
B. 1
C. 2.5
D. 4

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