PROBLEMS USING BOUNDARY-SCAN FOR MEMORY CLUSTER TESTS

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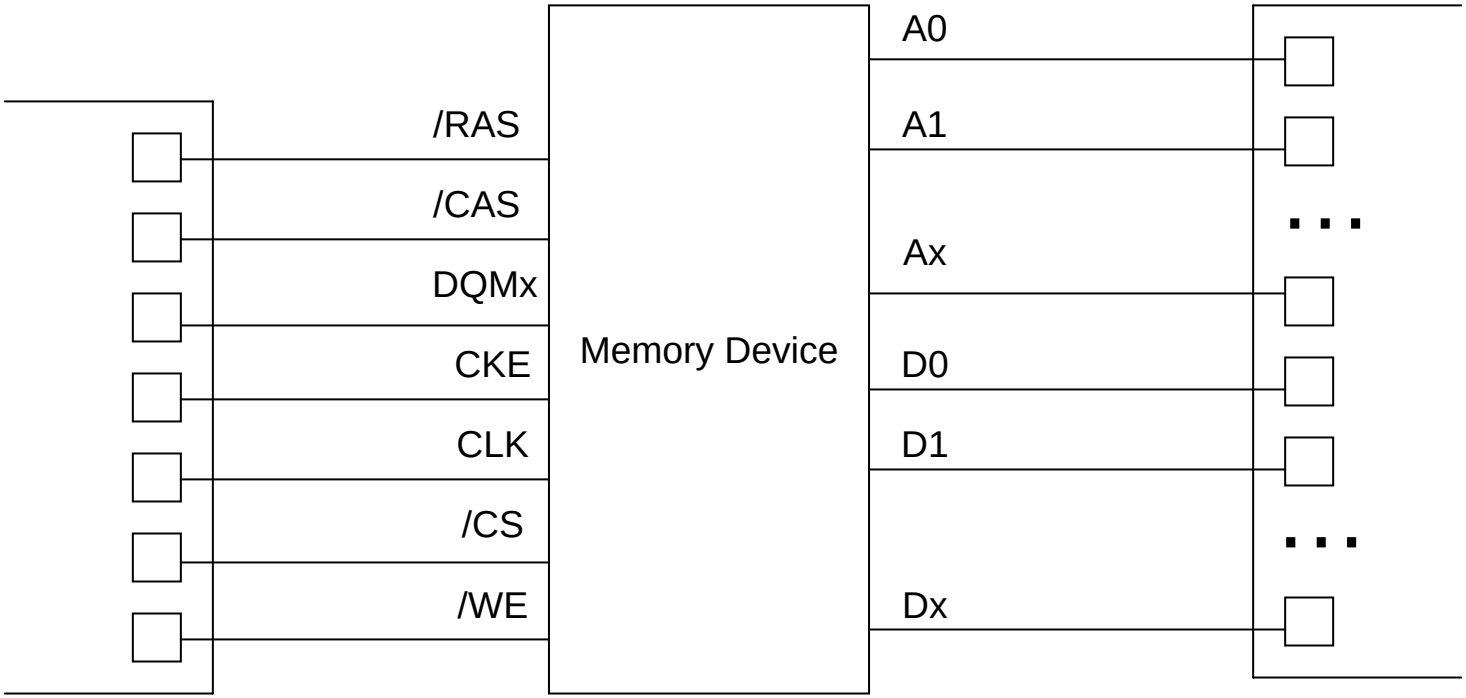
Outline

- Memory Cluster Test Development Process Overview
- Memory Model Test Cases
- More Problems Related to FPGAs
- Problems of Consistency Across Manufacturing Station Controllers
- Alternatives for Testing
- Conclusions

Memory Cluster Test Development Process

Basics of Memory Cluster Testing



Memory Cluster Test Development Process

Fallacies of the process

- Functional Model access can be emulated with Boundary-Scan
- The Cluster Test will work with any set of Boundary-Scan drivers and observers
- All TAP interfaces behave the same way
- The algorithm timing for access may be defined using a set of parallel vectors for read and write cycles
- Current ATPG products provide tools to easily debug functional models of algorithms

Memory Cluster Test Development Process

Debug of Models

- Debug based on trial and error with current design
- Requires use of other tools (e.g., scopes, logic analyzer) when model does not work
- Access to memory interface signals may not be possible for additional tools
- Time to debug a model may be from a few hours to person months of development
- One model does not always work for other circuits using the same memory

Memory Model A Test Case

Tool Vendor Assistance Required for Modified Model

Host Device	Memory Part	Memory Type	Model Instance	Time to debug	Tester Comments
FPGA	MT46V32M16FN-6I	DDR-SDRAM	Model A	8 hours	Model finally received from tool supplier
ASIC	MT46V32M16FN-6I	DDR-SDRAM	Model A	Fails so split to 2 below	Worked for 4 instances and fails for 1 instance (Tool bug)
ASIC	MT46V32M16FN-6I	DDR-SDRAM	Model A		Works as expected first time
ASIC	MT46V32M16FN-6I	DDR-SDRAM	Model A		Works as expected first time

Memory Model B Test Case

One Model does not fit all instances

FPGA (47..32)	MT46V16M16FG	DDR-SDRAM	Model B	Debugging > 3 mo.	Same Model works with similar design on another board for one DDR-SDRAM.
FPGA (63..48)	MT46V16M16FG	DDR-SDRAM	Model B	Debugging > 3 mo.	Same Model works with similar design on another board for one DDR-SDRAM.
ASIC (15..0)	MT46V16M16FG	DDR-SDRAM	Model B	4 hours+ongoing	Made control pins optional to get test to work
ASIC (31..16)	MT46V16M16FG	DDR-SDRAM	Model B	ongoing	Made control pins optional to get test to work
ASIC (47..32)	MT46V16M16FG	DDR-SDRAM	Model B	ongoing	Fails all instances
ASIC (63..48)	MT46V16M16FG	DDR-SDRAM	Model B	ongoing	Made control pins optional to get test to work
ASIC ECC(7..0)	MT46V16M16FG	DDR-SDRAM	Model B	ongoing	Made control pins optional to get test to work

Memory Model C Test Case

Problems Controlling Clock

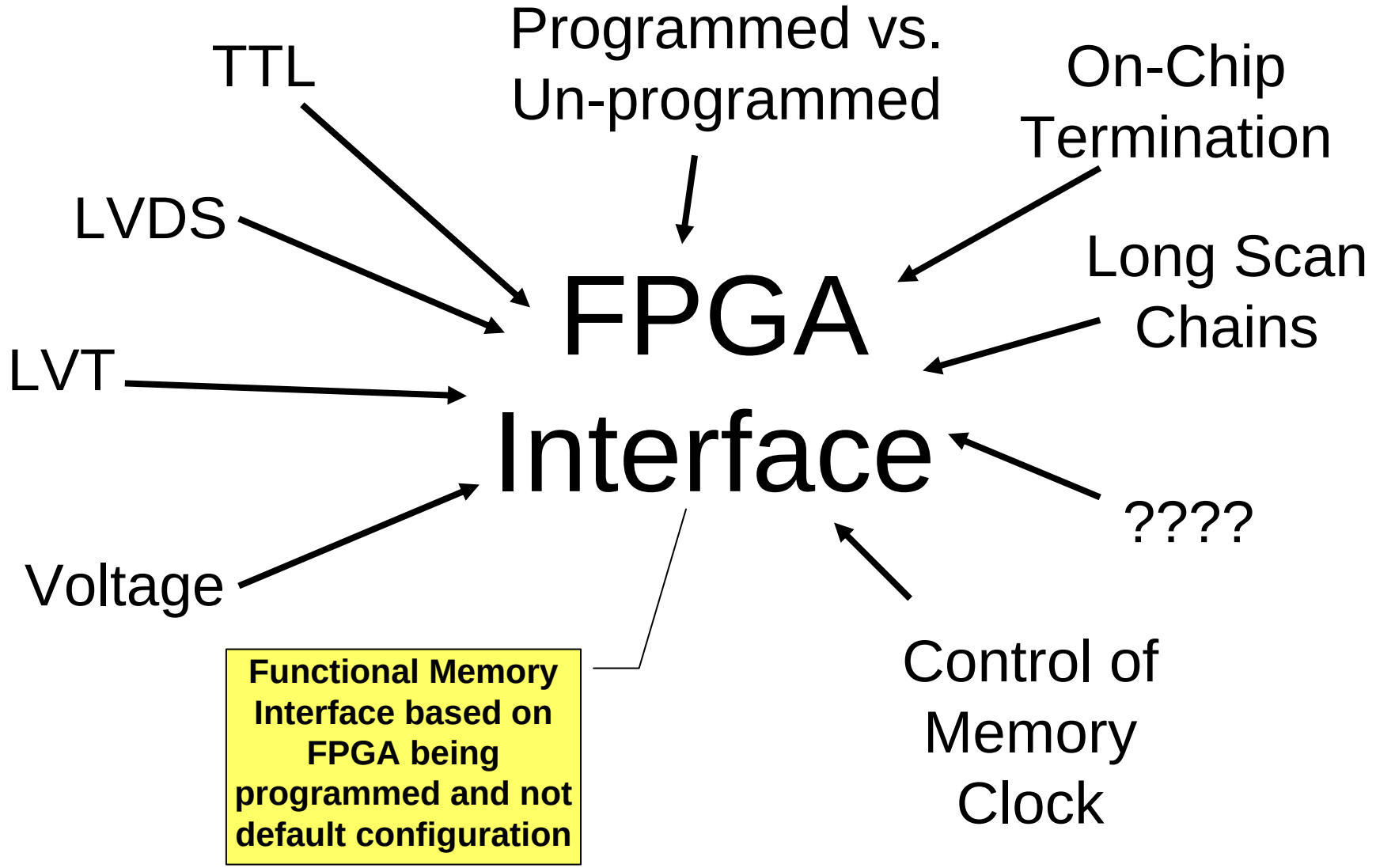
Host Device	Memory Part	Memory Type	Model Instance	Time to debug	Tester Comments
DSP (15..0)	MT48LC8M16A2-75I	SDRAM	Model C	8 hours+on going	clock of mem via DSP controlled buffer
DSP (31..16)	MT48LC8M16A2-75I	SDRAM	Model C	ongoing	clock of mem via DSP controlled buffer

Memory Models D, E, F, and G Test Cases

SRAMs Easy – SDRAMs Difficult (Assistance Required)

Host Device	Memory Part	Memory Type	Model Instance	Time to debug	Tester Comments
ASIC,FPGA,CPLD	7C1021CV33-10	SRAM	Model D	1 hour	Passed first try
CPU	MT46V64M8	DDR-SDRAM	Model E	8 hours	Solution eventually provided by tool vendor
CPU	MT47H64M8	DDR2-SDRAM	Model F	4 hours	Passed with minor rework
FPGA	MT46V16M16FG-75I_FBGA	DDR-SDRAM	Model G	16 hours	After eliminating model hardware, found a note in a similar user defined model suggesting a fix to a similar problem. Created my own user model, made the modification and then the model worked.

More Problems Related to FPGAs



Problems of Consistency Across Manufacturing Station Controllers

- Set of factors affecting consistency and repeatability of tests from manufacturing station to manufacturing station (Especially for synchronous memory):
  - Effective TCK frequency (Not TCK frequency but average frequency)
  - TAP Controller vector reload overhead
  - Speed of hosting computer applying vectors (Most critical)
  - Speed of interface bus between hosting computer and test controller
  - Speed of hosting interface bus to the test controller (e.g., USB 1.1 vs. USB 2.0 – USB 1.1 proved to be 40x slower)

Example of different controllers for a test (~1MHz TCK over Multi-drop Backplane)

TestType	3GHz P4, 1GB RAM, PCI		3GHz P4, 1GB RAM, USB 2.0		1GHz P3, 256MB RAM, USB 2.0 Cardbus Interface	
	Test Time (Sec.)	Test Status	Test Time (Sec.)	Test Status	Test Time (Sec.)	Test Status
FPGA1 Erase	8.72	PASS	7.25	PASS	15.78	PASS
FPGA2 Erase	4.77	PASS	4.58	PASS	4.78	PASS
Interconnect	7.53	PASS	7.01	PASS	18.33	PASS
FPGA1 Program	7.09	PASS	12.69	PASS	44.37	PASS
FPGA2 Program	2.80	PASS	4.28	PASS	10.14	PASS
Flash IDCode	6.11	PASS	5.78	PASS	17.05	PASS
SDRAM1	8.48	PASS	9.03	PASS	13.01	PASS
SRAM	4.17	PASS	4.16	PASS	5.54	PASS
SDRAM Cluster(4)	6.42	PASS	7.77	PASS	13.57	PASS
SDRAM2	6.34	PASS	7.69	PASS	13.46	PASS
SDRAM3-7 Cluster	17.47	FAIL	9.7	FAIL	23.13	FAIL
SDRAM3	15.78	FAIL	17.95	FAIL	24.22	FAIL
SDRAM4	18.44	FAIL	18.12	FAIL	23.07	FAIL
SDRAM5	17.34	FAIL	18.14	FAIL	24.77	FAIL
SDRAM6	13.37	PASS	18.03	FAIL	23.32	FAIL
SDRAM7	15.94	FAIL	23.92	FAIL	23.13	FAIL

Alternatives for Memory Cluster Testing

- Device changes to map functional test to standard structural test facilities
  - Memory vendors add IEEE 1149.1 support directly to memory devices
  - IEEE P1581 to turn at-speed/pseudo-near-speed testing into a true 1149.1 interconnect cluster test
- Work-arounds
  - In-Circuit Test if test points are able to be equipped (no EBST support)
  - Build memory cluster BIST into the memory controller interface device reusing at-speed functional interface (esp. FPGA design)
  - Build P1581 aware BIST into the memory controller interface if P1581 is available in memory device (Best for EBST for concurrency with short test time)
  - Rely solely on Software Functional Test for debug

Conclusions

- Memory Cluster Test does not guarantee a workable test for all instances
- Because a test works on one circuit does not mean it will work for another
- FPGAs present a special class of problems for Memory Cluster Test due to the variability of the interface characteristics
- Debugging of Memory Model definitions is cumbersome at best – most time additional test equipment is required
- Boundary-Scan is running out of steam for memory test support as memory gets more complicated and faster
- Memory cluster BIST or P1581 BIST reuses functional test interface in the memory controller and provides concurrent test and detailed diagnostics (Works for FPGAs)