What is happening with IEEE P1581?

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Memory devices have been becoming more complex with every generation and this trend will continue. Different kinds of memories present different challenges for board level test applications.
Ideally, connectivity to the memories on a Unit Under Test should be verified, detecting and locating any opens, stuck-at faults or shorts before moving on to functional test. Unfortunately, most of these memories do not implement Boundary Scan resources (IEEE 1149.1 resources [1]).
Conventional approaches, utilize the memory's functionality to verify its connectivity by writing a test pattern into the memory and then reading this pattern out again. This can cause all kinds of problems, such as long test execution times, difficulty creating test applications, and reduced quality of diagnostics. In some cases such an approach may not even be possible. For example, if Boundary Scan is used for board level interconnect test and the memory device to be tested is a synchronous DRAM device, a test would be only possible if the memory's clock pin(s) can be controlled via Boundary Scan as well. [2]

In an attempt to overcome these problems, the IEEE P1581 working group is defining a protocol and architecture for static component interconnection test. This standard [3] is being developed to define a test strategy for complex memory devices which do not support IEEE 1149.1. It describes a means to verify the memory I/O pin connectivity (address, data, and control signals). The memory cell structure is completely bypassed; a combinational test circuitry implemented into the memory device is used instead during test mode to link input and output signals. A controlling device (typically an IEEE 1149.1 compliant component connected to the memory device) applies a stimulus to the input pins and observes the output pins of the device under test.

IEEE P1581 defines two test architectures, one of which is patented, while the other one appears to be in the public domain. Test logic implementations may differ in the quality of fault diagnosis they support. The P1581 draft document requires that faults on the P1581 device pins can at least be detected, if not diagnosed.
The draft document also specifies two test mode control methods, one of which is utilizing a dedicated test enable pin, while the other method works without an extra pin (referred to as TTM). The test mode entry and exit protocols vary for those two methods.

At a board level, the P1581 device – most likely a memory component – is connected to some kind of host or master device. The draft document recommends that this master device is IEEE-Std. 1149.1 compliant. This will be the case most of the time, since today's more complex digital components, such as CPU's, DSP's, PLD's and FPGA's, as well as many custom ASIC's, have Boundary Scan test resources built in. For the purpose of an interconnect test between the master device and the P1581 device, latter is put into test mode, causing the test logic to be connected to the device inputs and outputs, bypassing the functional circuitry (e.g. the memory area) of the device. Test pattern is then applied to the inputs by the master device, while the outputs are observed. Since the test system applying those test pattern knows the structure of the test logic or at least the expected response pattern, it can then determine whether or not the response pattern on the P1581 device's output pins are as expected or not. In case the response pattern differs from the expected pattern, a fault has been detected and the affected pin(s) can be diagnosed (diagnostic capabilities depend on the test logic implementation and test pattern).

It is likely that there will be more than one P1581 device connected to the same data bus. The test system needs to make sure that only one of these P1581 devices is actively driving its outputs at any given time, avoiding any bus contentions. Since all P1581 devices most likely will enter test mode concurrently, additional control signals, such as Chip Enable and/or Output Enable need to be asserted respectively.
The P1581 draft document clearly specifies how pins of a compliant component are to be connected to the test circuitry and which pins must be excluded from the test circuitry.

The remaining tasks for the P1581 working group are mainly of editorial nature. Certain parts of the draft document have to be reworded to cover all allowed test circuitry and test mode control architectures. Those interested in joining the efforts or just following the progress please contact Heiko Ehrenberg at h.ehrenberg@ieee.org.

[1] IEEE Computer Society, *IEEE Standard Test Access Port and Boundary Scan Architecture - IEEE Std. 1149.1 2001*, IEEE, New York, NY, 2001
[2] Heiko Ehrenberg, Norbert Muench, *Leveraging Boundary Scan resources for comprehensive cluster testing*, Proceedings of BTW2004
[3] IEEE P1581 D1.11, website: http://grouper.ieee.org/groups/1581/