What is happening with IEEE P1581?

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Purpose

“IEEE Std. 1581 will make you forget you ever had a memory problem”

Bob Russell
Outline

• Why do we need P1581?
• How does P1581 work?
• What are possible implementations?
• What is the impact on Board level test?
• Current status of development
Why do we need P1581?

- DDR-SDRAM, DDR2-SDRAM, FLASH, etc.
  - 1149.1 not built in!
  - Controllability
  - Complexity
  - Test time
  - Test conditions
    *(use of untested resources to test the DUT)*
How does P1581 work?

Example: memory device

IEEE Std. P1581 device

- Memory Controller
- Test Control
- TTM (optional)
- Memory Cells
- Combinational Test Logic
- Test Pin (if no TTM)

Micro Controller, or other host device

Input bus \( x \)

Output bus \( y \)
P1581 test logic circuitry

- XOR/XNOR, or Inverters/AND
- Only combinational, non-sequential logic
- Easy to implement, simple test vectors
- Faults on pins don't inhibit test of other pins
- Fault detection guaranteed
- Fault diagnostics depends on implementation, test vectors
- Patented vs. public domain
Entering and leaving Test Mode

Test Pin
- Dedicated test enable pin
- Unconditional test mode access
- Active state defined by chip designer

TTM (Transparent Test Mode)
- No dedicated pin
- P1581 mode until first write
- Not usable for certain devices (e.g. FLASH)

TTM:

<table>
<thead>
<tr>
<th>Power On</th>
<th>write access detected</th>
<th>Power Off</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1581 test mode outputs = f(inputs)</td>
<td>functional mode</td>
<td>t</td>
</tr>
</tbody>
</table>

What is happening with IEEE P1581?  http://grouper.ieee.org/groups/1581/
Board level test and P1581

• Simple, quasi-static interconnect test
  (no need for at-speed access or initialization)
• Multiple P1581 devices in bus structure
Current status of development

• Test logic architecture defined; editorial work remains;
• Test mode control defined; editorial work remains;
• Description language defined
• Completed draft expected for early 2006
  → Ballot in 2006
Conclusion

Before P1581:
- FLASH device connections not easily testable
- Synchronous memory devices may cause test problems

Now:
- P1581 = an elegant solution
- A perfect match for Boundary Scan

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