Abstract:
IEEE P1581 is aimed at ICs that are otherwise not provisioned with Design For Test (DFT) for any reason, targeting primarily memory devices, but also allowing for implementation in other devices. This Poster provides an overview of Test Mode Entry and Exit Methods proposed in IEEE P1581.

Introduction
IEEE P1581 will provide the specification of protocol and implementation rules helping vendors to implement test hardware functionality in their ICs (Integrated Circuits) to support connectivity tests, Device ID Code, and built-in self test (BIST) in a standardized manner. Without such an independent standard, interoperability amongst ICs is unlikely, jeopardizing reuse of any implemented test technology at board and system levels and, as such, failing to provide the intended test coverage.

Part of the IEEE P1581 specification are various test mode entry and exit methods, all but one of which do not require any extra device pins. The standard proposal is aimed at ICs that are otherwise not provisioned with DFT for any reason, targeting primarily memory devices, but also allowing for implementation in other devices.

IEEE P1581 ..
• Provides a simple test logic implementation for memory devices (and possibly other complex, slave-type components);
• Requires no extra pins;
• Does not rely on complex memory access cycles or critical timing;
• Allows very fast test execution with a small test vector set; and
• Is usable with any access methodology (Boundary Scan, functional, ICT).

Test Mode Entry and Exit Methods proposed in IEEE P1581 include the following:
• Non-Functional Stimulus (NFS),
• Clock Frequency (CKF),
• Code Selection (CDE),
• Analog Level (ANL),
• Power-Up Selection (PST),
• Power-Up Default (PDT),
• Simultaneous Input/Output (SIO), and
• Test Pin (TPN)

Motivation
IEEE P1581 has been developed to define a test strategy for memories and other complex devices that do not support IEEE Std 1149.1 in order to verify I/O pin connectivity and enhance testability. Memory devices have been becoming more complex with every generation and this trend will continue. Different kinds of memories present different challenges for test applications above the IC level. By offering various methods for test mode entry and exit, IEEE P1581 can be applied to many different types of memory devices and other slave-type components.

Most memory ICs do not implement boundary scan (IEEE Std 1149.1). Yet, connectivity to the memories on a unit under test should be verified – detecting and locating any opens, shorts, and other stuck-at faults before moving on to functional test. It is common practice to utilize a memory's functionality to verify its connectivity - writing a test stimulus pattern into the memory and then reading from the memory to check for the matching response pattern. This approach brings problems with it, such as long test execution times, difficulty creating embedded test applications, and reduced quality of diagnostics. In some cases, such an approach may not even be possible.

In an attempt to overcome these problems, the IEEE P1581 working group has been defining a protocol and architecture for component interconnection test [1].

References
http://grouper.ieee.org/groups/1581/