IEEE Std 1581 drastically simplifies connectivity test for memory devices potentially without any extra pins.

IEEE Std 1581 ...
- requires no extra pins;
- uses simple (inexpensive) test logic for memory devices and other complex, slave-type components;
- tests dynamic devices with static stimulus thus avoiding complex memory access cycles, and preserves non-volatile content;
- allows very fast tests with a small test vector set (important for embedded test applications); and
- is usable with any access methodology (ICT, functional, and especially – Boundary Scan);

Further Info: http://grouper.ieee.org/groups/1581/

Menu of Test Logic Implementations

- **XOR**
  - (3-input XOR or XNOR gates)

- **IAX**
  - (XOR, Inverters, and AND gates)

- **XOR-2**
  - (2-input XOR or XNOR gates)

Menu of Test Mode Entry and Exit Methods

- **NFS**
  - (Non-Functional Stimulus; TTM)
  - IEEE 1581 Device

- **DCC**
  - (Designated Command Codes; TTM)
  - IEEE 1581 Device

- **ANL**
  - (Analog Level; TTM)
  - ROM IEEE 1581 Device

- **CKF**
  - (Clock Frequency; TTM), example A
  - IEEE 1581 Device

- **CKF**
  - (Clock Frequency; TTM), example B
  - IEEE 1581 Device

- **SIO**
  - (Simultaneous Input / Output; TTM)
  - IEEE 1581 Device

- **CPI**
  - (Conditional Power-Up Initiation; TTM)
  - Non-Volatile IEEE 1581 Device

- **DPI**
  - (Default Power-Up Initiation; TTM)
  - Volatile IEEE 1581 Device

- **TP** (Dedicated Test Pin)
  - Dedicated Test Pin (no non-test purpose)
  - IEEE 1581 Device

IEEE Std 1581-2011 has been approved in March and published in June 2011.

Join us at the IEEE 1581 fringe meeting on Wednesday, Sept 21, at 3:00pm.