IEEE Std 1581 - A Standardized Test Access Methodology for Memory Devices

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Purpose

• Provide an overview of IEEE Std 1581:
  – Test mode control methods
  – Examples of IEEE 1581 test functions
  – Examples of test logic implementations
  – Possible future extensions
Outline

• History of IEEE Std 1581
• Defects addressed by IEEE Std 1581
• Key elements of IEEE Std 1581
• IEEE 1581 test mode control methods
• IEEE 1581 test functions
• Outlook
The PAR was extended twice in order to complete the standard development effort.
Defects addressed by IEEE Std 1581

IEEE 1149.1 compliant device

IEEE 1581 compliant device

- Bridging fault
- Vcc (stuck-at-1)
- GND (stuck-at-0)
- Open fault
- Bridging fault
- Vcc (stuck-at-1)
- GND (stuck-at-0)
- Open fault
- Bridging fault
Key elements in IEEE Std 1581

- Simple test logic implementation for complex, slave-type devices
- No extra pins required
- No reliance on complex access cycles
- Fast test execution, small test vector set
- Usable with any access methodology (Boundary scan, functional, ICT)
Basic concept

PCB

IEEE 1149.1 device(s)

Input Bus x

Memory Cells

Combinational Test Logic

IEEE 1581 device

Test Control

TTM (optional)

Optional Test Pin (if no TTM)

Output Bus y
Test mode control

- One of seven transparent test mode (TTM) control methods:
  - Non-functional stimulus (NFS)
  - Designated command codes (DCC)
  - Simultaneous input/output (SIO)
  - Clock frequency (CKF)
  - Analog level (ANL)
  - Conditional power-up initiation (CPI)
  - Default power-up initiation (DPI)

- or a Dedicated test pin (TPN)

Test entry or exit is triggered by a condition on the pins that would otherwise never exist under normal functional conditions.

These methods may require additional board-level and/or controlling device DFT to be implemented.
Test mode control – NFS example

IEEE 1149.1 device

/WE

/CS

≥ 150 µs

Enter test mode

IEEE 1581 device

/Write Enable

/Chip Select

< 100 µs

Exit test mode
Test mode control – DCC example

**IEEE 1149.1 device**

**Mode2**

**Mode1**

**Strobe**

**IEEE 1581 device**

**STB = Strobe: triggers capture of mode selection bits**

<table>
<thead>
<tr>
<th>MDS2</th>
<th>MDS1</th>
<th>Mode / description</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Read</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Write</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Enter IEEE 1581 test mode</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Exit IEEE 1581 test mode</td>
</tr>
</tbody>
</table>
Test mode control – CPI example

Test mode is entered if a predetermined set of logical input states exist at a predetermined period after device power-up.
Test logic

• One of three defined test logic architectures:
  – XOR (3-input XOR or XNOR gates)
  – IAX (XOR, Inverters, and AND gates)
  – XOR-2 (2-input XOR or XNOR gates)

• Or a custom test logic that satisfies rules in IEEE Std 1581-2011
Test logic example - XOR

IEEE 1581 memory device

Inputs
I1
I2
I3
I4
I5
I6

Outputs
O1
O2
O3
O4
Optional test functions

- Optional test functions accessible via Test Pattern Partitioning (TPP)
- Examples include:
  - Reading a device identification (ID)
  - Control line continuity test
  - Built-in self test (BIST) access
  - Other public or private commands
Outlook for IEEE Std 1581

- IEEE Std 1581 approved March 2011 and published in June 2011
- Working group is considering future work:
  - Description language
  - Bi-directional test features
  - ...
- More details possibly at BTW 2011
Thank you

For more details and questions, or to join the working group, contact the authors:

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