An Economical Alternative to Boundary Scan in Memory Devices

(White Paper of the IEEE P1581 Working Group)

IEEE P1581 proposes a standard means of including test features in a memory device, which can collaborate with other 1149.1 Boundary-Scan devices, without requiring boundary scan circuitry, complex controllers or dedicated test pins. The result is a memory device design suitable for printed circuit board (PCB) applications, including those where design for test overhead is often deemed economically unacceptable. Recently developed P1581 test mode entry/exit methods have eliminated the dedicated testpin requirement which was part of the original methodology and still remains as a supplier selected option. Also, the original continuity test circuitry has been joined by an equally robust and simple alternative.
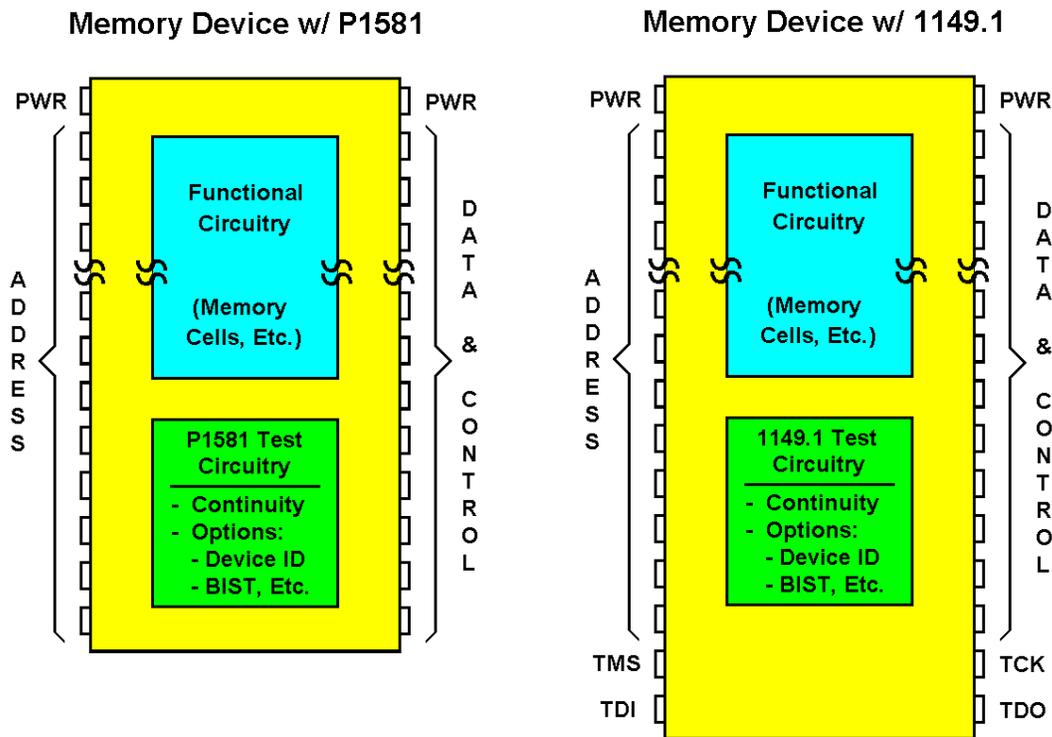

Figure 1. Comparison of Features - P1581 vs. 1149.1

Figure 1 illustrates the features and pinouts of similar memory devices in which test capabilities have been included, P1581 in the device on the left and 1149.1 in the device on the right. When connected to other devices having boundary scan (1149.1) capability, both devices: (1) interface with surrounding boundary scan devices to allow continuity testing, (2) optionally allow JEDEC standard manufacturer, part identifier and revision codes stored within the device to be externally or remotely sensed and (3) optionally allow other supplier selected test options (e.g., BIST, self-repair) to be externally controlled (e.g., by boundary scan test equipment, in-circuit testers [ICT], or PCB built in self test [BIST] circuitry). P1581 has the advantage of not requiring any dedicated test pins. It is important to note that P1581 is not intended to be a general replacement for 1149.1.

P1581 Concept

The general concept of P1581 is shown in Fig. 2. The P1581 memory device on the right has two modes of operation: functional mode and test mode. The circuitry to operate in functional mode, including the memory cell array, is represented by the blue box. The two green boxes and the switch represent the P1581 circuitry. Of the P1581 boxes, the one marked Test Gates includes all of the circuitry needed for test mode logical operation. The remaining box, labeled Mode Control, and switch represent the circuitry needed to switch device outputs between circuitry for the two modes.
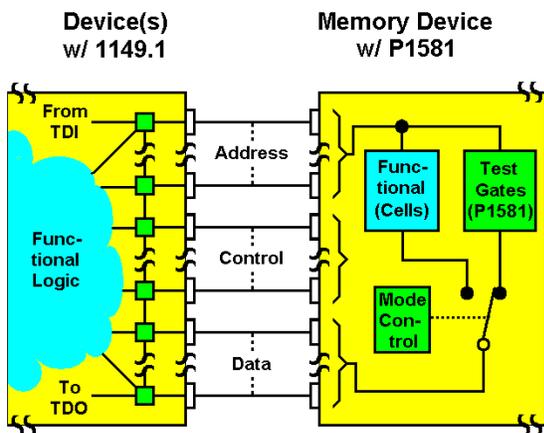

Figure 2. P1581 Test Concept

Note that connections to the mode control circuitry are not shown. These connections and the operating details of mode switching will be discussed in the next section. For the present, it will be assumed test mode and functional mode may be selected as needed.

The P1581 memory device on the right in figure 2 is shown connected to a single external boundary scan device on the left by address, data and control lines. In practice, the P1581 memory device may, if desired, be controlled by a group of boundary scan devices, an external tester, or special PCB test circuitry. That is, there is no requirement that other devices on the PCB contain boundary scan. Power connections have been omitted for clarity. No other connections are necessary.

The P1581 and 1149.1 concepts are similar in that the test mode circuitry in each case completely controls

device outputs in test mode. In P1581 test mode operation, address inputs to the memory device drive combinational logic which, in turn, drive device outputs. By proper design of the combinational P1581 test circuitry, then, a robust continuity test may be conducted on these connections. Test of control line connections not implicit in the test of the address and data lines may be achieved through means such as counters. Control lines not utilized for device control during test mode may be included as inputs to the P1581 test gating, in the same manner as address inputs.

P1581 Test Gates

An example of the simple circuitry needed to conduct continuity testing is shown in figure 3. Note that figure 3 shows the P1581 memory device of figure 2 as a smaller box, with details of the circuitry within the P1581 Test Gates section shown in detail above. In this example, P1581 test gate circuitry suitable for testing continuity of a memory device having 12 address and 4 data I/O lines is shown. Nine of the address inputs are connected to inputs of an XOR gate, the output of which is connected to one of the device data outputs through the switch shown. The remaining 3 address inputs are each connected to one of the 3 remaining device data outputs by other switch contacts omitted for drawing clarity. (Note that data I/O pins function only in output mode during P1581 test operations.)
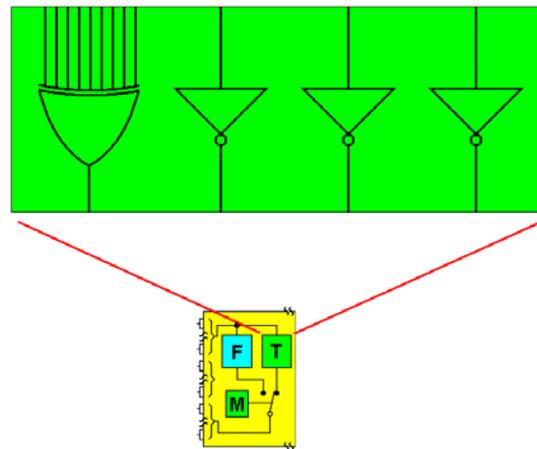

Figure 3. Continuity Test Logic
(IAX Type - 12 Address, 4 Data Bits)

The simplicity of the circuitry may be deceptive in that it can appear its use permits only a less than adequate test. In fact, the P1581 Working Group has determined this circuitry allows a very robust test

indeed. Furthermore, the simple P1581 gating circuitry is highly likely to permit automatic test generation by ATPG tools such as those provided with, or available for, boundary scan or in-circuit testers.

Any reader doubting the robustness afforded by the P1581 test gates shown in this example would probably do well to attempt to determine any short, open or stuck-at that could not be detected and diagnosed by a modest series of test patterns applied to the address inputs. Readers not convinced this simple means of test is sufficient are invited to contact the Working Group for clarification.

P1581 Test Gating Alternative

The test gating circuitry shown in figure 3 is an example of what has been designated as the IAX method, a method developed after formation of the Working Group. An example of the circuitry first explained by Philips Corp. in the International Test Conference papers preceding the Working Group is shown in figure 4. It has been designated the XOR method. No overall test benefit has been shown to exist by choosing either test gating method (XOR or IAX) over the other.
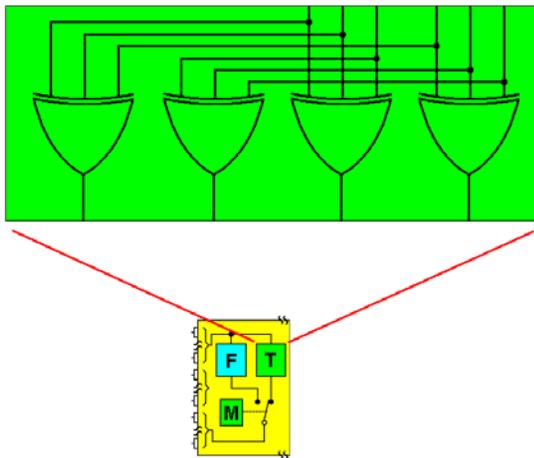

Figure 4. Continuity Test Logic
(XOR Type - 6 Address, 4 Data Bits)

Test Pattern Partitioning

Referring again to the example of figure 3, it is obvious that 4,096 different test patterns may be applied to the 12 address inputs. However, a robust continuity test may be conducted using only a small

subset of the 4,096 possibilities. In fact, a test consisting of (1) all ones, (2) all zeroes, (3) a "walking one" and (4) a "walking zero" would be the normal ATPG test generated by a sophisticated boundary scan software tool suite. Such a subset would consist of 26 patterns.

The 4,096 patterns possible with 12 address inputs consist of 2 where all inputs are logical one or zero, 24 (twice the number of address bits) where all inputs save one are logical one or zero, and 132 (twice the sum of the first n-1 numbers, where n is the number of address bits) where all inputs save two are logical one or zero. The remaining 3,938 (4,096 - 132 - 24 - 2), then, consist of at least 3 logical ones and at least 3 logical zeroes.

Figure 5 illustrates how test patterns that might otherwise be superfluous for continuity test may be readily decoded for other purposes. In the figure, test patterns having leading bit values of 1110000, 101010 and 010101 (a maximum of 160 different patterns) are used in controlling P1581 features beyond continuity test.

Figure 5. Test Pattern Partitioning

Device ID Option

Figure 6 shows a P1581 device having continuity test and device ID capabilities. Assuming the device to have 12 address inputs and 4 data outputs, the circuitry of the box labeled Gates (Continuity) in figure 6 would be the same as the IAX circuitry of figure 3. The box labeled Decoder in figure 6 would contain circuitry to detect a bit pattern of 1110000 on the leading 7 of the 12 device address inputs and, when detected, cause the circuitry of the box labeled Mux to switch such that the box labeled Device ID Reg controlled the 4 device data outputs.

Furthermore, the remaining 5 address inputs applied to the Device ID Reg box would be used in selecting among the 32 bits stored therein (the standard JEDEC format as used in 1149.1).
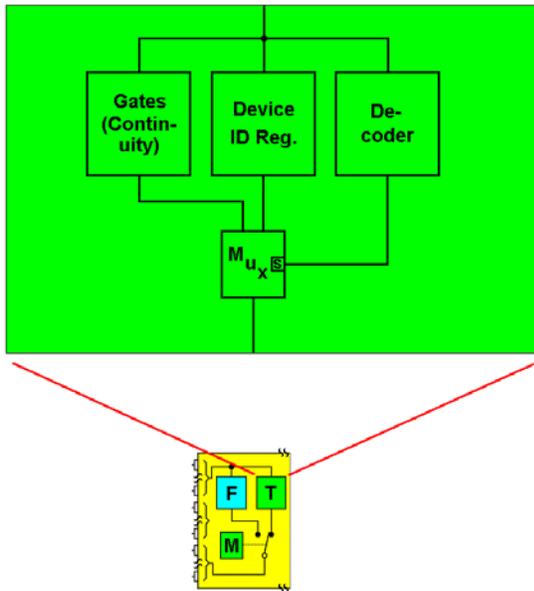

Figure 6. Device ID Option

Other Partitioning Options

Figure 7 illustrates how the concepts shown in figures 5 and 6 may be expanded to control other
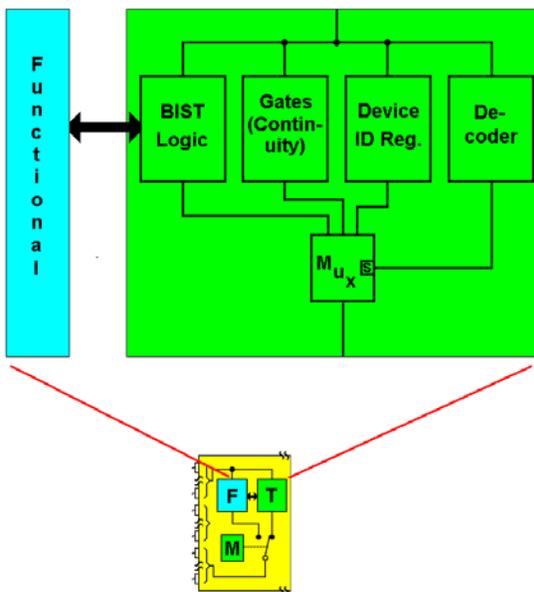

Figure 7. Device ID & BIST Options

features. BIST is shown as an example. In figure 7, a BIST capability of the functional logic (including the memory cells) has been added to the device ID and continuity features of figure 6.

As suggested in figure 5, optional features controlled by the test pattern partitioning method may be public (e.g., documented and available to device users) or private (e.g., documented and available only to the device supplier). An example of the former (in addition to BIST and Device ID) is control of self-repair circuitry which would effectively substitute other cells for ones found defective during pervious tests (BIST or otherwise). An example of the latter is controlling circuitry used to conduct margining tests in conjunction with device manufacture).

Test Mode Control

In discussing figure 2, operation of the box labeled Mode Control was deferred. It will now be explained.

Seven mechanisms for entering test mode are available for device designers to choose between. They are summarized in Table 1.

NFS - Non-Functional Stimulus

P1581 circuitry within the memory device is designed to monitor predetermined inputs for activity that could occur only in PCB test operation, but never in PCB functional operation. An example is shown in figure 8.

In this example, the PCB incorporates boundary scan devices. The memory device shown has been designed to monitor inputs WE* and CS* to be simultaneously active (logical zero) for a period of 100 milliseconds or longer. Combined active pulses of that duration would occur only when the PCB was being tested with boundary scan stimulus, but never during functional operations. Thus, test mode is entered when the long combined pulse condition occurs on those two inputs. As shown in the figure, the boundary scan stimulus is provided external to the memory device, from the Control Device on the left.

Test Mode Entry & Exit Methods		
Acronym	Method	Description of Test Mode Control
Independent of Time After Power up		
NFS	Non-Functional Stimulus	Device inputs driven by stimulus not possible in functional operation, but easily accomplished during board test operations (e.g., boundary scan, ICT, board level BIST).
CKF	Clock Frequency	Device clock input frequency altered (e.g., static) by board level control of the clock driver device.
CDE	Code Selection	Device codes not required for functional operation (e.g., read, write) are assigned to test mode control.
ANL	Analog Level	One or more device inputs are driven to a non-logical level for a duration not possible during functional operation.
TPN	Testpin	A dedicated device input is used for test mode control.
Initial Dependence on Power up Timing		
PST	Power up Selection	A short delay after power up certain device inputs are monitored for presence of states that would be avoided through customary board design (e.g., write and chip select both active). Various exit means.
PDT	Power up Default	Test mode occurs at power up. Exit occurs at beginning of first write unless other exit means chosen.

Table 1. Summary of Test Mode Entry/Exit Methods.
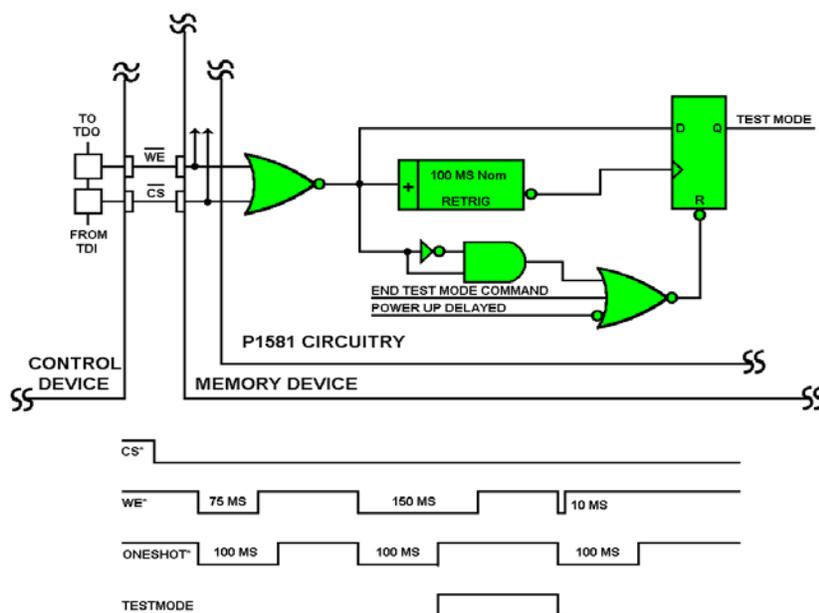
Test Mode Control from Existing PCB BScan Circuitry
(No additional DFT)

Figure 8. NFS Test Entry/Exit

Operation is as follows. When power is applied to the device, an internal circuit holds the line labeled POWER UP DELAYED at a logic zero until the device is capable of proper operation. Thus, the compound OR/NOR gate shown will apply a logical zero at the reset input of the flip flop, assuring test mode is inactive directly after device power up. If a boundary scan test is not conducted, any pulses applied to the one shot will be of a duration less than 100 milliseconds. Therefore, a logical zero will be clocked into the flip flop whenever one shot timeout occurs. If a combined pulse of greater than 100 milliseconds is applied at the WE* and CS* inputs, timeout of the one shot will result in a logical one being clocked into the flip flop, invoking test mode. Test mode is reset by applying a WE*/CS* pulse of any duration to the AND/INVERTER circuit, with the exception of certain glitches. Test mode may also be terminated by means of a predetermined test pattern applied to address inputs of the memory device in a combination not used for continuity checking.

The P1581 logic designer may, alternatively, choose other non-functional stimulus. For example, it has been suggested changes to address input values during WE* activity could be used to invoke test mode, as such changes would never occur in normal PCB functional operation.

A primary advantage of the NFS method is that it requires no PCB support circuitry in PCBs already incorporating boundary scan.

CKF - Clock Frequency

In the case of memory devices having a free running clock input, the memory device could be designed such that test mode was invoked whenever the clock was running at a frequency not used during device functional operation - for example, a static level. The clock generation device would be designed to allow frequency control by internal boundary scan circuitry or by an external input.

An advantage of the CKF method is its simplicity. A possible disadvantage is that it depends on the availability of a device which may not be available

for purchase when the memory device is introduced to the market.

CDE - Code Selection

In memory devices where operations (e.g., read, write) are controlled by a code applied to a group of inputs, the device may be designed such that one otherwise unused code, when the device is in functional mode, causes the device to enter test mode. Once test mode has been established, codes having one purpose in functional mode may be re-used for another purpose in controlling test mode functions. In many cases, then, the availability of a single "spare" functional code will allow test mode control by a plurality of codes without the need of providing additional device connections.

ANL - Analog Level

Figure 9 illustrates how an analog level may be used to control test mode. To apply the level, the
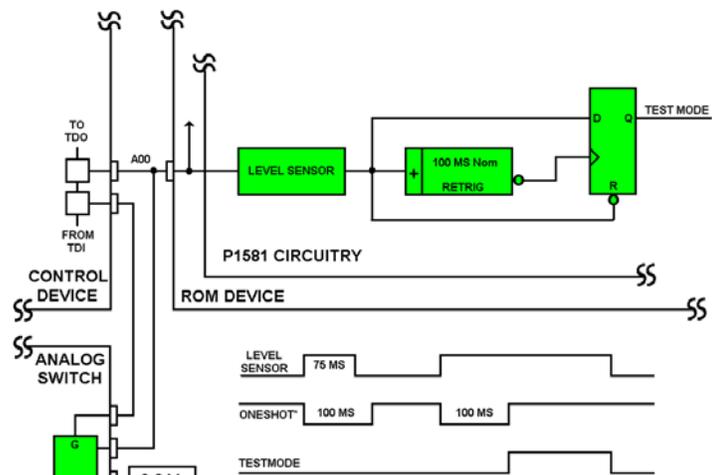

Figure 9. ANL Test Mode Entry/Exit

boundary scan cell of the control device pin connected to the memory device input pin being monitored for a non-logical level is set to high impedance by boundary scan commands. Other commands would then cause the normally open analog switch to close, thus applying the analog level to the memory device pin which is monitored for that level, causing the device to enter test mode after 100 milliseconds has elapsed. Note that the test circuitry

of figure 9 causes an exit from test mode as soon as the analog level is switched off.

This circuit uses the only one of the seven test mode entry/exit methods that will work with a memory device having only address and data pins (i.e., certain ROMs). Its disadvantage, of course, is the need to provide an analog level and an analog switch as part of the PCB design, both of which might otherwise be unnecessary.

TPN - Testpin

A dedicated device connection is used to control test mode entry and exit. One input state causes the device to be in functional mode. Applying the opposite state causes the device to be in functional mode.

This method offers simple operation, but the dedicated connection may be deemed objectionable.

PDT - Power up Default Test

Intended exclusively for use with volatile RAMs, the memory device is designed to enter test mode a short delay - nominally 10 milliseconds - after power up. At the beginning of the first device write operation, test mode ends and the write continues through to its normal completion. Thus, test mode is generally limited to the period where the device outputs would be driven by memory cells in an unknown (X) state. Instead, the device outputs are driven by the P1581 test logic.

An advantage of this method is that it exits test mode on its own when the PCB circuitry causes the first write to begin. Test mode may be extended or re-established by circuitry controlled by non-continuity test patterns applied to the device address inputs according to the test pattern partitioning method previously described.

This method, and the PST method discussed below, have the disadvantage of requiring the PCB test circuitry external to the device to assume a known state very shortly after power up. This may be difficult to achieve using the boundary scan tools in existence at the time the P1581 proposal was formulated.

PST - Power up Selectable Test

In the PST method, the memory device may be caused to enter test mode directly after power up by circuitry which forces certain inputs to a predetermined state (e.g., the WE* input held active). Like the PDT method, the PST method requires that the PCB or the boundary scan system be capable of controlling one or more P1581 device input pins very shortly after power up. Unlike the PDT method, however, the PST method is applicable to both volatile and non-volatile memory devices.

P1581 Description Language

TBD.

The language will describe the test features of the device in a format suitable for both manual interpretation and ATPG operations.

Goal - IEEE 1581 in 2007

P1581 has been a long time in the making. This is because the Working Group wasn't comfortable that the methodology proposed at the outset answered the needs of device manufacturers, users interested in 1149.1 or P1581 test features, users interested in only functional test and not 1149.1 or P1581 features, and test tool vendors, both hardware and software.

The descriptions in the previous sections of this paper serve as proof that P1581 has reached a state where all the conceptual problems have now been solved. The P1581 solution is workable in any memory device case where 1149.1 is workable and is a better fit in cases where 1149.1 is deemed impractical because of additional test connection requirements. All that remains is to tailor the P1581 overall solution described herein to work most effectively for both suppliers and users. It's time to move forward and finalize a standard that as many participants as possible find satisfactory.

Ensuring Benefit to Your Business

Anyone whose business involves memory devices stands to gain if IEEE 1581 (P1581 until after balloting is complete, assuming adoption) best meets their needs and gain less if it doesn't. This follows regardless of their sector of interest.

(1) Device manufacturers need to ensure that 1581 satisfies all their customers so that they need offer

only one series of devices. They also need to ensure such features as Device ID and Private Options are implemented in such a way as to be most beneficial in their manufacturing operations.

(2) Many users have been waiting years for 1149.1 or 1581 to be included in the memory products they use to increase test reliability (not subject to timing vagaries). They need to ensure, first, that 1581 becomes a reality, and, second, that important features, such as Device ID, do not fall by the wayside.

(3) Users who have no interest in test methods such as P1581 and 1149.1 need to ensure 1581 includes the features described above which allow compatible operation in both 1581 and non-1581 PCB environments. Of particular importance is the savings realized from reducing the number of pins dedicated for test from up to 5 down to zero.

(4) Test hardware and software vendors need to ensure IEEE 1581 is compatible with their products and not just with the offerings of others.

Anyone involved in the industry is invited to advise the P1581 Working Group of their ideas or concerns or, even better, participate in Working Group teleconference meetings, usually held monthly. Voting membership in the Working Group is open to anyone attending a minimal number of such meetings. For further information, please reference the P1581 website:

http://grouper.ieee.org/groups/1581/