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Recent developments on DAC modelling, testing and standardization

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Abstract

In the last years the technology improvements of Digital-to-Analog Converters (DACs) has extended the use of digital techniques in a multitude of applications. Consequently, there is an increasing attention to DAC topics, from researchers and manufacturers. The paper is aimed at providing a metrological overview and the leading trends of the research in the field of DACs.
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1. Introduction

Digital computing power has exponentially increased at ever smaller incremental costs. As a consequence, many applications formerly performed with analogue circuitry have found a new lease-on-life in this digital realm. Hot application areas include compact disc players, telecommunications, computer sound cards, digital instrumentation, computer graphic adapters [1].

However, the real world is still and will always be an analog place. To bring digital processing and its benefits on real-world applications, the analog signal must be translated into a format that a digital computer can utilize. This is the function of the Analog-to-Digital Converter (ADC). After processing by a digital computer or Digital Signal Processor (DSP), the resulting digital stream of information must be returned to its analogue form by a Digital-to-Analog Converter (DAC). Once analog again, the information can be "consumed" by the human senses, most often sight or hearing.

ADCs and DACs are the bottleneck from the analogue world to the digital one, and vice versa, respectively. Therefore, particular attention has to be paid to these components both from the design point of view and from the metrological characterisation point of view. Papers, conferences, standards are mainly oriented to the analysis of the ADCs. The metrological characterization of the DACs seems less investigated.

These components are crucial in emerging applications such as telecommunications, where the

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DAC puts the information on the channel and a wide frequency band and high resolution are required to satisfy the need for high speed and high accuracy. For these reasons, DACs are receiving an increasing attention, as testified by the growing amount of scientific contribution in this field. Moreover, the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society is working on a new project to produce a standard focused on DACs [2]. Since most of the scientific literature concerning DAC modelling and testing is architecture-dependent, the first section of the paper reports some developments on DAC architectures. In the following sections a metrological overview of DAC topics is proposed by referring to: (i) DAC modelling, (ii) DAC testing, and (iii) DAC standardization.

2. DAC architecture

This section focuses on the new developments and the leading trends of high-performance DACs.

For the majority of communication circuits, the most commonly used high-speed DACs are based on current-steering architecture. Typically, an N-bit current-steering DAC is designed using a segmented structure in which input bits are divided into two groups with B less significant bits switching binary coded current sources and (N–B) most significant bits switching thermometer coded unary current sources (Fig. 1). A layout-dependent switching sequence that minimizes the systematic errors of such architecture is presented in [3]. Using the results in [4] as a basis, a new cost-oriented approach to optimize the design area is developed. The optimum design can be obtained by reducing the area of the current source transistors. The corresponding DAC could feature a smaller size in comparison to equivalent subsystems reported in the literature.

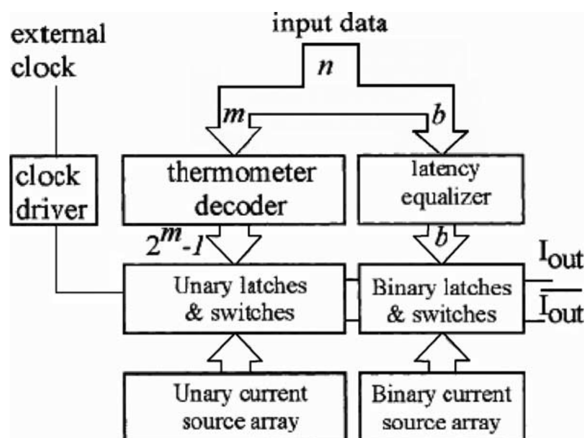

Fig. 1. Current-steering DAC architecture [14].

In order to achieve high linearity and Spurious Free Dynamic Range (SFDR), a large degree of segmentation has been used in [5] for a 12-bit 320-MSample/s current-steering D/A converter in 0.18-μm CMOS, with the seven most significant bits (MSBs) being implemented as equally weighted current sources. A "design-for-layout" approach has allowed limiting the device area to just 0.44 mm^2. The increased switching noise associated with a high degree of segmentation has been reduced by a new latch architecture.

For obtaining high-accuracy DACs the oversampling architectures, such as the Σ–Δ loops (Fig. 2), are usually preferred. In particular, stability analysis of high-order Σ–Δ loops is still a challenge for researchers. In [6] stable high-order error-feedback Σ–Δ DACs were designed based on a sufficient stability criterion. This analytical criterion asserts that an error-feedback modulator with Lth-order FIR noise transfer function and $L+1$ bits is stable. Such error-feedback DACs are robust and achieve better performance than output-feedback architectures. Due to aggressive noise shaping and multibit truncation, simulations show that these DACs can achieve high resolution even for low oversampling ratios.

An oversampling bandpass DAC has been proposed in [7] to eliminate the carrier leak and in-band SNR degradation that accompany I and Q channel mismatch in wireless transmitters. The converter combines a cascaded noise-shaping Σ–Δ modulator with digital FIR and mixed-signal semi-digital filters that attenuate out-of-band quantization noise. In Fig. 3 a functional diagram of the proposed bandpass D/A converter is shown. The digital baseband I and Q signals are first upsampled and then fed into oversampled low-pass noise-shaping modulators. The outputs from the digital noise shapers are mixed to IF in the digital domain and then converted into analog signals using a bandpass D/A converter with integrated filtering. The I and Q

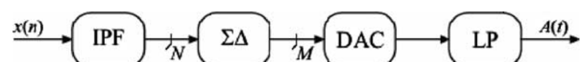

Fig. 2. Oversampling DAC architecture.

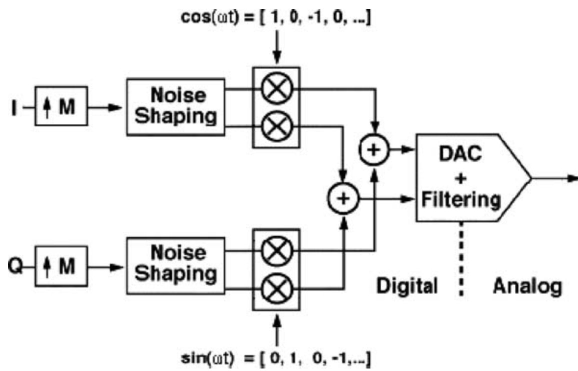

Fig. 3. DAC architecture proposed in [7].

signals are combined immediately prior to the D/A interface. The performance of the converter in presence of current source mismatch has been improved through the use of bandpass data weighted averaging.

The latest development in the DAC architecture design, aiming to achieve extremely high update rates, involve optics. A photonic implementation of DAC is proposed in [8] using electrooptic polymer modulators. There are many advantages of using photonic technology to implement D/A conversion, such as high-speed clocking and sampling, wide-bandwidth, lightweight components, and reduced interference. A 2-bit implementation at low frequencies is experimentally demonstrated at a conversion rate of 80 MS/s which is limited by the bandwidth of the photodetector and its associated electronics.

3. DAC modelling

The rapid diffusion of emerging high-performance standards for communication, measurement and entertainment purposes requires DACs with higher speed and accuracy so their design and testing become more challenging [9]. For this reason, DAC modelling research is almost always oriented to help designers to obtain converters having the best performance in terms of speed and accuracy.

Two DAC modelling techniques based on principles of wavelet theory are described in [10]. Macro modelling that uses passive components and adders and mathematical equations to depict the wavelet basis functions are proposed. The basis functions are identified by analysing the DAC output signal in the time and in the frequency domain. The proposed basic block diagram for DAC modelling consists of: (i) a glitch generator, (ii) a damped sine wave generator, (iii) an exponential function generator, and (iv) an adder (Fig. 4).

Architecture-based modelling follows the above quoted trends in DAC design, focusing on current steering or Σ–Δ converters.

Concerning current-steering DACs, several papers have proposed various models of the Integral NonLinearity (INL) as a function of the variance of the current source mismatch. However, most of these methods neither describe accurately the statistical behaviour of the INL and Differential NonLinearity (DNL) nor do they take into account the effects of the segmentation on the INL and DNL. In [11] it has been demonstrated that the segmentation of the current sources affects the statistical behaviour of the INL and DNL. Moreover, regression models for the DNL and INL are presented providing to evaluate the matching requirements of the current source of the current-steering DAC as a function of the segmentation ratio. It has been also demonstrated that with more than two segmented bits, the INL is the limiting factor [11].

For current-steering DACs, the delay difference among the current sources is one of the most important nonlinearity errors. In [12] a mathematical model that explains the impact of delay differences on the SFDR of a thermometric DAC is proposed. This theoretical analysis shows that the delay differences among the current sources limit the DAC SFDR even when the signal frequency is very low. According to this result it is suggested to the designers to reduce the delay differences or find out some optimized delay distribution in order to improve DAC performance.

In the past, dynamic element matching techniques were presented to tackle static mismatch of current-steering DACs. However, little attention was directed to dynamic errors. In [13] several implementations to tackle with dynamic errors while avoiding performance degradation due to static error sources are presented. Dynamic errors in current-steering DACs are analysed through a dynamic error model to show that they contribute to nonlinearity in a different way as static mismatch errors.

The paper [14] is aimed at making easy the automation of the circuit design of future current-steering DACs. Fig. 5 shows the two most usual topologies for the current source cell circuit. The basic circuit includes the Current Source (CS) transistor and two complementary switch transistors (SW and $\overline{\text{SW}}$), as shown in Fig. 5a. Some cases

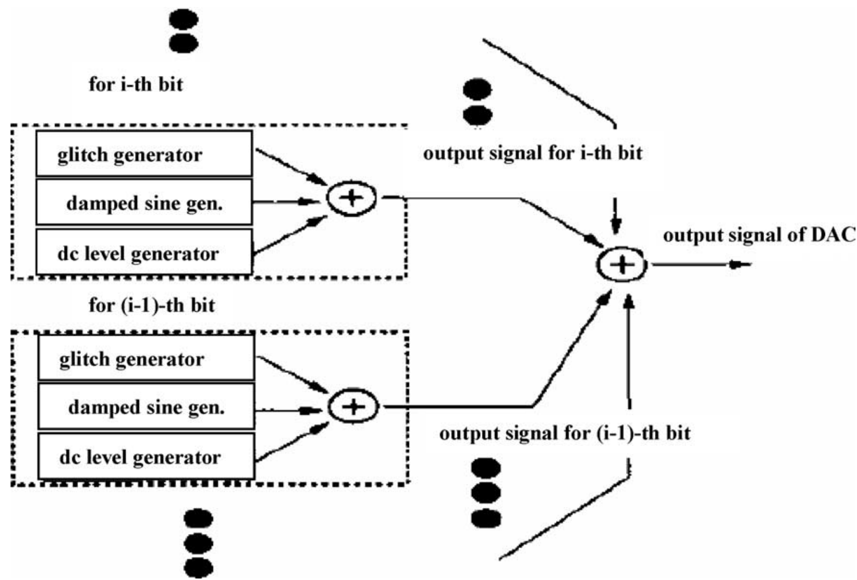

Fig. 4. Block diagram for DAC model [10].

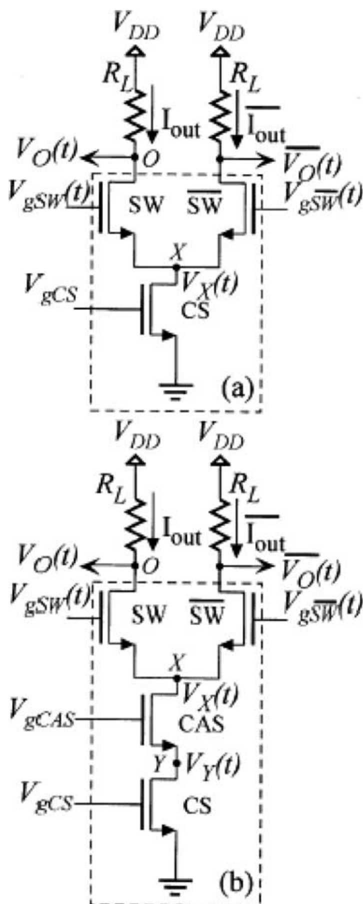

Fig. 5. Current source cell topologies: (a) basic; (b) cascoded [14].

require an additional CAScode (CAS) transistor in series with the CS transistor to increase the cell output impedance and improve node isolation, as shown in Fig. 5b. These two current source cell topologies, namely a simple cell and a cascoded cell, are considered in [14] to obtain the relation between the transistor design parameters and the static and dynamic models. On one hand, a mismatch statistical analysis is applied to all the transistors of the current source circuit. This allows the definition of design expressions relating the circuit parameters to the DAC specifications without the need of arbitrary design margins or Monte Carlo simulations. On the other hand, an improved analysis of the current source switching characteristics provides a more realistic modelling of the relation between transistors sizes and output current settling time. By including these two improved models into the usual design procedure, circuit sizing for optimum settling time and proper static behaviour can be obtained analytically, leading to smaller current source area, and, hence, to an overall DAC area reduction.

A segmented DAC structure based on recursive decomposition is proposed in [15]. An N-bit binary DAC is split into two $(N-1)$-bit DACs and one 1-bit DAC. A DAC model that includes matching errors has been simulated to develop optimal segmentation.

The effect of nonlinearities on DAC resolution is studied in [16]. Two models, an exponential and a

sinusoidal approach, are proposed to estimate the drop in SIgnal to Noise And Distortion ratio (SINAD). These models were used to study the performance loss of a multibit DAC when used in frequency synthesizer architecture. From the results obtained in [16], it follows that the amplitude errors should not be neglected for DACs that have less than 8-bit resolution as they degrade considerably the accuracy of the synthesizer output. However, using at least 8 bits implies larger die area and higher circuit complexity, as the use of compensation techniques might be required. Authors suggest the choice of a 1-bit Σ–Δ architecture for the DAC to be used in a synthesizer because its transfer function is inherently linear and the converter resolution can be adapted by changing operating frequency and a single voltage reference.

4. DAC testing

Due to the exponential growth in DAC internal complexity there is a major increment in testing time and in the equipment cost [17]. In order to reduce the time necessary to carry out the static testing of a given N-bit DAC, parameters such as offset error, gain error, INL and DNL should be estimated by measuring the analog outputs corresponding only to a suitable subset of the 2^N possible input codes. These subsets are usually referred to as test vectors. This approach is increasingly convenient as the converter nominal resolution grows and it becomes particularly valuable when high volumes of production are considered. However, a reduction in the number of input test vectors requires the definition of appropriate mathematical models able of describing the influence of each elementary part of a given DAC architecture on its actual output voltages [18–20]. Once this data is known, the static testing efficiency can be improved by selecting only the input codes that enable the estimation of the most significant errors of the DAC. Interesting methods have been proposed to minimize the number of input codes aimed at testing both specific device families [21] and basic DAC schemes [22–24]. The interweaving of functional and parametric tests using the Linear Error-Mechanism Model Algorithm (LEMMA) test-point selection strategy proposed in [25] is described in [26]. The information required is the simulated behaviour of the DAC with a defect. In particular, by selecting test-points that serve the parameter estimation of the LEMMA-model for the device under test, and at the same time cover hard-faults, it is possible to have a means of combining functional and specification tests. In [26] authors show that this leads in the particular case of the DAC AD5320 to a cut in the number of test-points from 124 to 66.

A more general approach is proposed and justified in [9]. This approach is based on a high-level model that takes advantage of the basic structural features common to the most of high-performance DACs, thus enabling a major reduction in the total number of input test vectors. The parametric DAC block diagram considered in [9] is shown in Fig. 6. Such a scheme is absolutely general, i.e. independent of low-level structural or technological details, and consists of $M \leqslant N$ sections of N_m bits each, so that $\sum_{m=1}^{M} N_m = N$. The bits belonging to the B least significant slices control binary-weighted voltage or current sources (e.g. an R–2R ladder), whereas the M–B most significant sections are thermometer-encoded (e.g. they drive an array of unit current sources).

The efficiency improvement resulting from this procedure not only decreases the overall testing time, but it also promotes the design of both inexpensive Built-In Self-Test (BIST) architectures and digital self-calibration schemes.

BIST is a part of any complex System on Chip (SoC) design. The DAC is one of the most commonly used mixed signal block in a SoC. It requires both static and dynamic tests [27]. BIST schemes for testing static parameters, including the gain and offset errors, DNL and INL, follow three approaches. In the first approach, suggested in [28], tests are performed to check if any of the errors exceed the ± 0.5 LSB bounds. This scheme uses multiple voltage references and a precision gain amplifier (Fig. 7). When DTest input becomes active, the control logic begins the test procedure and directs the operation of the counter, DAC, analog switches and multiplexers, and observes the output of the comparator. This BIST structure tests the offset voltage, DNL error at all 2^N input codes, gain, and INL error at some critical points. The measured parameters are evaluated by the programmable window comparator. K is the gain of the error amplifier (EA) that has very high-input impedance.

In an attempt to reduce the number of required reference voltages, in [29] a variable gain amplifier is introduced to amplify different codes to the same level and then compare it with a single reference. The second approach uses the DAC in a feedback loop. In the scheme proposed in [30], the input to

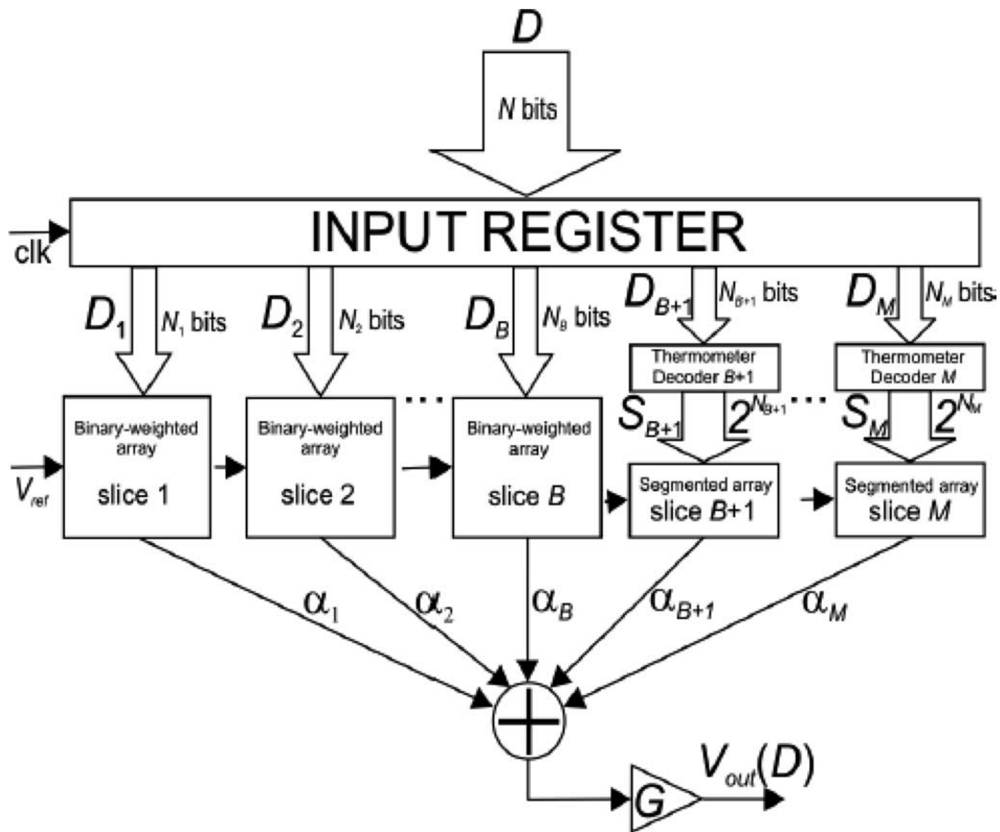

Fig. 6. General block diagram showing the structure of high-accuracy DACs based on the combination of binary-weighted and thermometer-encoded sections [9].

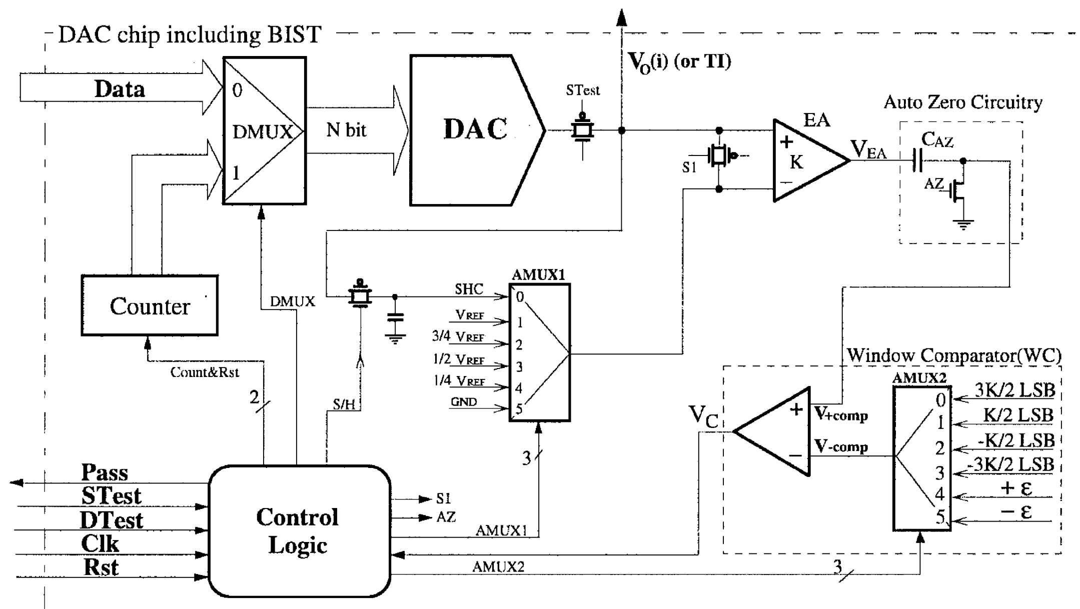

Fig. 7. The architecture of the fast BIST approach for D/A converter testing. TI (Test Input), DTest (Device Test), STest (Self Test) [28].

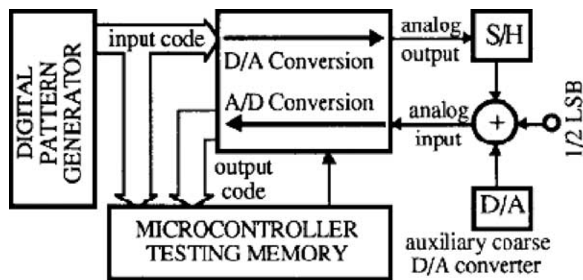

Fig. 8. Architecture of the data conversion system with self-testing capability [31].

the DAC in the feedback path of a Σ–Δ modulator is switched between two codes with opposite signs. Static errors are inferred from the average value of the output, measured using an up/down counter. In [31] a scheme is proposed where the output of the DAC used in a successive approximation ADC is first sampled. This is converted back to a digital code by reconfiguring the system as an ADC (Fig. 8). The difference between the two codes is a measure of the static errors in the DAC. In particular, an input digital code is initially applied to the system configured as a DAC and the resulting analog voltage is sampled by an auxiliary sample and hold circuit. Then, the system is reconfigured as an ADC and the sampled analog voltage is reconverted to an output digital code which ideally should be equal to the digital code applied at the input. Due to the capacitance mismatches and offsets occuring in the system, a nonzero difference error code may be detected by subtraction of the two digital codes. In order to prevent that, the errors on the A/D conversion cycle compensate those on the D/A conversion cycle. In order to compensate for the offset voltage that may result from the operations of D/A conversion, sample and hold and A/D conversion, an auxiliary DAC with coarse resolution is also included in the system. When the input digital code is zero, such DAC can generate an appropriate compensation voltage which added to the converted analog voltage, yields a zero error code.

In the third approach, a high-frequency clock is used and static parameters are measured in terms of the number of clock cycles. In the scheme proposed in [32], the time taken by a linear ramp to cross two consecutive output levels is considered a measure of the corresponding step. In [33] the DAC output voltage is used to control a Voltage Controlled Oscillator (VCO) and to obtain errors in terms of the frequency shift. Accurate on-chip voltage or current references are difficult to get. A relatively more accurate time reference can be obtained from an external crystal oscillator. This is the solution adopted in [33]. However, they require a VCO with linearity better than the DAC one over the entire output range. This is difficult to achieve.

In [34], a modification of such scheme, which reduces the linearity requirements of the VCO is proposed. The tests are based on estimating the voltage step corresponding to adjacent codes. This is done using an on-chip offset-compensated sample-and-subtract module and a VCO. An up-down counter is used to measure the frequency and the reference clock is used to set the counting window. The differential DAC output is connected to the sample-and-subtract module through switches. Computation of DNL is made from the estimated step size. Then, the computation of INL is made from DNL.

5. DAC standardization

Due to their numerous features and wide range of application uses, it is very difficult to define a unique way in which DACs can be specified and tested. For this reason it is growing the need for DAC standardization. At the present time the existing main DAC standards are: (i) IEC 60748-4, which include only DAC static specifications and test methods [35]; (ii) IEEE Std. 746 which addresses the testing of Analog-to-Digital and Digital-to-Analog converters, used for PCM television video signal processing [36], (iii) JEDEC Std. 99, addendum number 1, which deals with the terms and definitions used to describe Analog-to-Digital and Digital-to-Analog converters and does not include test methods [37], and (vi) EBU Technical Information I15-1998 [38] which reports ADC and DAC performance parameters for testing in conformity with ITU-R Recommendations BT.601 and BT.656. However, it does not exist a standard focusing specifically on terms, definitions and test methods for DACs for a wide range of applications as already done for ADCs [39]. In order to fill this lack the Waveform Measurement and Analysis Technical Committee (TC-10) of the IEEE Instrumentation and Measurement Society is working to realize a standard to provide common terminology and test methods for the testing and evaluation of DACs. The information in this standard will be useful both to manufacturers and users of DACs because it will

provide a basis for evaluating and comparing existing devices, as well as providing a template for writing specifications for the procurement of new ones. Moreover, in some applications, the information provided by the tests described in this new standard could be used to correct DAC errors.

6. Conclusions

DAC topics are becoming a very attractive research field as testified by the increasing amount of scientific contributions. In the paper a metrological overview of DACs has been presented involving DAC modelling, testing and standardization. In order to help young researchers interested in DACs to orientate themselves in this field.

Due to the rising amount of activities in this field and the their fast evolution in the time, the authors beg readers pardon in advance for all the omissions surely present in this paper, mainly due to time and space limits.

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