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Standardized Access to Embedded Test and Debug Instruments IEEE P1687 – The Next Step

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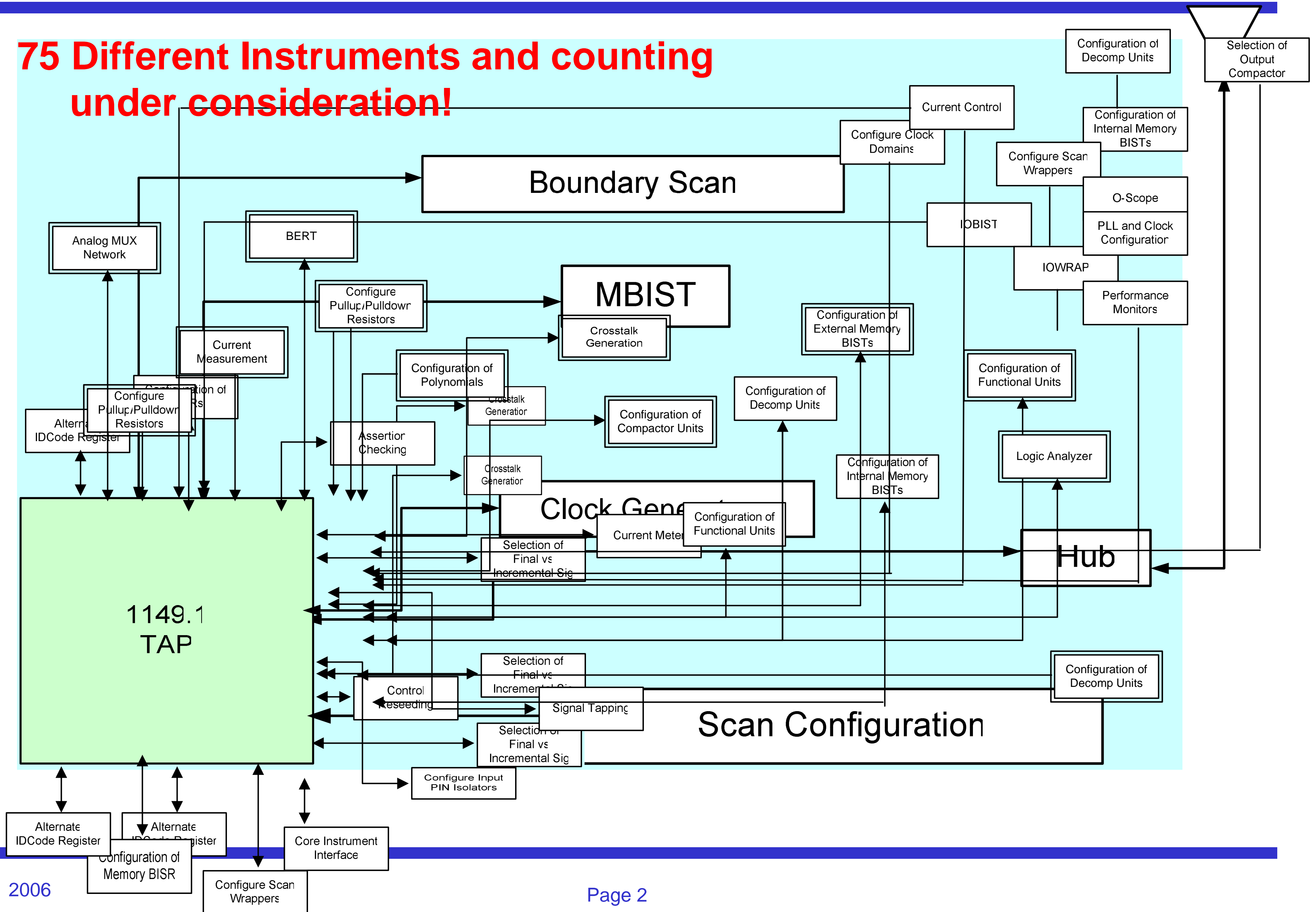
IJTAG (IEEE P1687)



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IJTAG (IEEE P1687) – Instruments under consideration

- Alternate IDCode Register
- Analog Mux Network
- Assertion Checking
- BERT
- Clock Divider and Chop Control
- Clock Mode Control for Delay Test
- Clock Tree Gating
- Configuration of Compactor Units
- Configuration of Decomp Units
- Configuration of external Memory BISTs
- Configuration of Functional Units
- Configuration of internal Memory BISTs
- Configuration of Memory BISR
- Configuration of MISRs
- Configuration of Polynomials
- Configuration of STUMPS Channels
- Configure Clock Domains
- Configure Input Pin Isolators
- Configure Pullup/Pulldown Resistors
- Configuring Scan Wrappers
- Control of ReSeeding
- Core Instrument Interface
- crosstalk generation
- Current Control
- Current Measurement
- Current Meter
- Data Analyzer
- Digital Mux Network
- Enabling Breakpoint/Cycle Counters
- Enabling Compactor Diagnosis
- Enabling Comparators
- Enabling DMA
- Enabling Scan Mode Configurations
- Enabling Scan Safety Logic
- Enabling Scan Wrappers (TAMs)
- Enabling Single-Step Operation
- Enabling/Configuring Data Collection
- Enabling/Configuring X-Masking
- Generic
- IBIST
- Inter-domain Synchronizers
- IO Parametric Adjustment
- IOBIST
- IOWRAP
- Logic Analyzer
- O-Scope
- Performance Monitors
- PLL and clock configuration
- Power Control
- PRBS
- Scanning in of Compare Signature
- Security
- Selecting Trace Buffers/Watch Buffers
- Selecting/Configuring Triggers
- Selection of a Scan Mode
- Selection of DeCompression Units
- Selection of Final vs Incremental Sig
- Selection of Functional Units
- Selection of Logic BIST Units
- Selection of Memory BISR
- Selection of Memory BIST Units
- Selection of Output Compactor Units
- Signal Tapping
- Single Step
- SSO
- State Dump
- Supplying Match Values
- Temperature Measurement
- Test Executive
- Test Scheduling of Memory BISTs
- Voltage Control
- Voltage Measurement
- Voltage Meter
- Waveform Analysis
- Waveform Generator

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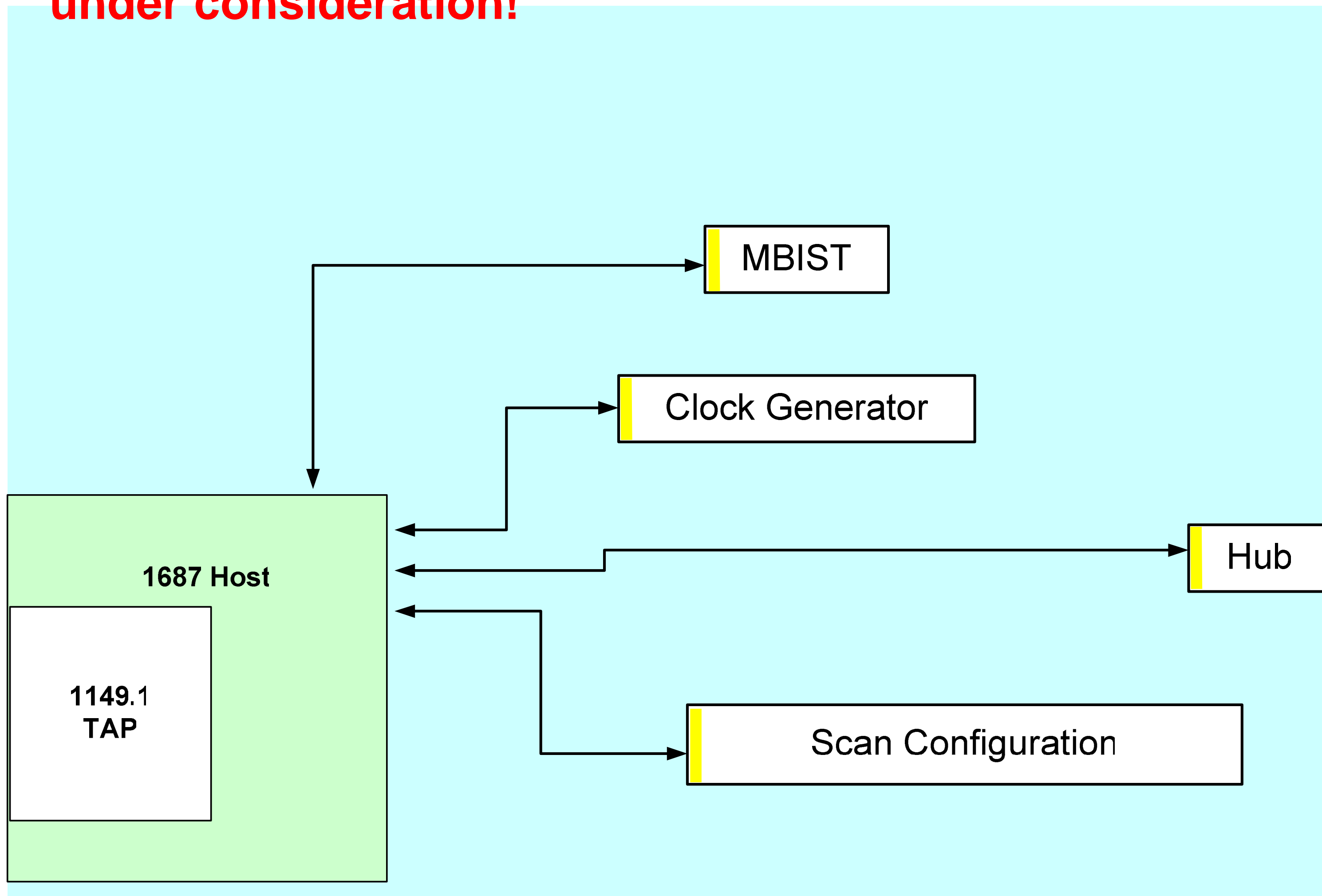
IJTAG (IEEE P1687)

75 Different Instruments and counting under consideration!



IJTAG (IEEE P1687)

- These instruments are needed for testing, debugging, yield improvement
  - IP companies do not want to be
    - Devoting huge resources to generic test structures
    - Writing programs to enable these test structures
    - Having to redesign the wheel
    - Debugging test structure that can be bought off the shelf

IJTAG (IEEE P1687)

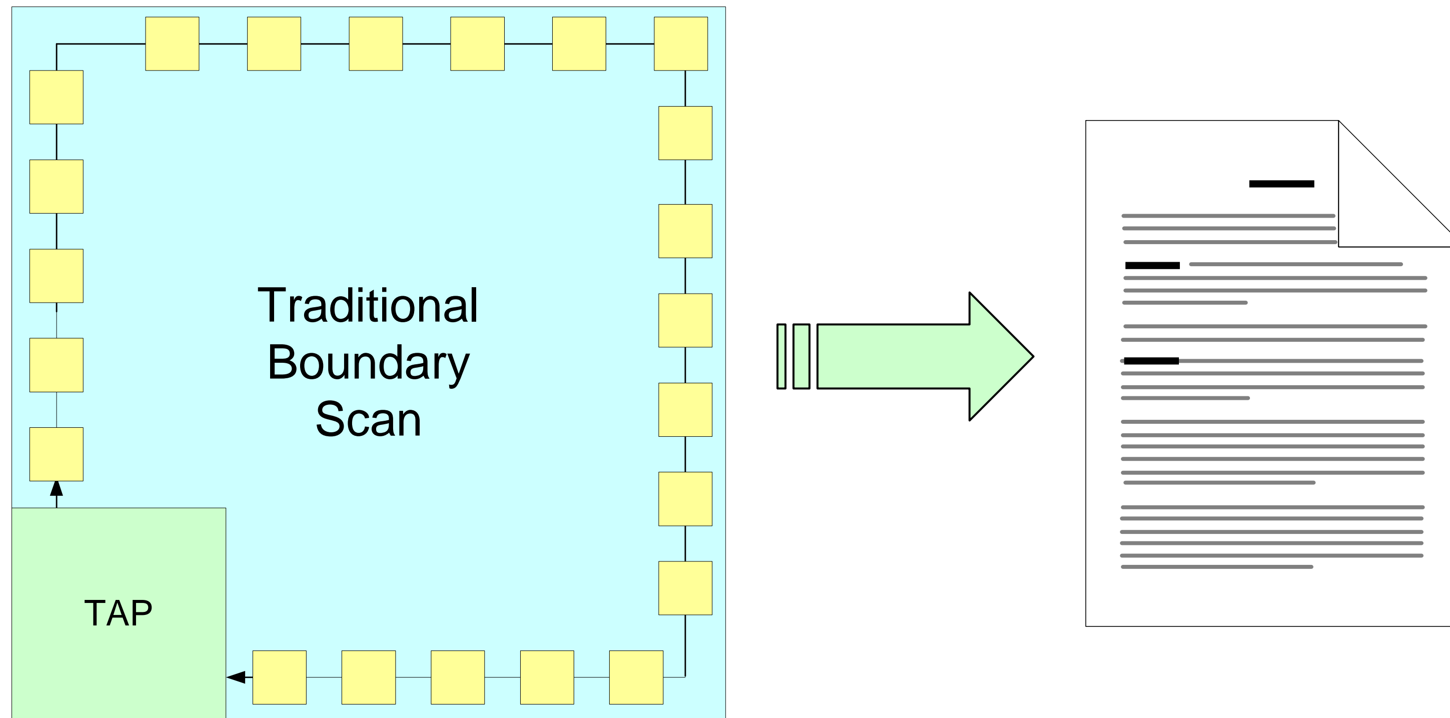
- Common, standardized internal test structures
  - Cost less to implement
  - Are less risky on 1st Silicon
  - Enable debugging tests
  - Result in better quality products
  - Enable faster yield learning
    - Result in even better quality products
  - Result in more defect-free systems
    - Create happier customers

IJTAG (IEEE P1687)

- IEEE P1687 is the draft standard for access and control of instrumentation embedded within a semiconductor device
- It provides a standardized process that allows test systems to communicate with embedded instruments

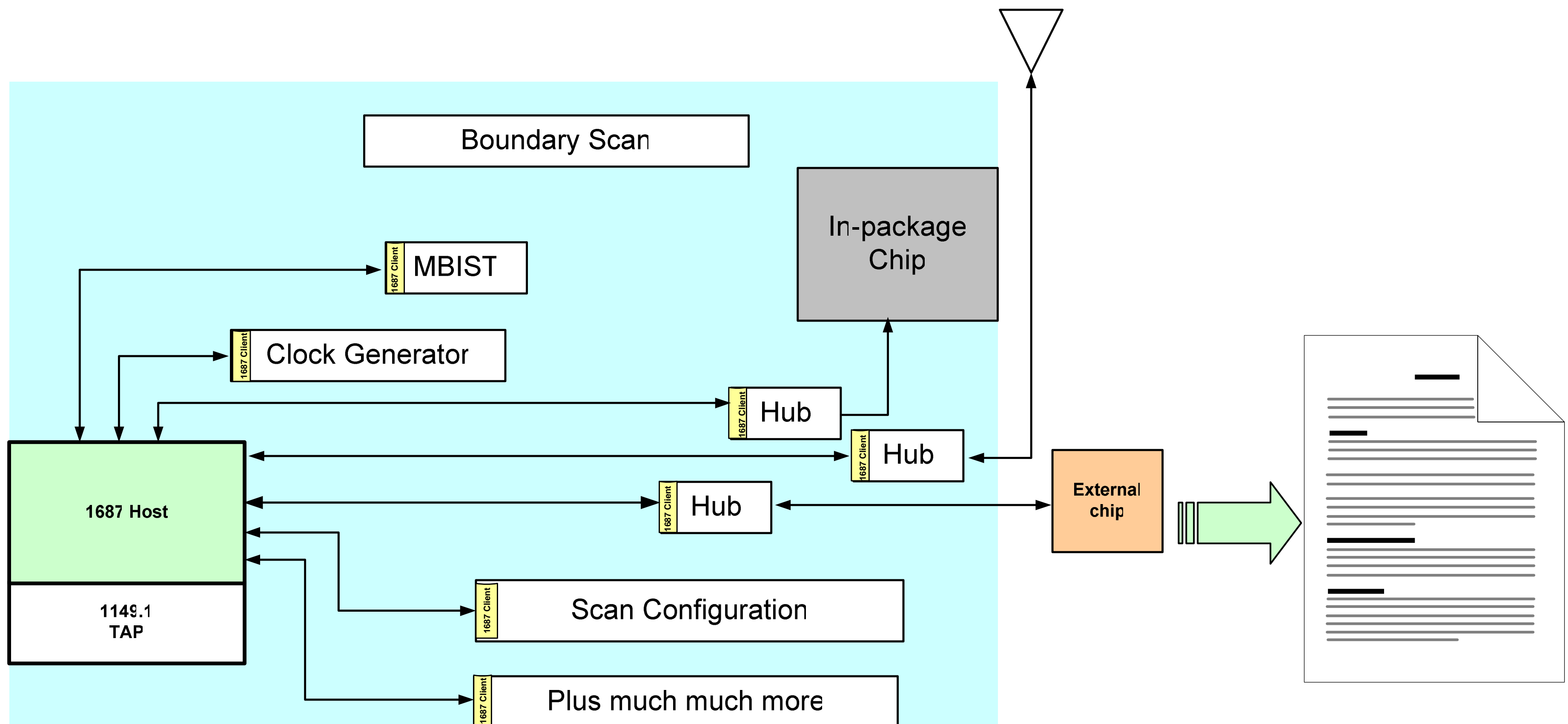
JTAG defined Boundary Scan

- IEEE 1149.1 (JTAG) defines BSDL.
  BSDL describes boundary scan in a chip



IJTAG defines a new language of internal instruments

- IEEE P1687 (IJTAG) defines a language that describes internal test and debug structures



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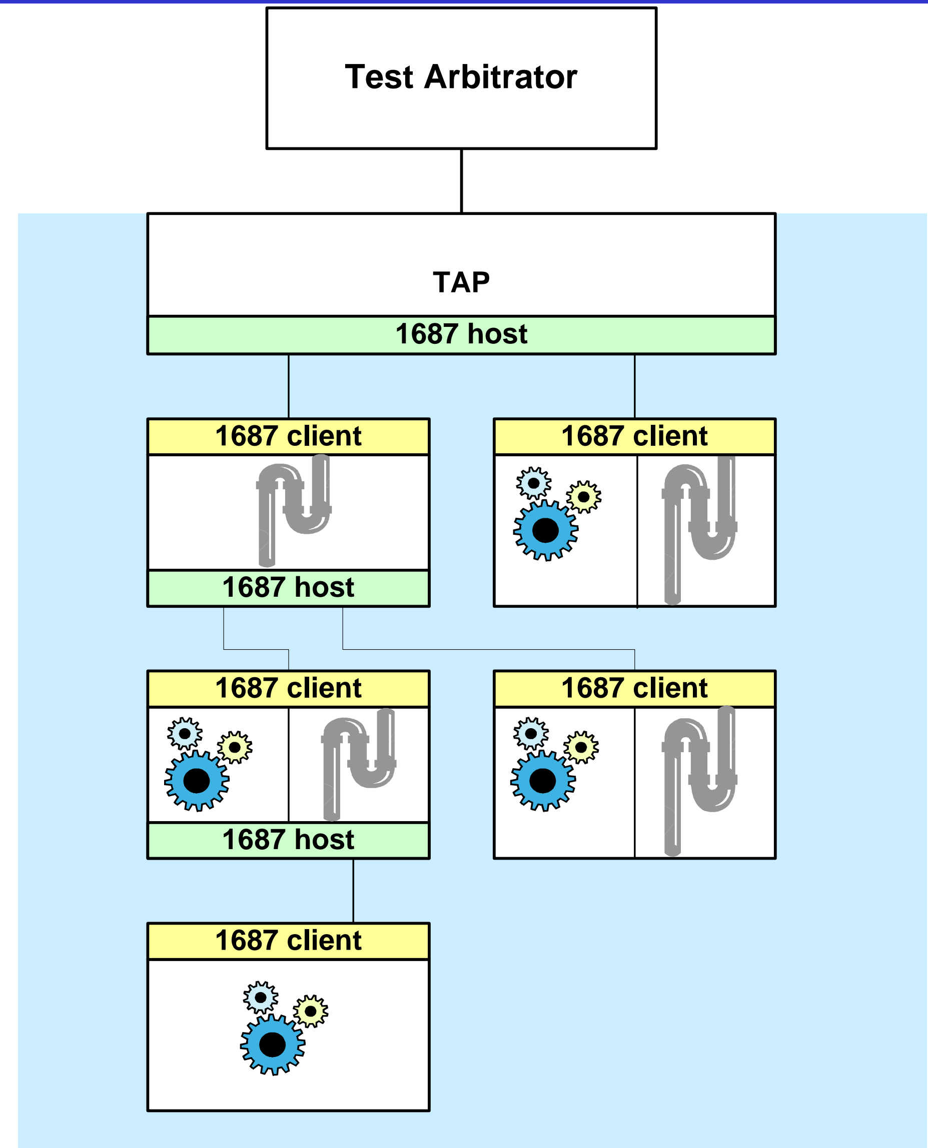
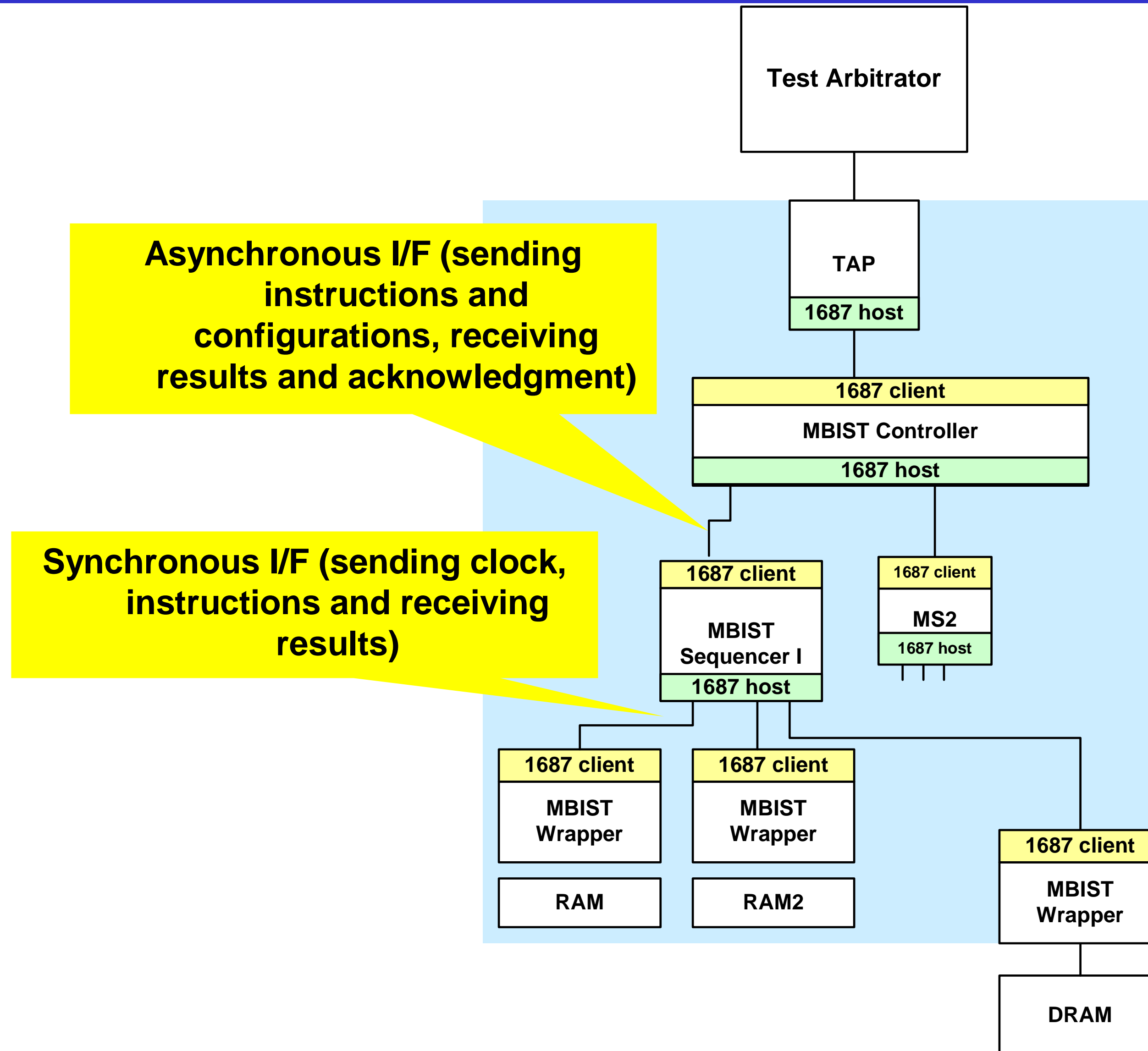
IJTAG (IEEE P1687)

- TAP controller must have
  - 1687 host (1687-ifier)
- Each instrument must have
  - 1687 client
- Each instrument may contain
  - Instrument
  - Pipe
  - 1687 host
  - Any or all
- Each instrument may communicate one level up (interrupt) or one level down if it has both a 1687 client and 1687 host

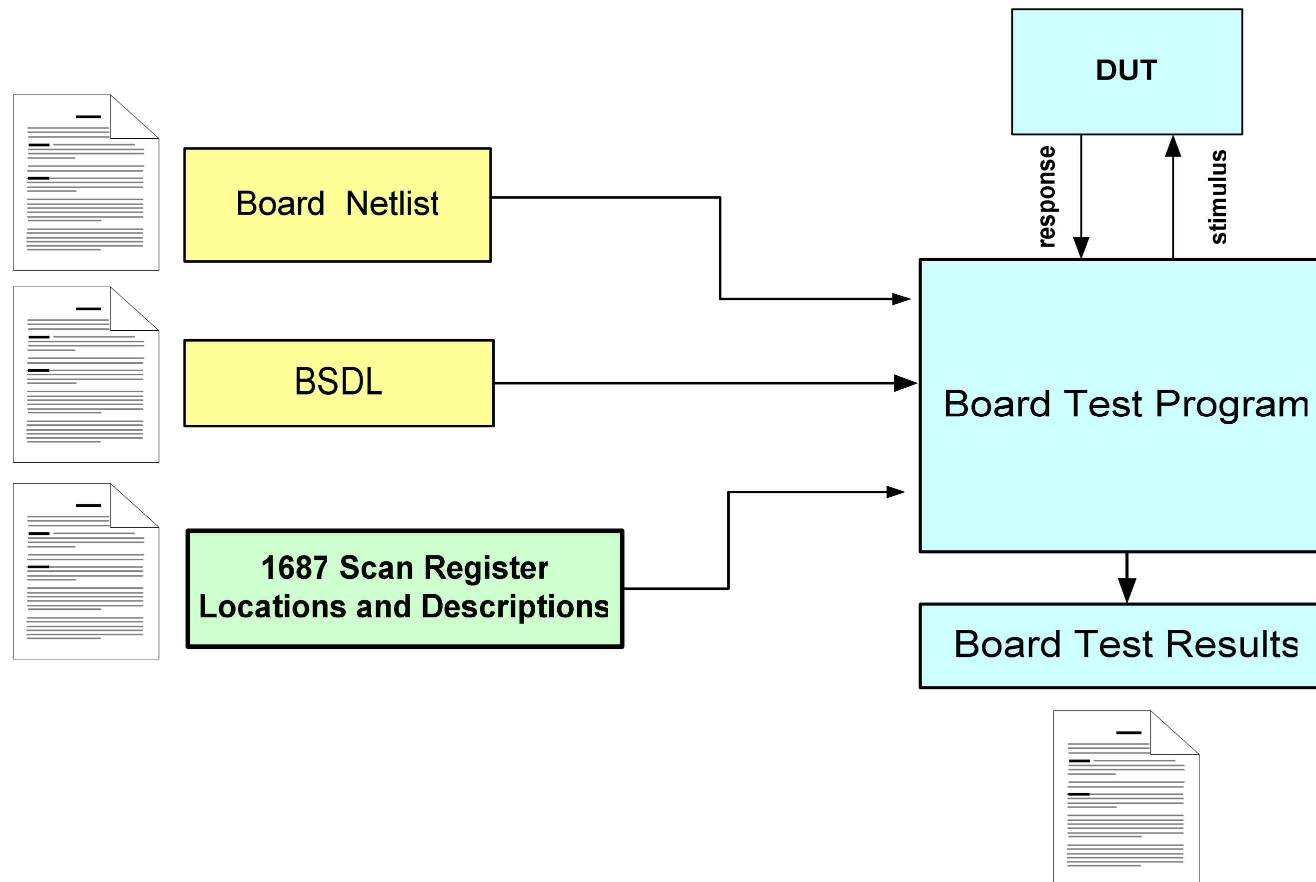


IJTAG (IEEE P1687)



IJTAG (IEEE P1687)

- Scan path location of registers is contained in a file based 1687 description language



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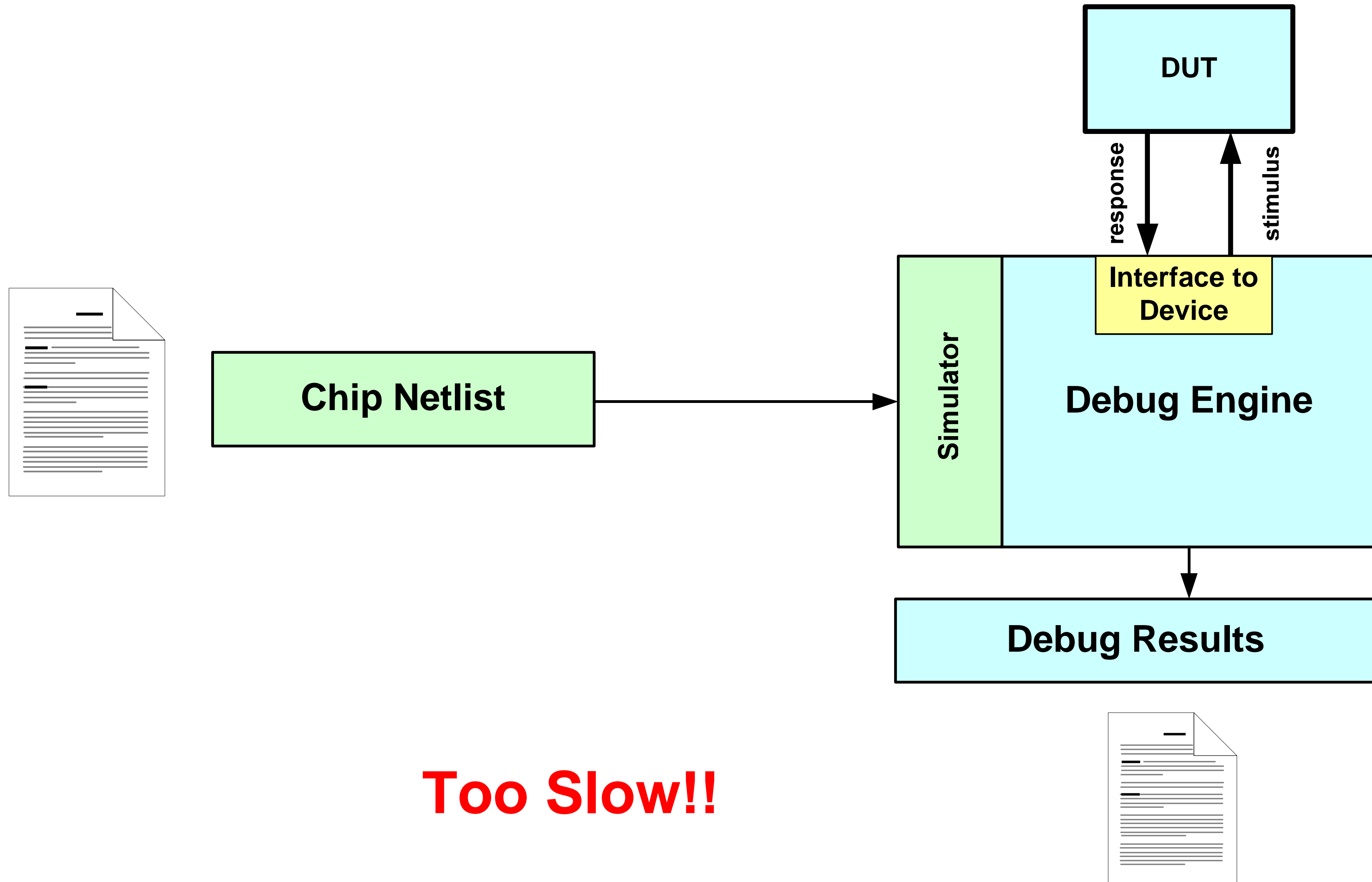
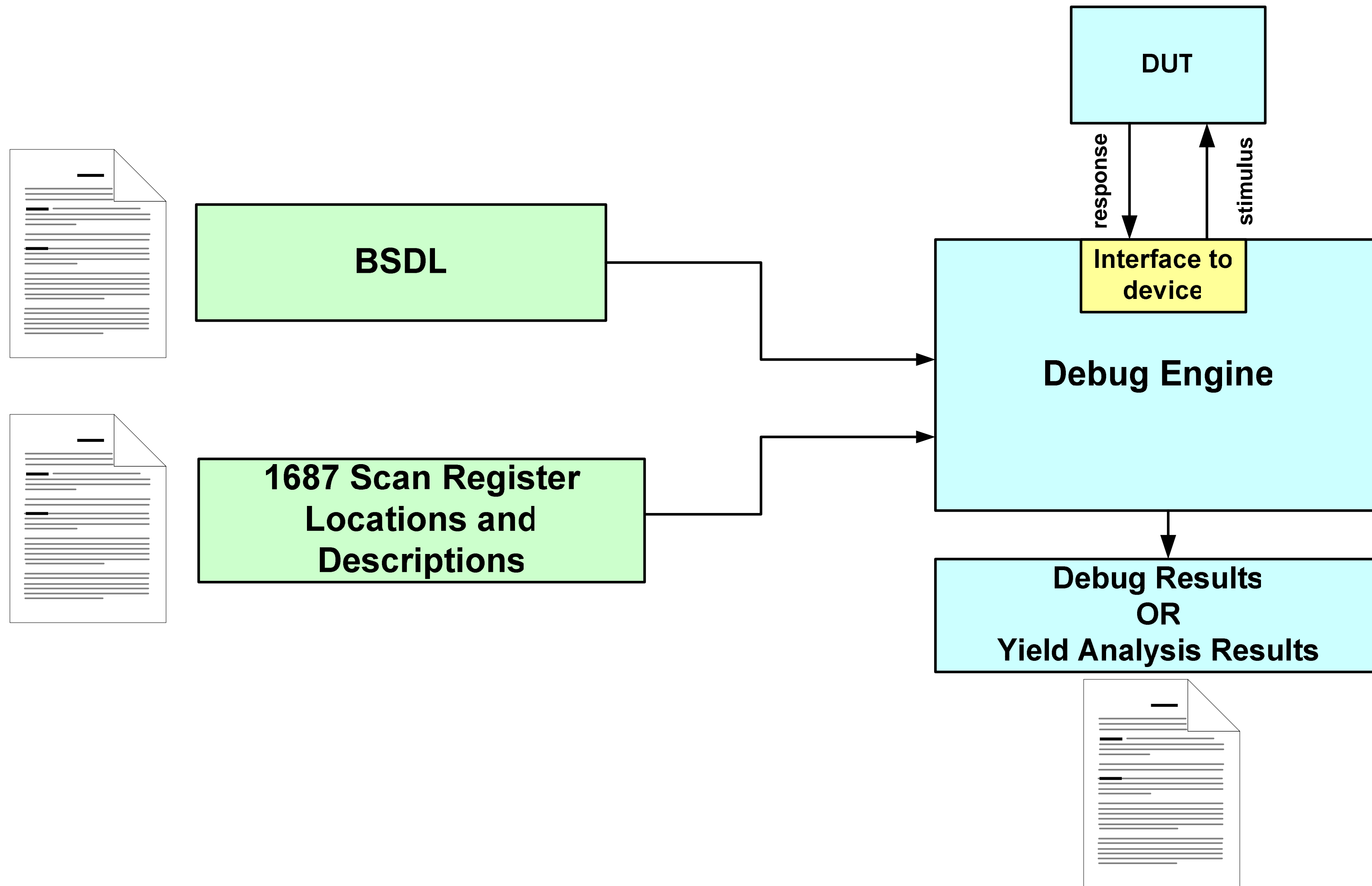
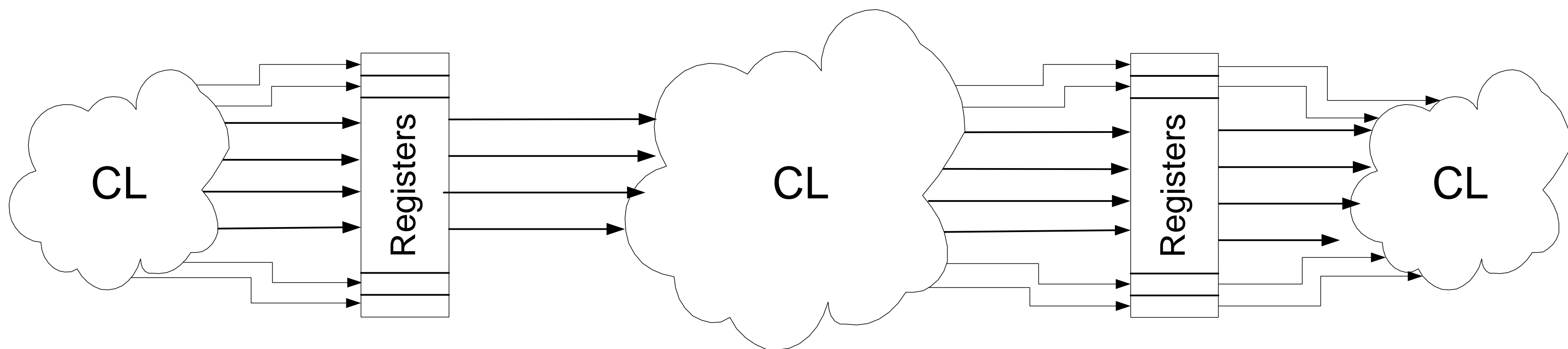


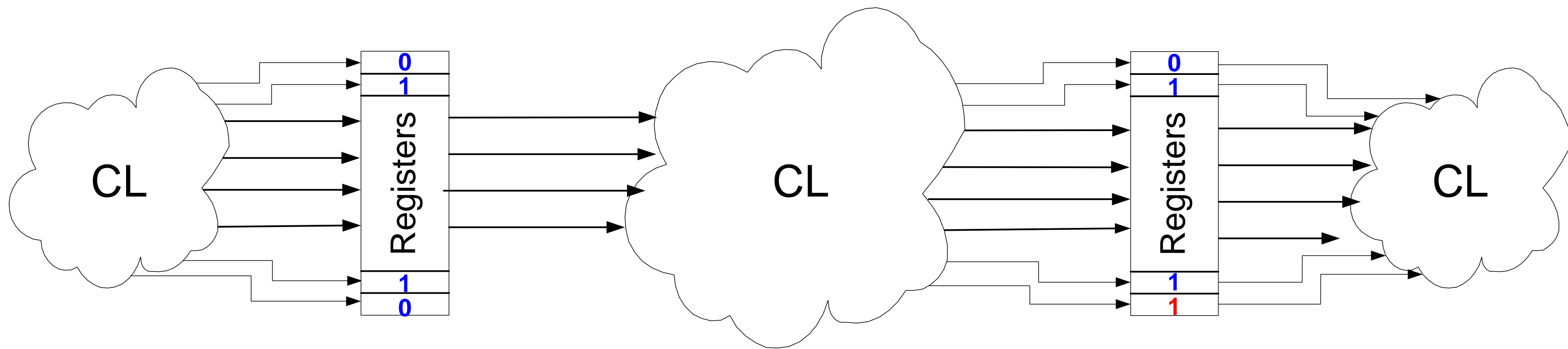
IJTAG (IEEE P1687)



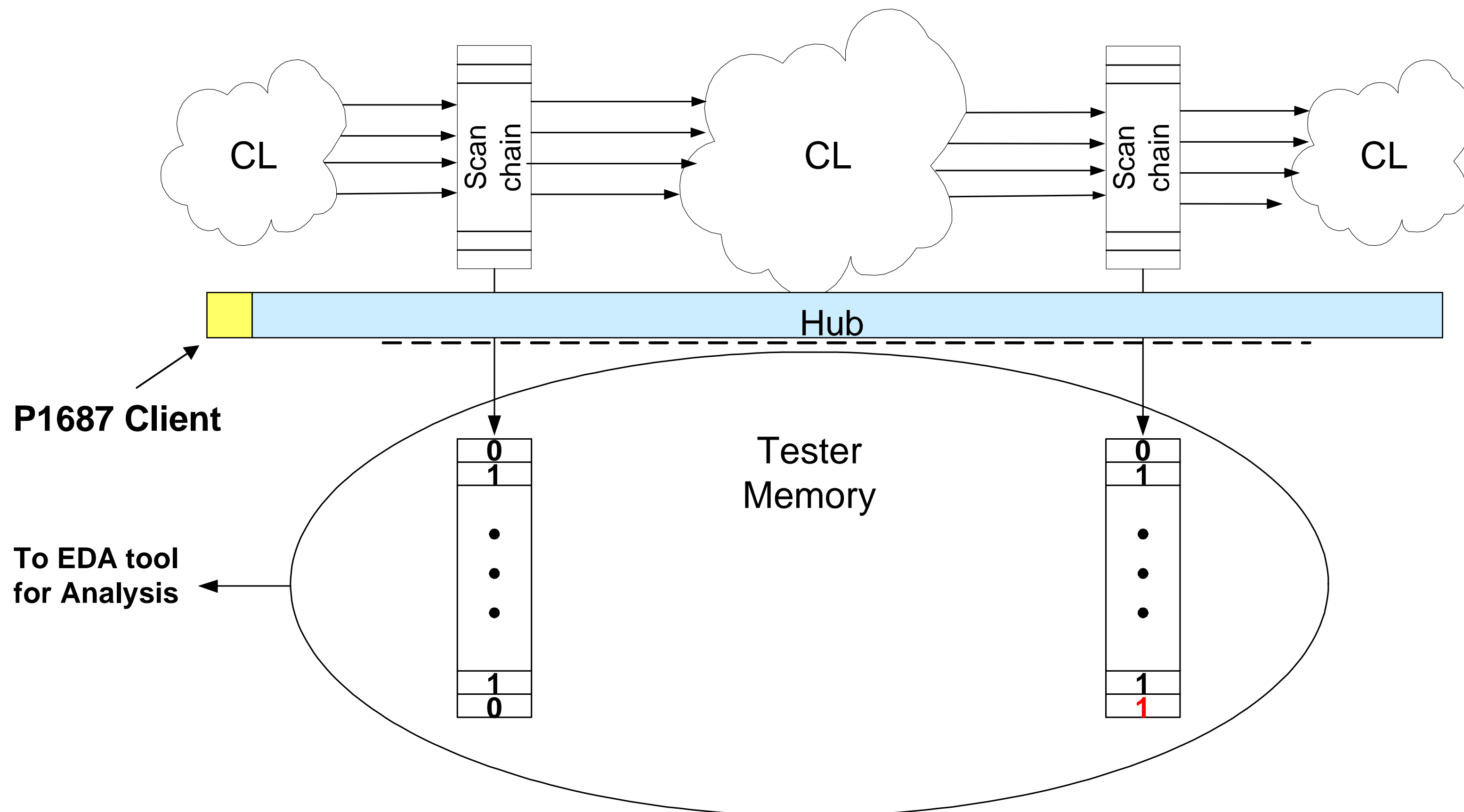
Functional diagnosis – run functionals



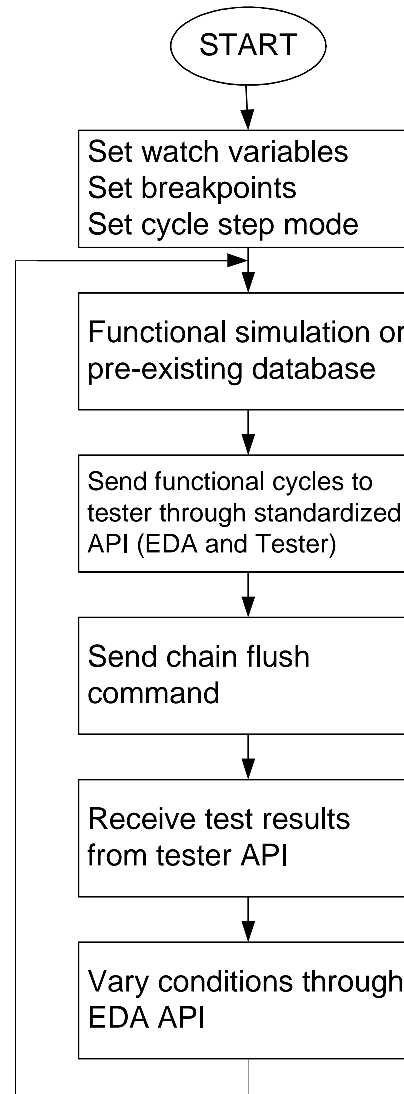
Functional diagnosis – capture results



Functional diagnosis – scan out results



Functional diagnosis



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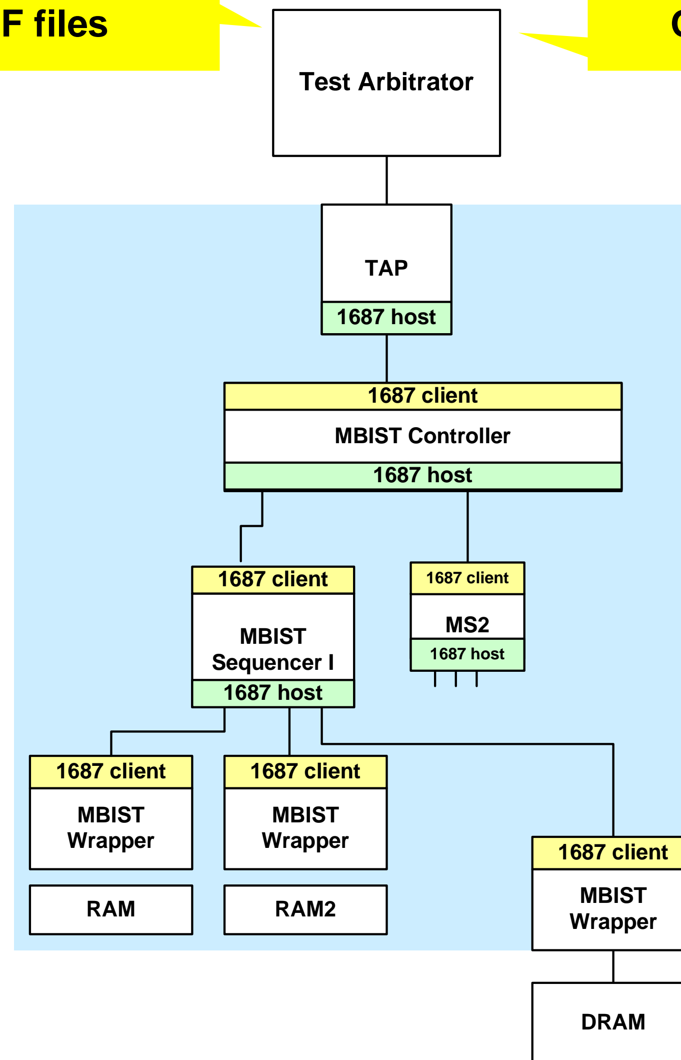
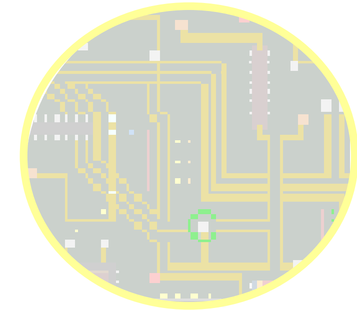
IJTAG (IEEE P1687)

- Using this standardized approach foundries can purchase off the shelf tools for memory yield improvement.
- Similar structures can be created for ATPG yield improvement, for functional vector debug, and for functional to test mode timing correlation



Output X, Y location for FA



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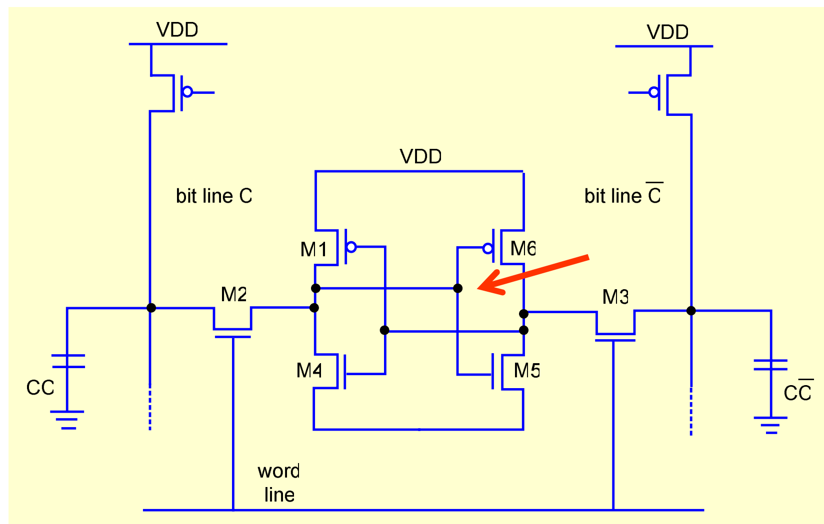
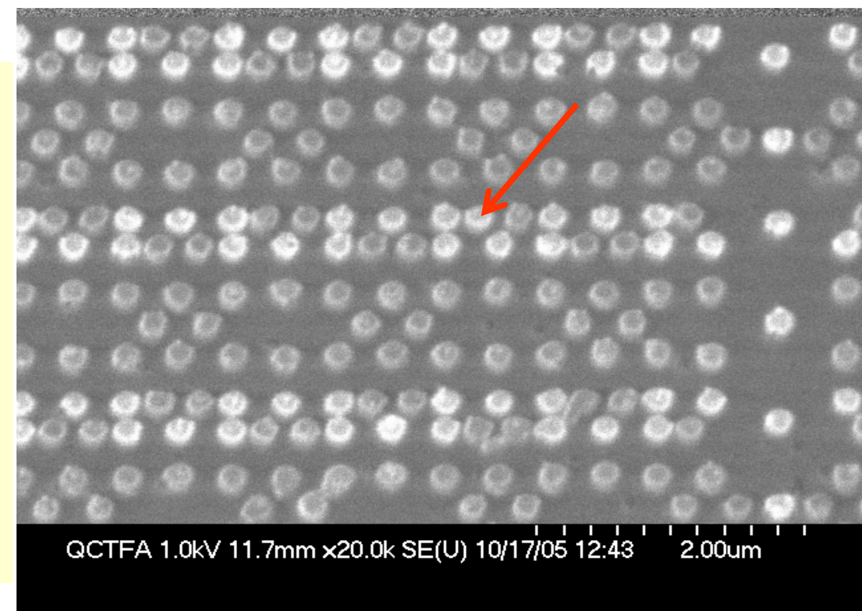
90 nm Memory

- FA result on 90 nm single bit speed failure

6-T SRAM Schematic



90 nm failure SEM Image



Bright spot showed electrical path from poly contact to vdd or “1”

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IJTAG (IEEE P1687) - Considerations

- Determine requirements – what makes sense and what is doable
- Requires adoption of standardized TAP features and architecture that supports IJTAG (specialized instructions)
- Creation of standardized mechanism for high bandwidth data
  - External Instrumentation and synchronization
- Language based Instrument description
- Establishment of Language based Protocols for use
- Relationship to other standards

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Questions?