

IJTAG Examples

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IJTAG Scope

- This standardization effort is intended to address the **access** to on-chip instrumentation, not the instruments themselves. The elements of standardized access include:
 - a description language for the characteristics of the instruments,
 - a protocol language for communication with the instruments, and
 - interface methods to the instruments.

TAP-based Access to Test Features

Desc
Lang

uP/ASIC/ASSP/FPGA

ATE, system,
remote

Internal test features
(BIST, DIAGs,
instruments,
etc.)

Scan
chains

Internal
interface

IEEE
1149.1
TAP

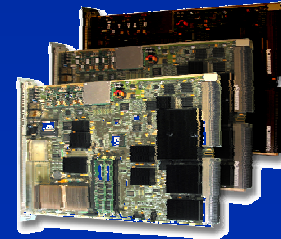
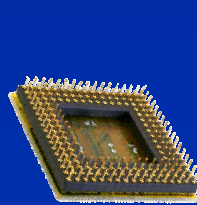
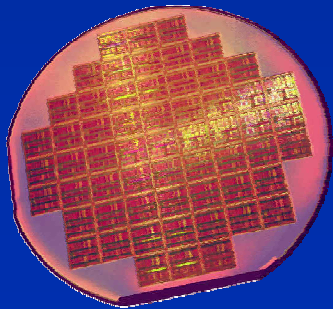
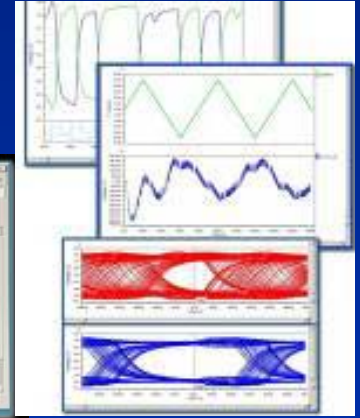
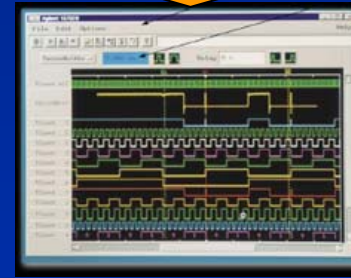
High
band
width

Standard
Protocol

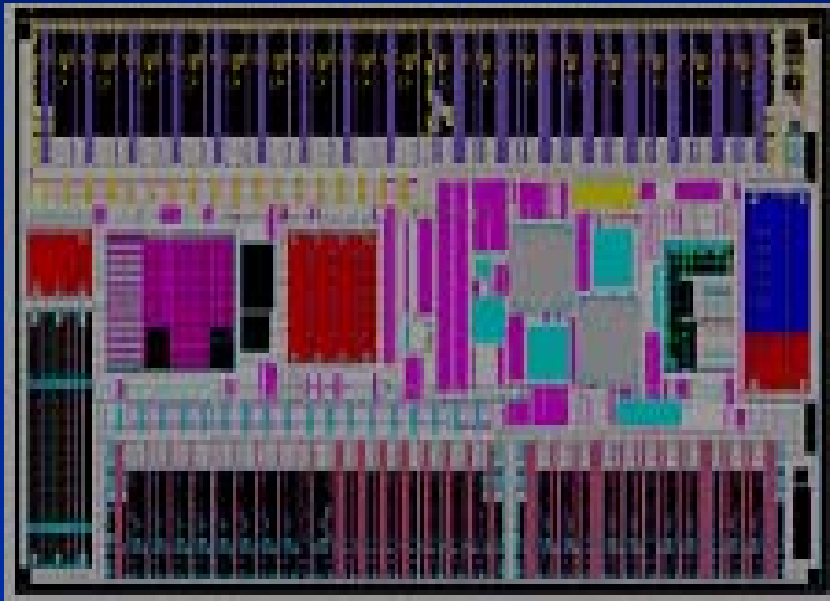
hand
shake

Latest
Protocol

Test
Data



IJTAG Example Instruments



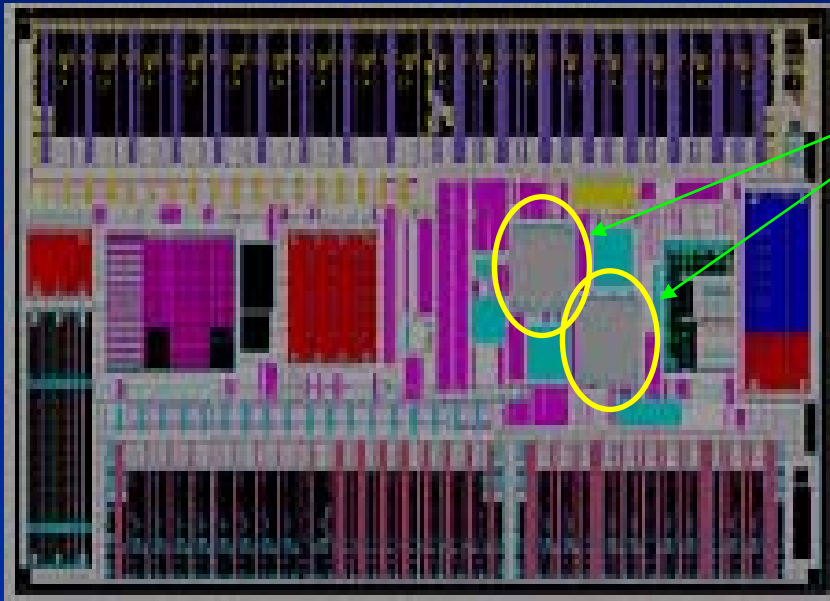
MEMBIST

packet_count_regs

SerDes PRBS BIST

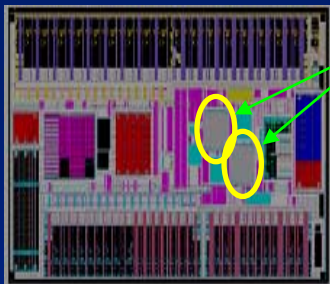
Rx_eye

IJTAG Instrument Description



MEMBIST

IJTAG Instrument Description

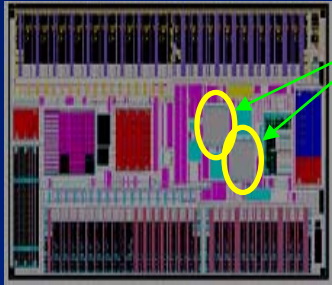


MEMBIST

```
MEMBIST_1 {  
    type = "memory BIST";  
    launch_proc = MEMBIST_1_launch;  
    check_proc = MEMBIST_1_check;  
    test_options = (stop_on_fail,  
                   background,  
                   march_alg);  
}
```

```
MEMBIST_2 {  
    type = "memory BIST";  
    launch_proc = MEMBIST_2_launch;  
    check_proc = MEMBIST_2_check;  
    test_options = (stop_on_fail,  
                   background,  
                   march_alg);  
}
```

IJTAG Protocol



MEMBIST

```
MEMBIST_1_launch (stop_on_fail,  
                  background,  
                  march_alg);  
IR[$_M1stop_on_fail] = $stop_on_fail;  
if ($background == A)  
  { IR[$M1_background_A] = 1; }  
elseif ($background == C)  
  { IR[$M1_background_C] = 1; }  
else { error("bad background")  
      ...  
}
```

IEEE 1532 Example : Flow

attribute ISC_FLOW of xcf01s_vo20 : entity is

```
"flow_program(array) " &
  "initialize          " &
    "(DATA0           2048:?    wait TCK 1)" &
    "(FADDR           16:$addr=0 wait TCK 1)" &
    "(FPGM              wait 14.0e-3)" &
    "Repeat 511        " &
    "(DATA0           2048:?    wait TCK 1)" &
    "(FADDR           16:$addr+32 wait TCK 1)" &
    "(FPGM              wait 14.0e-3)" &
    "Terminate         " &
    "(FADDR           16:0001   wait TCK 1)" &
    "(SERASE           wait 37.0e-3)," &

"flow_verify(array)  " &
  "initialize          " &
    "(FADDR           16:$addr=0 wait TCK 1)" &
    "(FVIFY0           wait 50.0e-6 2048:$data?:CRC)" &
    "Repeat 511        " &
    "(FADDR           16:$addr+32 wait TCK 1)" &
    "(FVIFY0           wait 50.0e-6 2048:$data?:CRC),"
```

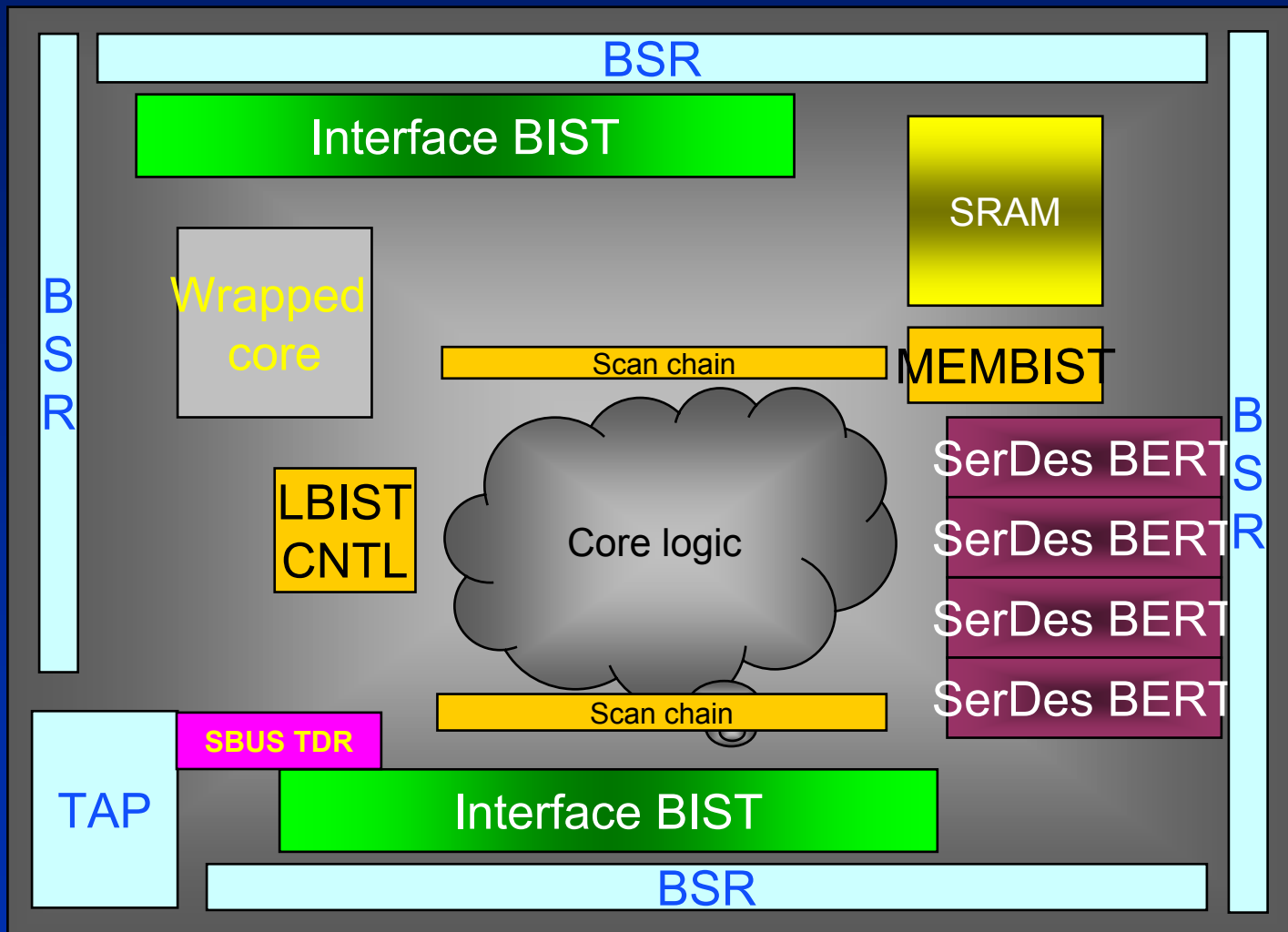
IEEE 1532 Example : Procedure

```
attribute ISC_PROCEDURE of xcf01s_vo20 : entity is
  "proc_verify(idcode)    = (flow_verify(idcode))," &
  "proc_enable           = (flow_enable)," &
  "proc_disable          = (flow_disable)," &
  "proc_erase            = (flow_erase)," &
  "proc_program          = (flow_program(array))," &
  "proc_verify           = (flow_verify(array))," &
  "proc_verify(usercode) = (flow_verify(usercode))," &
  "proc_read             = (flow_read(array))," &
  "proc_read(idcode)     = (flow_read(idcode))," &
  "proc_read(usercode)   = (flow_read(usercode))," &
  "proc_program_done     = (flow_program_done)," &
  "proc_error_exit       = (flow_error_exit)";
```

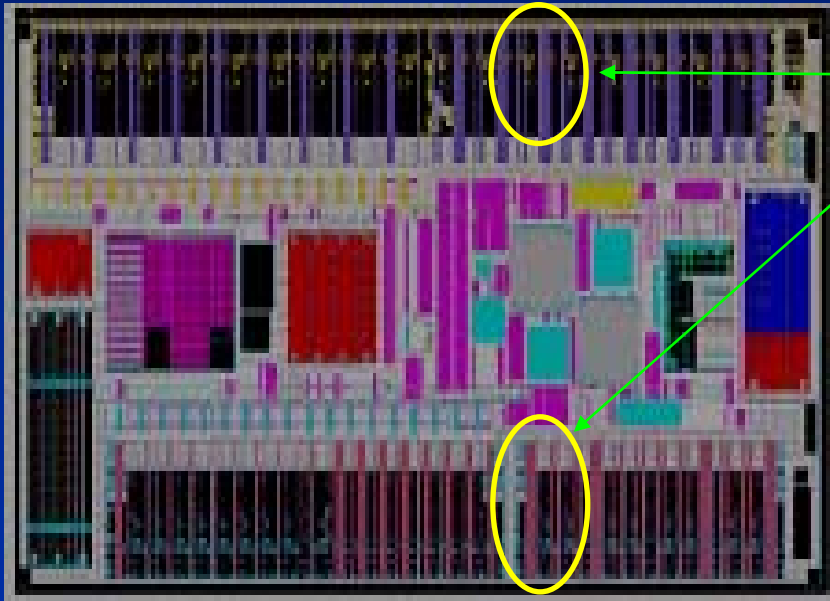
IEEE 1532 Example : Action

```
attribute ISC_ACTION of xcf01s_vo20 : entity is
    "erase          = (proc_verify(idcode)
recommended," &
    "                proc_enable," &
    "                proc_erase," &
    "                proc_disable)," &
    "program        = (proc_verify(idcode)
recommended," &
    "                proc_enable," &
    "                proc_erase," &
    "                proc_program," &
    "                proc_enable," &
    "                proc_verify optional," &
    "                proc_disable)," &
```

TAP Access to Chip Test Features

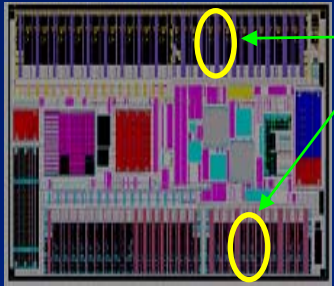


IJTAG Instrument Description



SerDes BIST

IJTAG Protocol



SerDes BIST

{ PRBS_1_sel_PRBS7;
PRBS_1_pre_emph 0110;
PRBS_1_rx_eq_filter 01110100;

PRBS_1_tx_start;
PRBS_1_rx_check;
PRBS_1_rx_eq_tune;
PRBS_1_eye_map;

Next Steps

- Understand what we need to describe
 - Descriptions
 - Protocols
- Understand language options
 - BSDL
 - STIL
 - STAPL
 - ...
- Select a language
- Specify the syntax and semantics

Homework Assignment

- Describe your favorite test feature
- Focus on procedural access
- Email to:
- kepos@comcast.net