The P1687 Proposed HW Architecture Update: SDD06

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Disclaimer!!!

- The following presentation is a “snapshot” of work being done by the P1687 Core Working Group and is subject to change…

- Feedback or concerns about what is presented is welcome. Please send email to:

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P1687 Base Assumptions

- IEEE P1687 will Mandate TAP Control of On-Chip Embedded Instruments using an 1149.1 TAP Controller as the main gateway to the chip [this is our Scope and Purpose].
- Will define the instrument access/protocol, and maybe the interface port – but will not define the instrument
- When not used/active, the P1687 logic is quiescent.
- Will not cause Compliance/Operation Efficiency Problems with the 1149.1 TAP/TAP Controller
- Ease of instrument scheduling – an architecture that allows individual instruments to be enabled and synchronized concurrently (in parallel).
- Automation of: logic insertion; vector generation/translation; generation of "BSDL-like" description files; and verification/test-bench generation.
- Enable reuse of vectors/instruments at board/system-level – minimizing use of "extra signals".
- Will not adversely affect chip engineering budgets (timing, power, area, routing, etc.) any more than currently-supported commonly-used ad hoc methods.
- In final form, P1687 must be adoptable…

P1687 Interpretations

- The 1149.1 TAP and TAP Controller has access or a map of all of the P1687 instruments on the chip and “enables” the P1687 portion of the chip (P1687 ON is an instruction)
- P1687 in at-least one mode must provide access to all public instruments through the TAP-Only for board/system-level reuse
- Instruments are not 1-per-instruction, TDRs are allowed; no extreme requirements can be placed on TCK, TMS, TDI-TDO
- Alternate controllers are allowed if enabled by the TAP Controller
- P1687 will define the preferred instrument interface (w/legacy considerations) – but not the instrument – instruments control their Bandwidth needs
- Instrument control allows operation in parallel (concurrently) – not 1-at-a-time
- “BSDL-like” description of the instruments can be done with just the I/F
- P1687 will not make control or access any worse than it is today

P1687 Instrument Taxonomy

- There are 4 Fundamental Instrument Archetypes that can be mixed-and-matched

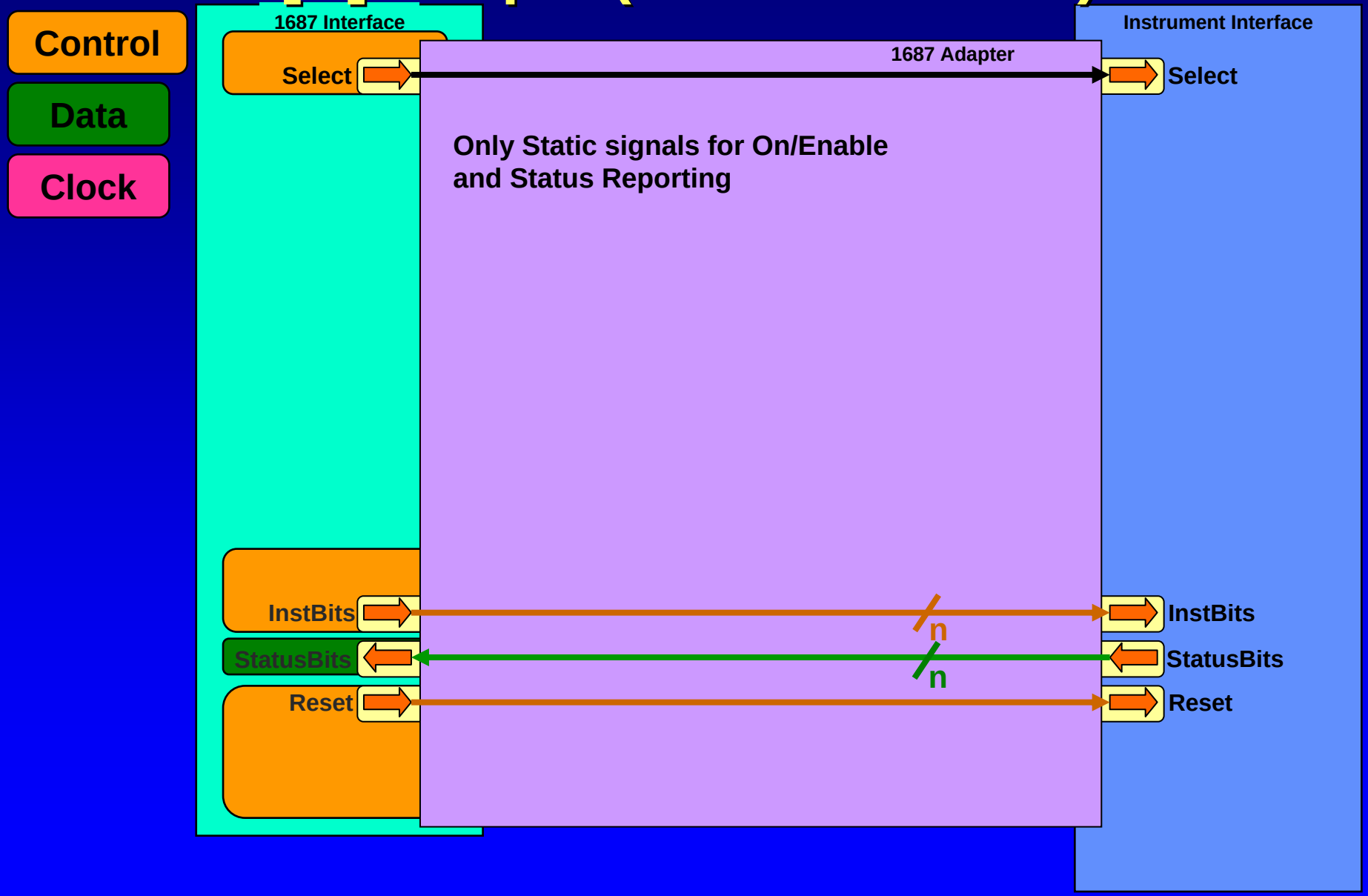
A. Simple (static signals only for control/report)

B. 1149.1 Compatible (uses sequences/signals)

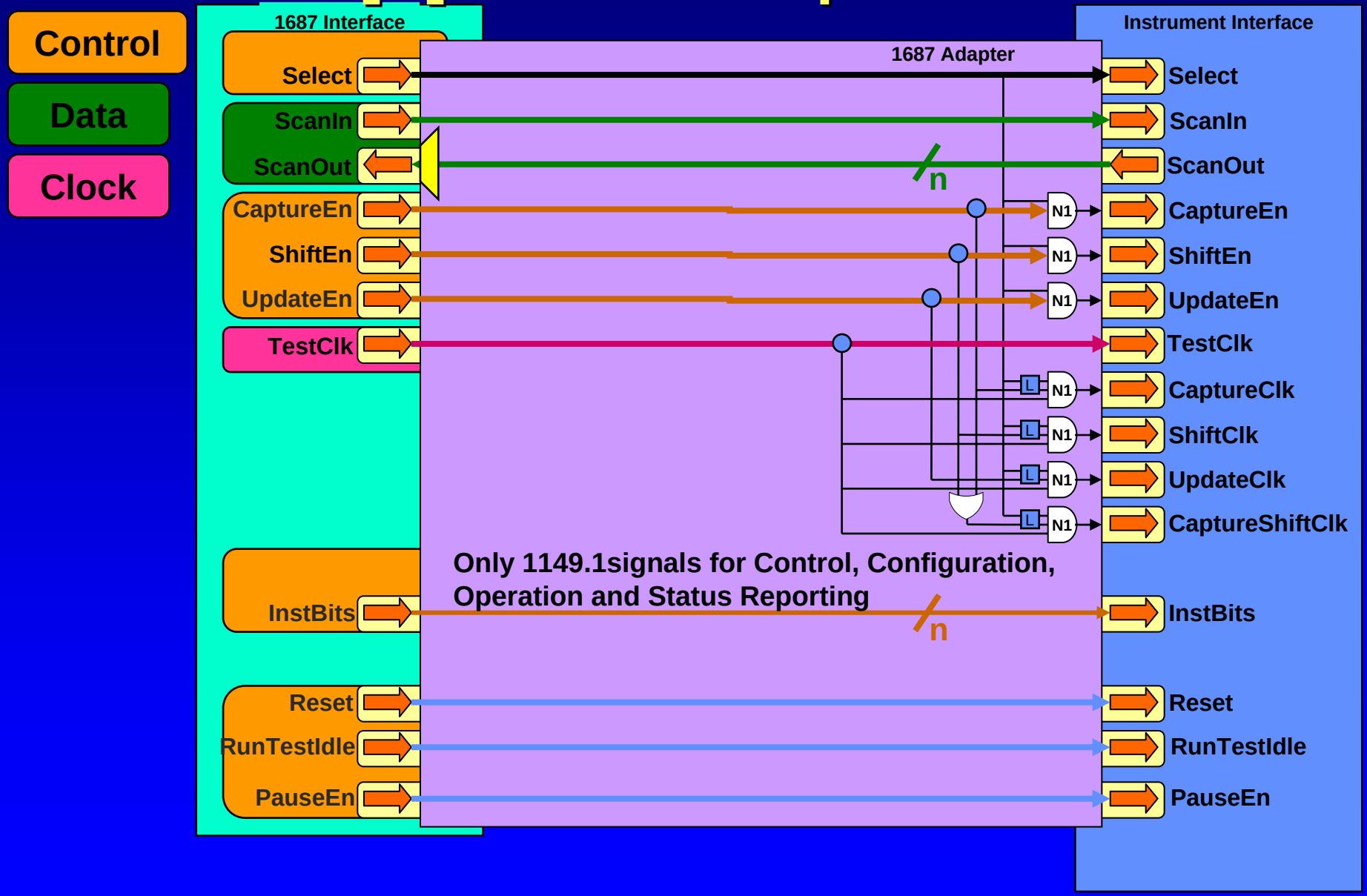
C. Self-Instructed (contains Local IR)

D. Complex (uses non-1149.1 compatible sequences/signals)

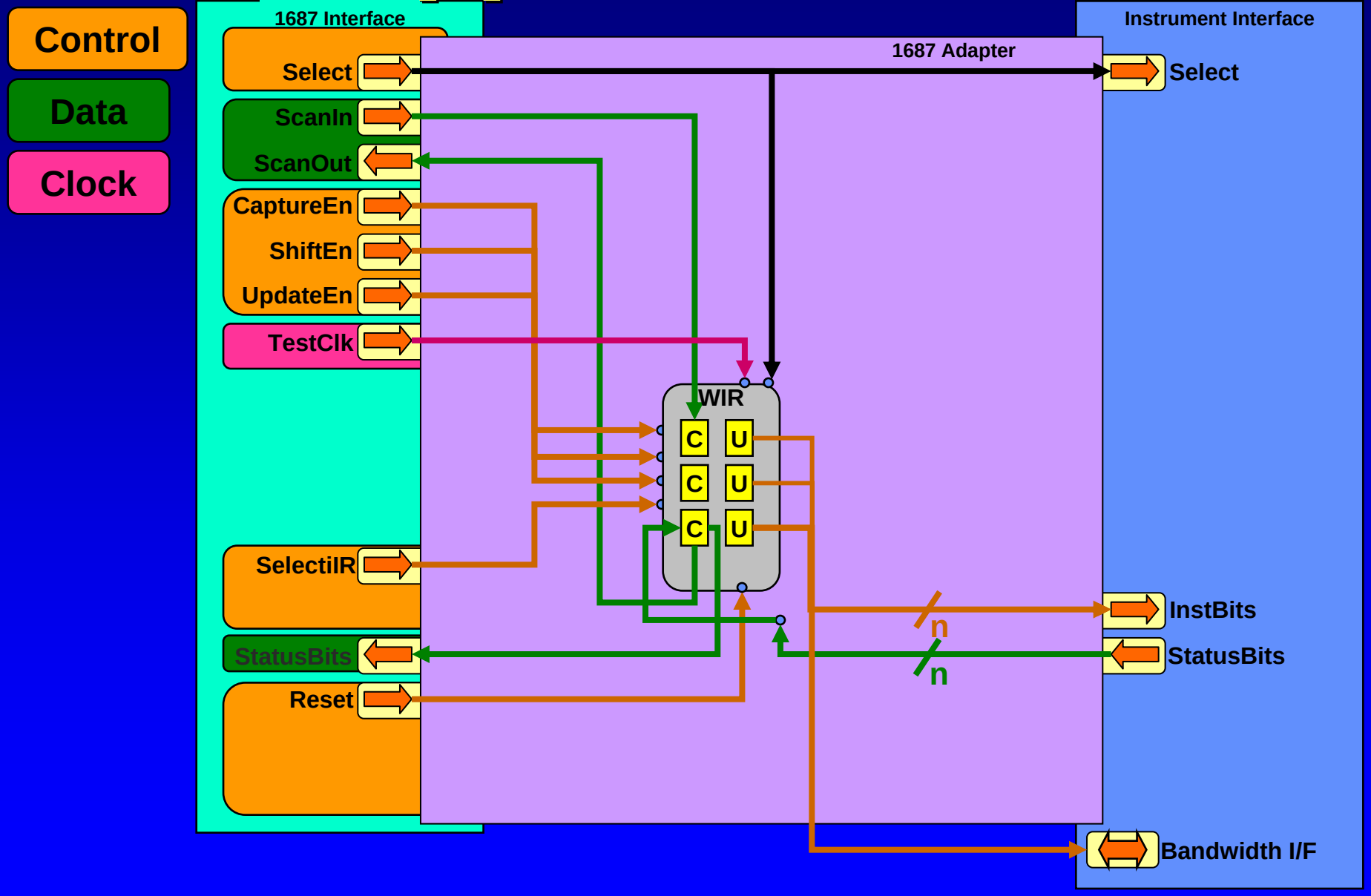
[A] Simple (Self-Contained)



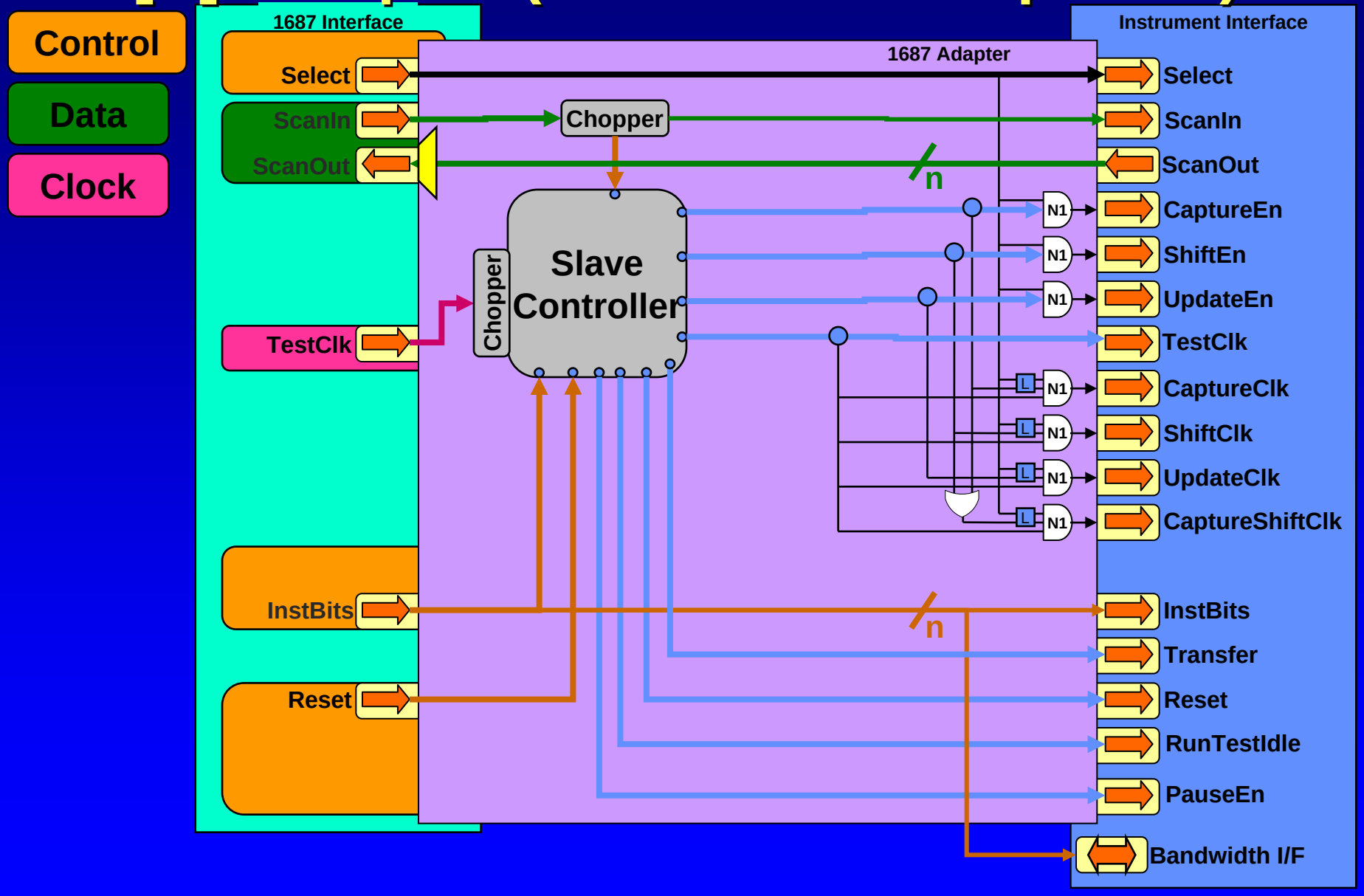
[B] 1149.1 Compatible



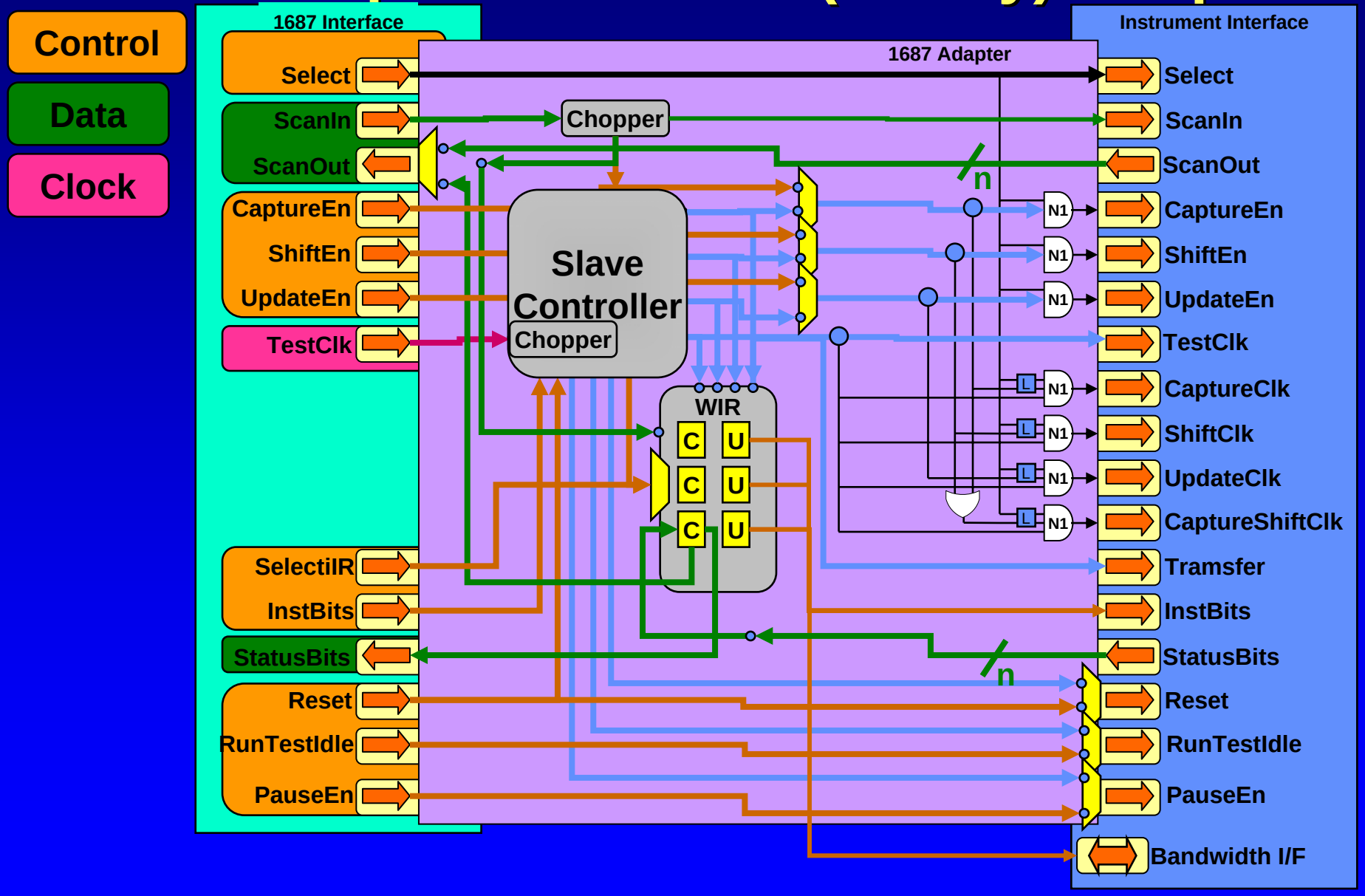
[C] Self-Instructed



[D] Complex (non-1149.1 compatible)



A Close-Up of the Whole (messy) Adapter



Rules

Signal	Type A	Type B	Type C	Type D
Select	Mandatory	Mandatory	Mandatory	Mandatory
ScanIn	NA	Mandatory	Mandatory	Opt.+
ScanOut	NA	Opt.	Mandatory	Opt.+
Capture	NA	One of:	Mandatory	Opt.+
Shift	NA	One of:	Mandatory	Opt.+
Update	NA	One of:	Mandatory	Opt.+
InstBits	Preferred	Opt.	Opt.	Opt.
Status	Preferred	Opt.	Opt.	Opt.
TAPStates	NA	Opt.	Opt.	Opt.+
TCK	NA	Mandatory	Mandatory	Opt.+
SelectIR	NA	NA	Mandatory	Opt.
Reset	Preferred	Opt.	Mandatory	Opt.

+ => Type D: requires at least one of – data path different than TDI-TDO; signal or sequence different than that provided by the TAP or TAP Controller; clock different than TCK

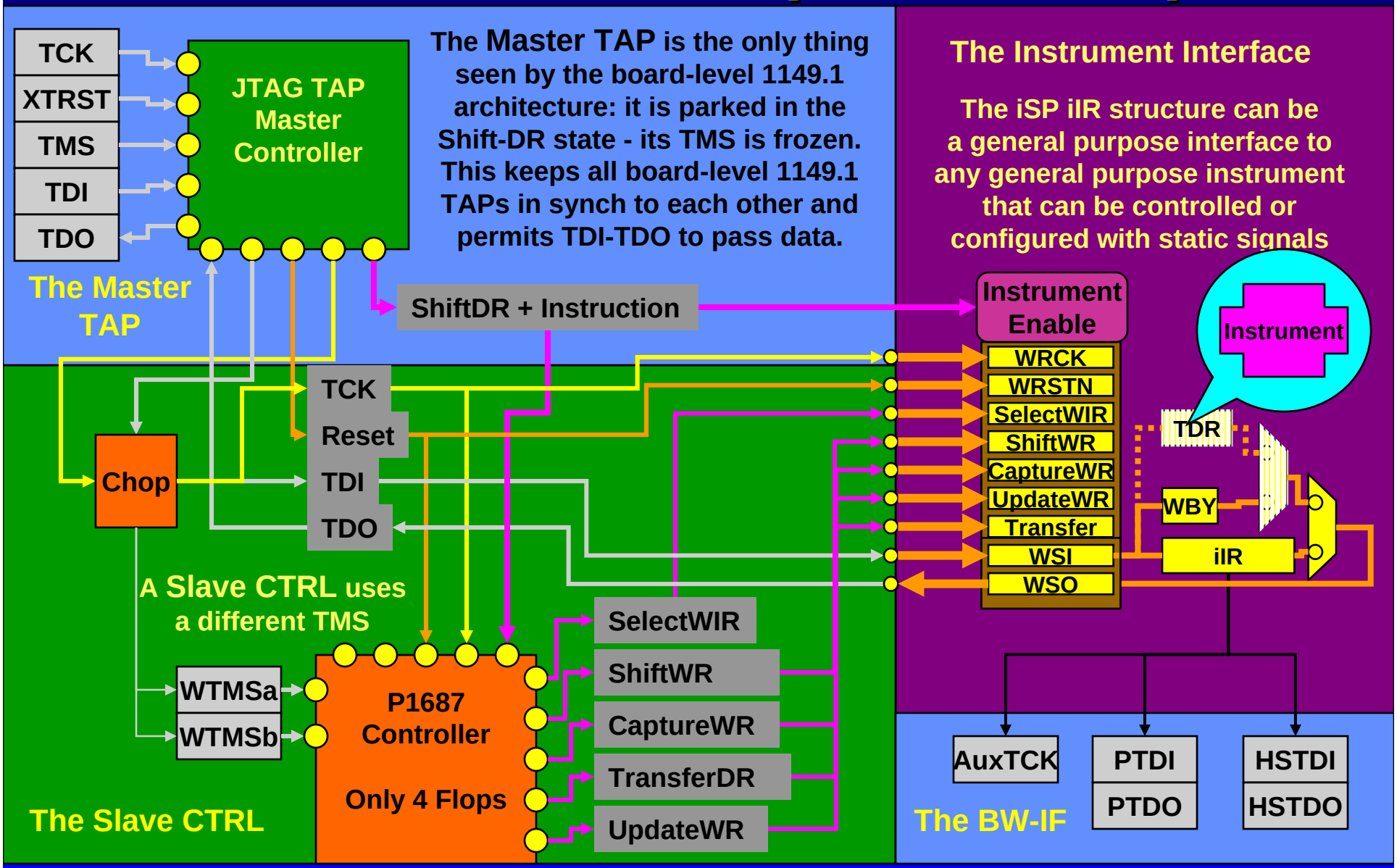
Instrument Documentation

- Instruments can be classified as one of the 4 Fundamentals or a mixture of them
  - Example, A+B+C = Static signals for control or status or both; plus 1149.1 compatible sequence-signals to operate instrument; plus local instruction register to create control and configuration bits
  - Rules applied for merger of types – finite groupings
- Current thoughts on “Instrument BSDL”
  - No language picked yet…
  - A description of the interface signals
  - The length of any shift registers connected to TDI-TDO

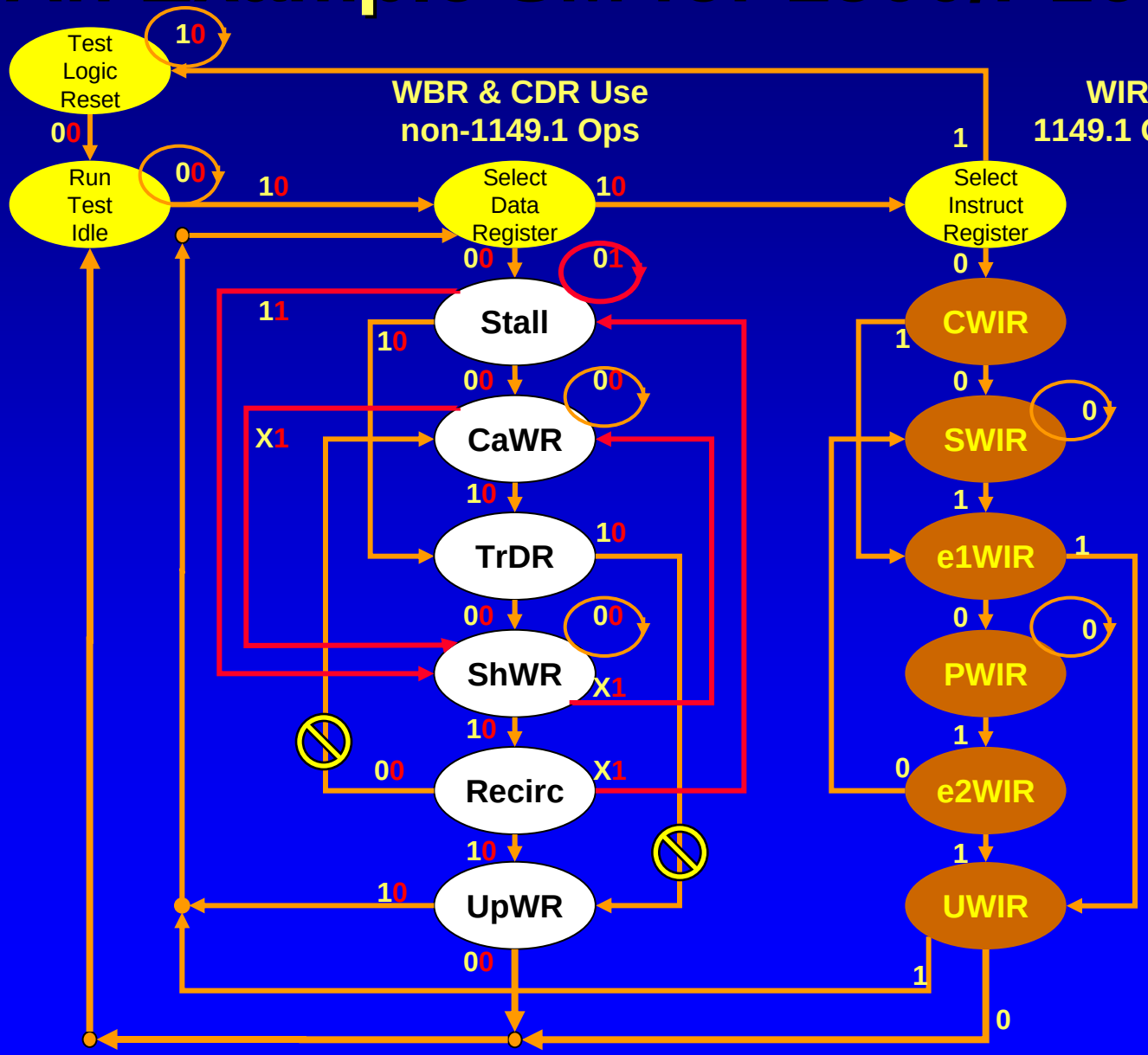
The HW Proposal in a Nutshell

- There are basically 4 parts:
  - A Board-Level Compliant 1149.1 TAP Controller selects targeted instruments with the IR/TDRs, can enable a P1687 Controller, and parks in RTI, Shift-DR, or Pause-DR
  - A P1687 Alternate Controller can create “global” or “local” control signals and sequences
  - The Instrument interface contains elements (signal groups) of the 4-fundamental archetypal instruments
  - A Higher Bandwidth Port can be enabled by the instrument

P1687 HW Arch Proposal example



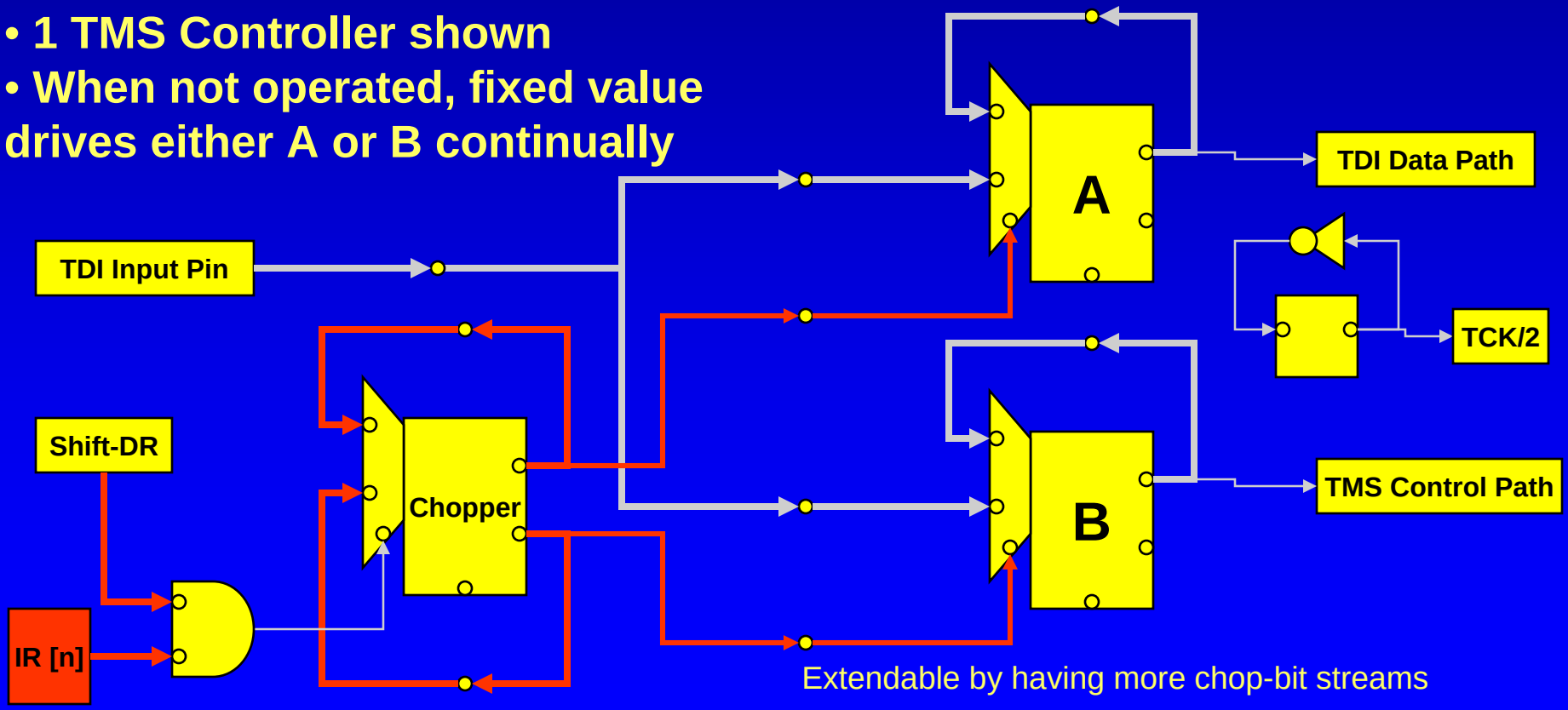
An Example SM for 1500/P1687



Chopper Example

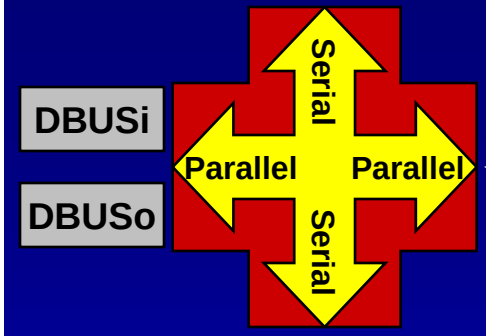
Splits TDI to go to 2 destinations
- **1149.1 TAP parks in Shift-DR**
- **every 1st bit goes to data path**
- **every 2nd bit goes to TMS for Alternate Controller**
- **1 TMS Controller shown**
- **When not operated, fixed value drives either A or B continually**

Best if users of A, B are operating at ½ TCK, then operations look like a Serial-to-Parallel conversion

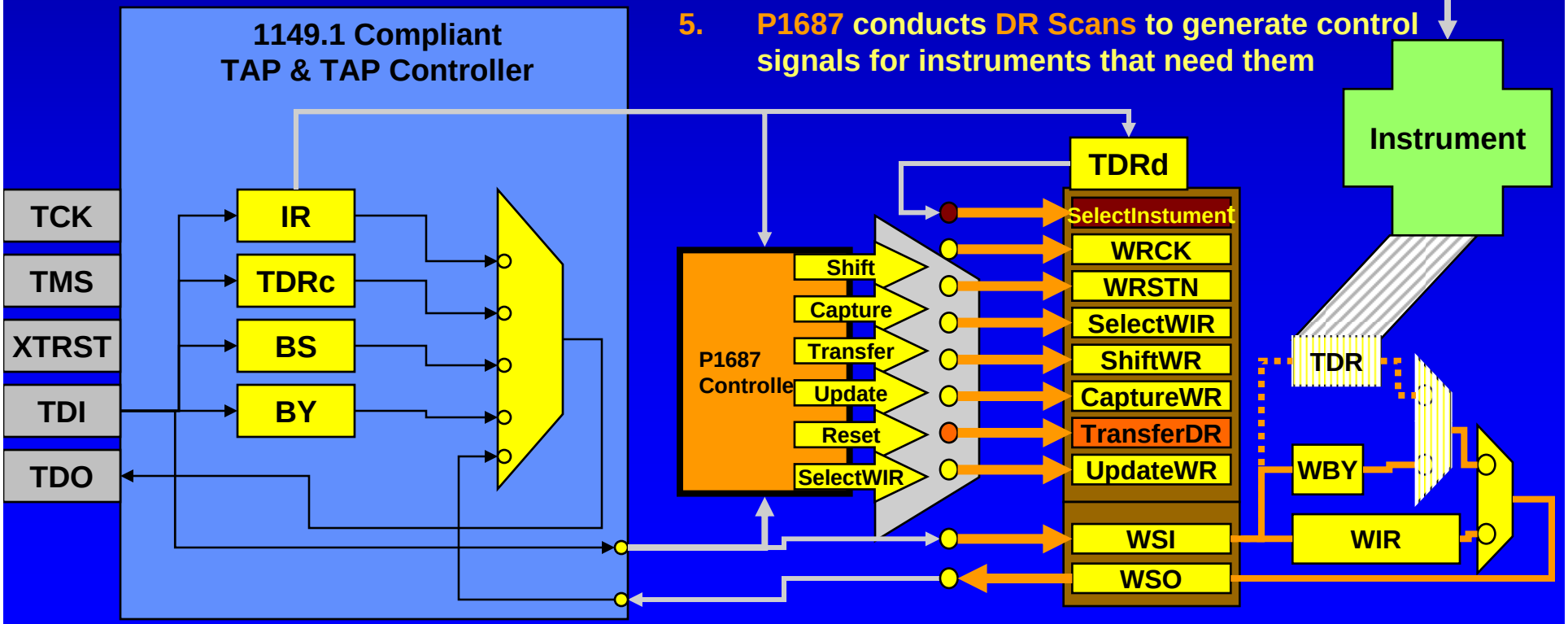


Extendable by having more chop-bit streams

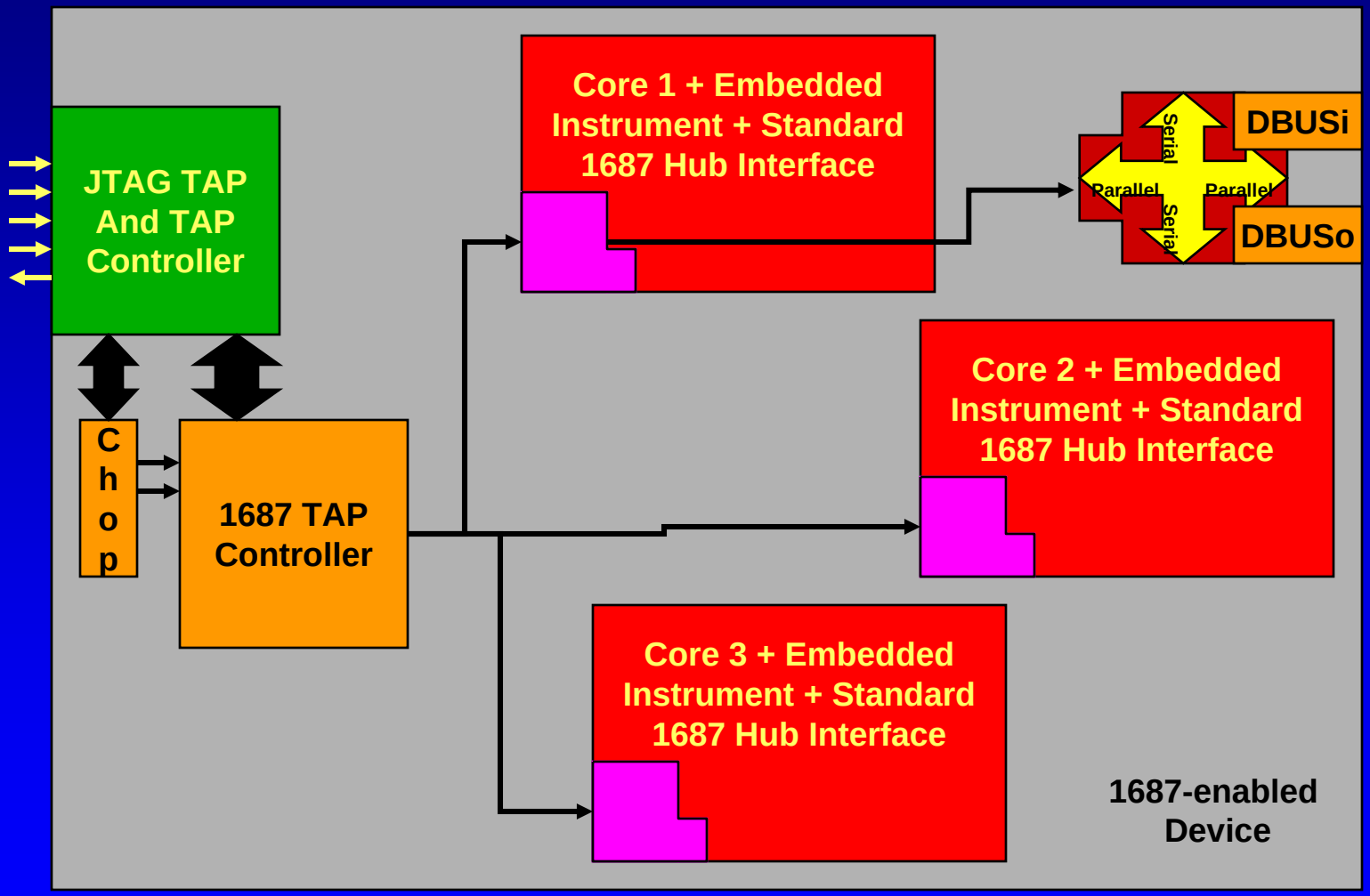
P1687 Operation Flow



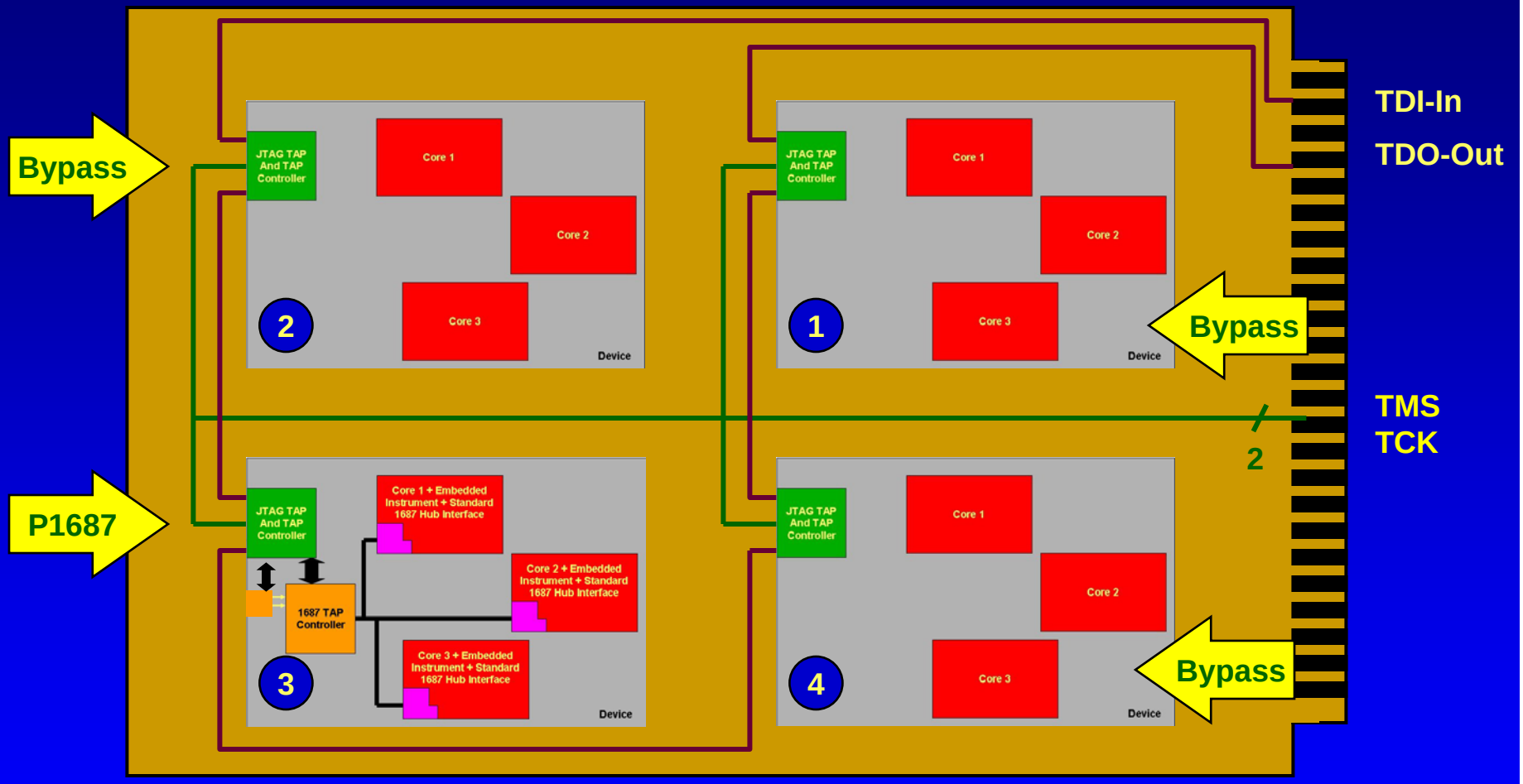
1. 1149.1 moves from TLR to an IR Scan to enable P1687 and to select the TDR of the instruments of interest
2. 1149.1 moves to a DR Scan to drive the TDR bits to select and enable the instruments of interest
3. 1149.1 parks in Shift-DR to activate the P1687 Controller
4. P1687 takes over & conducts an IR Scan to activate the WIRs and to shift configuration & control instructions into them
5. P1687 conducts DR Scans to generate control signals for instruments that need them



Higher-Level View

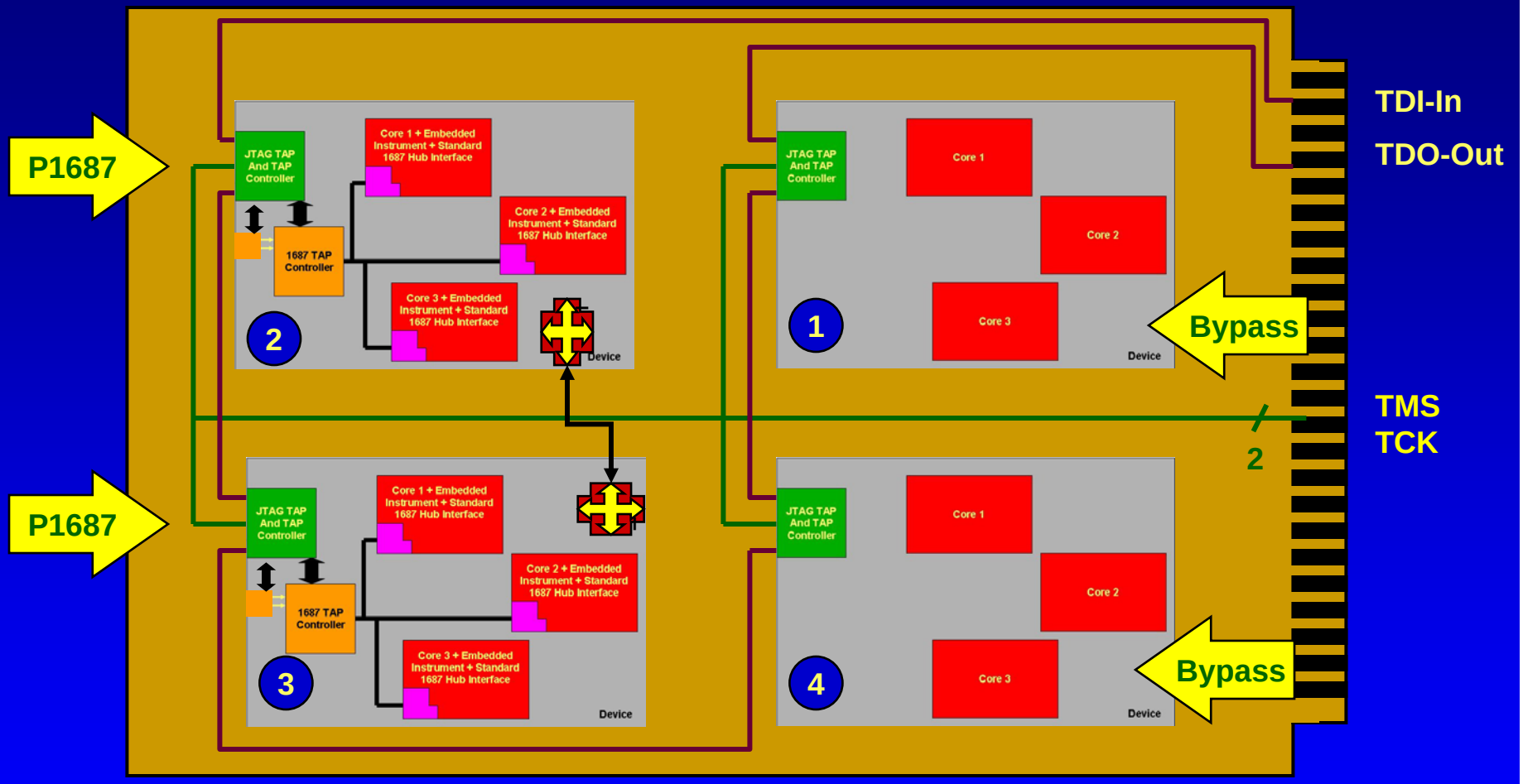


At the Board-Level View



The Bypass register is pre-selected in all devices using the BYPASS instruction prior to entry into 1687 setup mode. When the 1687 device enabled, all TAP controllers are parked in the *Shift_DR* state enabling shifting from edge-connector TDI-In to edge-connector TDO-Out through active Bypass registers in the other devices.

More Board-Level View



While other devices are in Bypass, this shows two P1687-enabled devices operating their instruments in conjunction with one another: for example, #2 has a digital counter used to drive data through a SerDes port; #3 has an LFSR to receive the data on the digital-side of the Serial-to-Parallel Converter.

Details Summary Conclusions

- The 4-step P1687 HW proposal seems to be an efficient first cut at a solution
- Details have been investigated and worked through with design, implementation, automation, and adoption concerns in mind:
  - Retaining 1149.1 compliance/optimization during P1687 Operation by not pushing extreme requirements on TCK, TMS, TDI-TDO
  - Reuse of vectors/instruments at board/system-level by not having Extra Pins in control IF (hard to reuse borrowed pins)
  - Parallel Control of instruments: possible through select/iIR, global control signals – and TDI-chop for Slave-Controller
  - Automation, insertion, documentation, and compliance are supported by having known HW signals and having a known operation flow all based on instrument types