

# **P1687 Working Group Activity**

# Overview

## □ Problem

- Diverse set of DFT structures in a SoC
- Possibly from multiple vendors
- Limited portability of off-the-shelf DFT IP

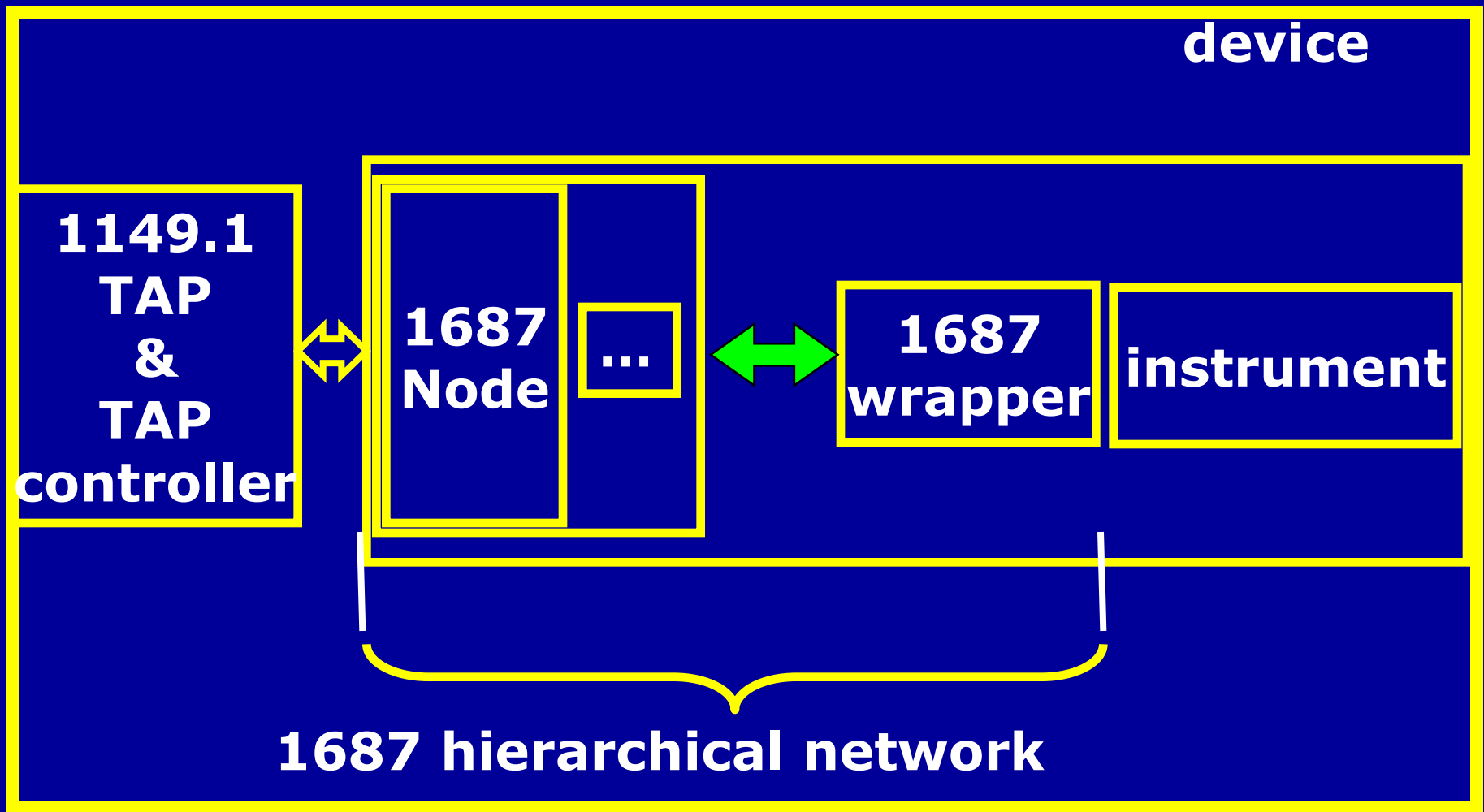
## □ Solution-P1687

- Provides a method to describe access mechanism for instruments
- Standard incorporates hardware and software description of interface
- Instrument details hidden from the user

## □ Enables greater portability of instruments across IP vendors, semiconductor companies, and EDA vendors

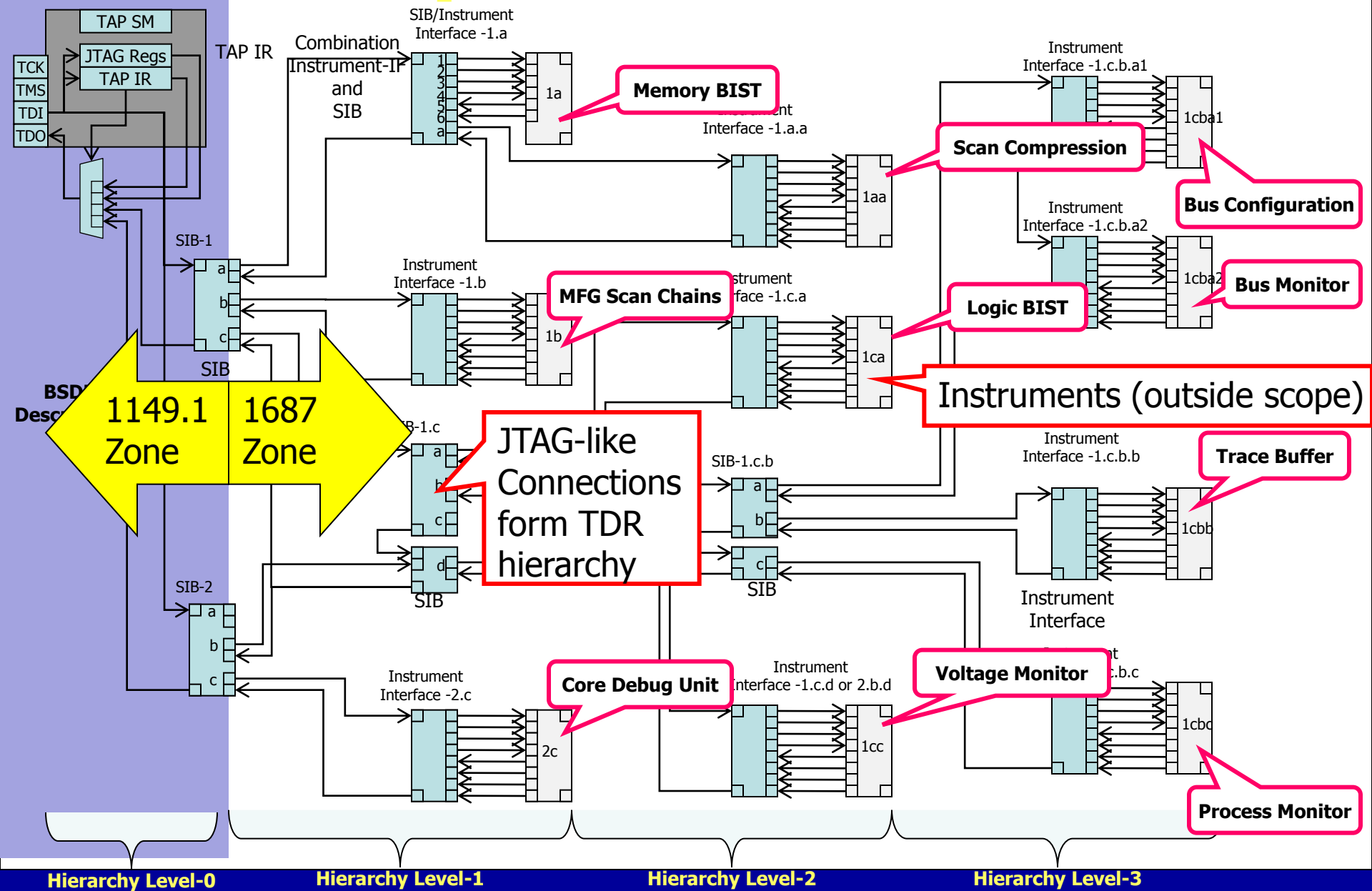
- Portability achieved because of standardized languages to describe operation of instruments

# P1687 Context

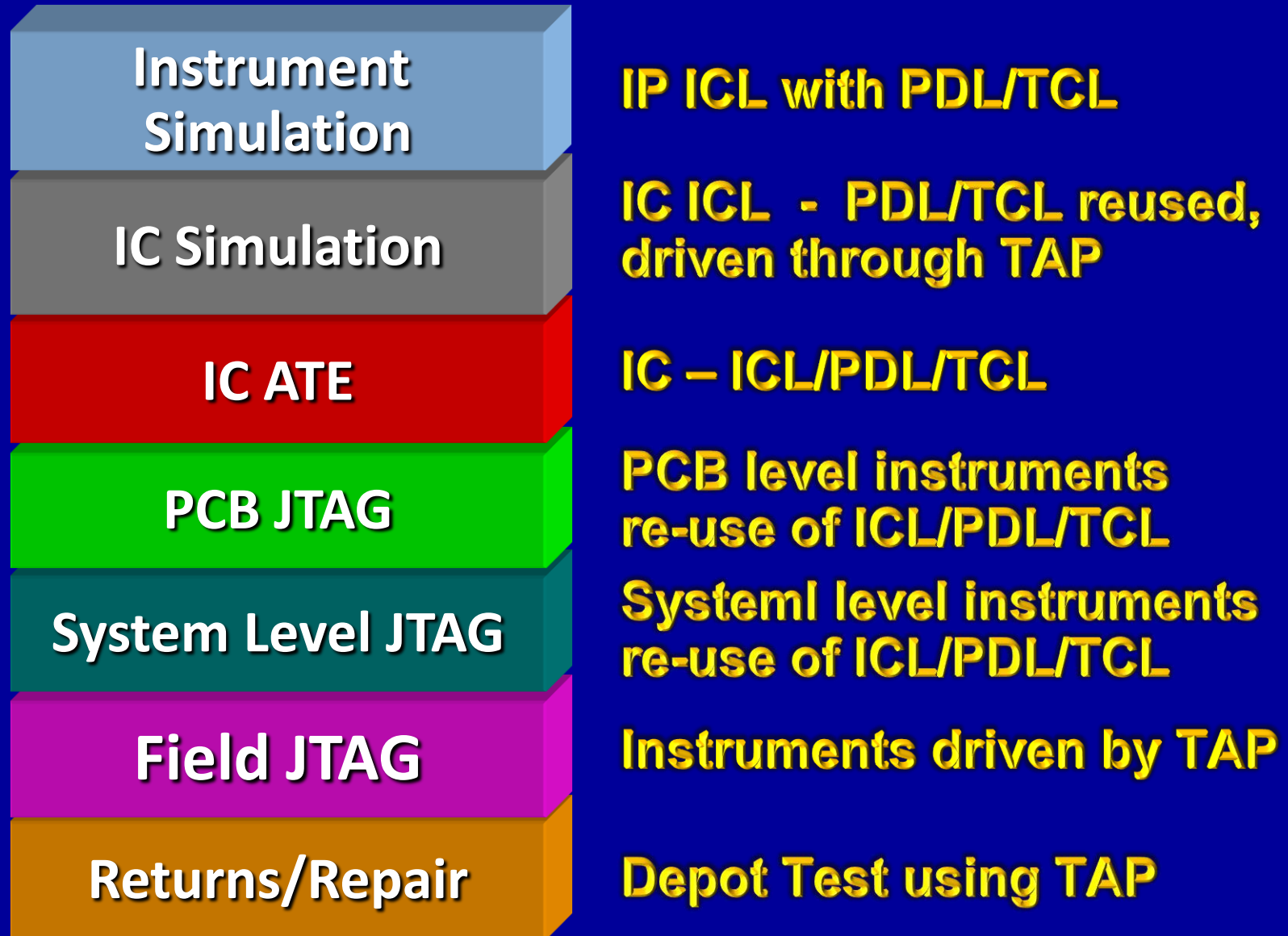


HDL describes the 1687 network  
PDL describes the procedures

# Example 1687 Network



# P1687 Instrument Verification/Test Flow



# ICL on one page: code blocks

```
• Module ( <ModuleName> ) { //Can be also be RawInstrument or SIB that drives grammar rules
• Attributes { //optional code block to list arbitrary user defined attributes. No prescribed usage
•   <attributeName> : <attributeValue>;
• }
• Ports { //Used to list 1687 ports on the module
•   <PortName> {...}
• }
• Instances { //Used to list instances of other modules in the module
•   <InstanceName> {...}
• }
• Registers { //Used to list registers in the module
•   <RegName> {...}
• }
• LogicSignals { //Used to describe muxes, logic driving select ports in the module
•   <SignalName> : <type> {...}
• }
• AliasNames { //Used to alias names for groups of ports and registers in the module
•   <AliasName> : <RegName> | <DataBitPortName> | <StatusPortName>;
• }
• ValueTables { //Used to define tables of symbol-value pairs in the module
•   <TableName> {...}
• }
• TableAssociations { // Used to associated Value table to register or ports in the module
•   <TableName> : <RegName> | <DataBitPortName> | <StatusPortName> | AliasNames;
• }
• SISOPaths { // To be reference by lscan PDL commands
•   <ScanPortName> : <scaninPort>, <scanoutPort>;
• }
• /* Name space within a module wrapper is unique across all <RegNames>, <InstanceNames>, <PortNames>, <AliasName>, <SignalName> */
• }
```

**module**  
**[optional]**  
**actual hardware description**  
**Mnemonics for writing nicer PDL**  
**HW for blackbox PDL**  
**endmodule**

# Raw PDL on one page (PDL API)

## •Level 0:

- **iscope** [pathRelToModule]
- **icomment** <string>
- **ireset**
- **iwrite** <TDR\_bit|UCreg|port|pin> <value>
  - **lwrite** reg|port|pin <name> <value>
  - **lwrite** [pin] <name> <value> # where name is reg|port if [pin] is omitted
  - **lwrite** pin::<<name>|<name> <value> # where pin:: is used only for device-level package pins
- **iread** <TDR\_bit|UCreg|port|pin> <value>
- **iapply**
- **irun\_loop** tck | sck <int>
- **iscan** <scanPort> <length> -si <siData> -so <soData>

## •Level 1:

- **iCaptureData** Reset | Enable | Disable | Single [–maxBits <int>]
- **iGetReadValues** <regName|pinName>
- **iGetWriteValues** <regName|pinName>
- **iGetExpectValues** <regName|pinName>
- **iGetMiscompares**

# Team Members

1. Ken Posse (Avago)
2. Al Crouch (Asset Intertech)
3. Jeff Rearick (AMD)
4. Mike Laisne (Qualcomm)
5. Bill Bruce (Silicon Aid)
6. CJ Clark (Intellitech)
7. J-F Cote (Mentor)
8. Adam Cron (Synopsys)
9. Ramyanshu (Romi) Datta (TI)
10. Stylianos Diamantidis (Globetech)
11. Jason Doege (AMD)
12. Richard Dugan (Agilent)
13. Ted Eaton (Cisco)
14. Heiko Ehrenberg (Goepel)
15. Bill Eklow (Cisco)
16. Pradipta Ghosh (Broadcom)
17. Suresh Goyal (Alcatel-Lucent)
18. JJ Grealish (Intel)
19. Scott Hartranft (Tektronix)
20. Guoxing Hu (ICPTEC)
21. Hongshin Jun (Cisco)
22. Rohit Kapur (Synopsys)
23. Guoqing Li (Huawei)
24. Ed Malloy (Cadence)
25. Harrison Miles (Corelis)
26. Skip Meyers (HP)
27. Jay Nejedlo (Intel)
28. Thai-Minh Nguyen (LSI)
29. Rick Nygaard (Agilent)
30. Srinivas Patil (Intel)
31. Michele Portolan (Alcatel-Lucent)
32. John Potter (Asset Intertech)
33. Paul Reuter (Mentor)
34. Mike Ricchetti (AMD)
35. 34. Thomas Rinderknecht (Mentor)
36. Bill Tuthill (Intellitech)
37. Brad Van Treuren (Alcatel-Lucent)
38. Hugh Wallace (Agilent)
39. Brian Wang (Cisco)
40. Mike Wiznerowicz (Intel)
41. Songlin Zuo (Qualcomm)