What Do Embedded Instruments Look Like?

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Outline

- IEEE P1687 Background
- HSSIO Background
- Embedded Instruments for HSSIO
- P1687-based HSSIO Characterization Results
- Implementation and P1687 API Suggestion
- Conclusion
TAP Access to Chip Test Features

- Power management
- Clock control
- Chip configuration
- Memory test
- Scan test
- Logic BIST
- Debug/diagnosis
- PLL control
- Reduced pin count
- Fault insertion
- Embedded instruments
4 Basic Instrument Types

- [A] Simple or “Self-Contained”
- [B] JTAG or “1149.1 Compatible”
- [C] Local-IR or “Self-Instructed”
- [D] Complex or “Non-1149.1 Compatible”
P1687 Interface

TAP

Instrument
P1687 Interface

TAP

Instrument
P1687 Interface: Flavors

(Ctrl) Select
(Data) InstBits
(Clock) StatusBits

(Type A)
P1687 Interface: Flavors

- Cntrl
- Data
- Clock

- Select
- ScanIn
- ScanOut
- CaptureDR
- ShiftDR
- UpdateDR
- TestClk
- InstBits
- StatusBits
- Other
- 5 TAP states

(Type B)
P1687 Interface: Flavors

- Cntrl
- Data
- Clock

Select
ScanIn
ScanOut
CaptureDR
ShiftDR
UpdateDR
TestClk
InstBits
StatusBits
Other
5 TAP states
SelectWIR

(Type C)
P1687 Interface: Flavors

(Cntrl) (Data) (Clock)

Select
ScanIn
ScanOut
CaptureDR
ShiftDR
UpdateDR
TestClk
Other, non-1149.1
InstBits
StatusBits
Other 5 TAP states
SelectWIR

(Type A) (Type B) (Type C) (Type D)
P1687 Interface: Flavors

(Type A)
Type A: Self-Contained: Simple MBIST
• Clock used doesn’t matter to P1687 if there is no configuration/control of the clock required
• Control and Report structure is comprised only of static signals
P1687 Interface: Flavors

Cntrl
Data
Clock

Select
ScanIn
ScanOut
CaptureDR
ShiftDR
UpdateDR
TestClk

InstBits
StatusBits
Other
5 TAP states

(Type B)
Instrument Scan Interface

- **D-inputs**: status signals from embedded instrument
- **Q-outputs**: control signals to embedded instrument

- **Scan chain safely polled for “done” bit**
- **Update fired after scanin complete**
P1687-Friendly Instrument/TAP Interface

- (optional) high-bandwidth interface
- functional logic
- (optional) functional interface to instrument
- scanin
- scanout
- instrument control, status, and result registers
  - instrument control logic
  - instrument circuitry
- circuitry being measured
High Speed Serial I/O Circuitry DFT

parametric adjustment interfaces and circuitry

TX

RX

LFE

DFE

PRBS gen

TX BERT circuitry

PRBS detect

error count

RX BERT circuitry

intraphase delay

dff

eye mapping circuitry

ref_ck

VREF DAC

comp

VREF DAC

intraphase delay

dff

error count

TX BERT circuitry

PRBS gen

TX

RX

LFE

DFE
[B] 1149.1 Compatible

Only 1149.1 signals for Control, Configuration, Operation and Status Reporting
P1687 Interface: Flavors

- Cntrl
- Data
- Clock

- Select
- ScanIn
- ScanOut
- CaptureDR
- ShiftDR
- UpdateDR
- TestClk
- InstBits
- StatusBits
- Other
  - 5 TAP states
- SelectWIR

(Type C)
[C] Self-Instructed

Control

Data

Clock

1687 Interface

Select

ScanIn

ScanOut

CaptureEn

ShiftEn

UpdateEn

TestClk

WIR

InstBits

StatusBits

Reset

Bandwidth I/F
Instrument Examples

Type C: Self-Instructed: 1500 Boundary Register with WIR
- Instrument Control/Report are from a Local IR
- IR Control/Report from 1149.1 TAP Controller
P1687 Interface: Flavors

Cntrl   Data   Clock

Select  ScanIn  ScanOut
CaptureDR  ShiftDR  UpdateDR
TestClk
Other, non-1149.1
InstBits
StatusBits
Other 5 TAP states
SelectWIR

(Type A)  (Type B)  (Type C)  (Type D)
Instrument Examples

Type D: Non-1149.1-Compatible: Complex Wrapper I/F

- A Control or Report signal requires a sequence/signal not available from a compliant 1149.1 TAP Controller
- ...or a Clock other than TCK
- ...or Data from other than TDI-TDO
[D] Complex (non-1149.1 compatible)
## Some Real Instrument Examples

- I/O drive strength control
- Memory BIST
- AC_CAL clock stretch calibrator
- SerDes BERT
- Temperature diode with ADC
- Ring Oscillators for process monitoring
- Vdd droop monitors