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Standard for Test Access Architecture for Three-Dimensional Stacked ICs

Sponsor

3D Test Working Group
of the
IEEE Computer Society Test Technology Standards Committee

Approved <Date Approved>

IEEE-SA Standards Board

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Draft Standard for Test Access Architecture for Three-Dimensional Stacked ICs
1. Overview

1.1 Three-Dimensional IC Stacking Technology

The market continues to pull for integrated circuits (ICs) with higher performance, better energy-efficiency, and lower cost. While conventional transistor scaling runs into increasing technical and financial hurdles, the baton in the race to create attractive new IC products that meet market expectations is gradually being taken over by innovations in multi-die stack-assembly and packaging techniques. Large-array fine-pitch micro-bumps implement dense high-performance low-power inter-die interconnects. Through-silicon vias in combination with wafer thinning provide electrical connections via the back-side of a die’s substrate, enabling stacks of more than two dies. Interposer dies, possibly implemented in a passive technology offer low-cost high-performance ways to interconnect multiple dies. Packaging costs are drastically reduced by using cheaper materials and processes and by turning packaging into a wafer-level operation. The I/O-to-pin fan-out functionality of package substrates is replaced by redistribution metal layers, cost-effectively manufactured at wafer level. And the cost of plastic or ceramic packages is circumvented by applying epoxy mold compounds at wafer level.

These and other interconnect, assembly, and packaging technology innovations lead to a wide range of multi-die stack architectures, including so-called “2.5D”-stacked ICs (SICs) consisting of multiple active dies stacked side-by-side on a passive silicon interposer base, “3D”-SICs comprising a tower of stacked active dies, and multi-tower-SICs which consist of multiple towers of stacked active dies side-by-side on a passive silicon interposer. Both in variety and product volumes we have yet only seen the beginning of multi-die stacks.

Like all micro-electronic products, these die stacks need to be tested before they can be shipped with acceptable quality levels to their customers. We distinguish the following tests: (1) pre-bond tests prior to stacking, (2) mid-bond tests on incomplete, partial stacks, (3) post-bond tests on complete yet not packaged stacks, and (4) final tests on the final packaged product. The number of possible test flows grows quickly with the number of dies in the stack and hence is subject of automated trade-off evaluation and optimization.
1.2 Motivation for a 3D-DfT Standard

A well-architected design-for-test (DfT) test access infrastructure is indispensable for achieving a high-quality test. Not only do we need conventional 2D-DfT structures (such as internal scan chains, test data compression circuitry, IEEE Std 1500 wrappers around embedded cores, and/or built-in self-test (BIST) engines) that provide test access within a single die, we also need new approaches for testing stacked systems. Especially once a (partial or complete) vertical stack has been formed (i.e., in mid-bond, post-bond, or final testing phases), we also need novel 3D-DfT structures that provide test access from (and to) the external stack I/Os to (and from) the various dies and inter-die interconnects. For example: if a stack consists of three dies and test access from external test equipment is exclusively possible via the stack I/Os which are concentrated in, say, Die 1, then Dies 1 and 2 need to cooperate in transporting test stimuli and responses up and down the stack in order to be able to test Die 3.

To enable separation of the test development as well as test execution for the various dies in the stack, the 3D-DfT architecture should enable modular testing, i.e., tests for dies and interconnect layers between adjacent stacked dies can be developed and executed individually. Several ad-hoc 3D-DfT architectures have been proposed, among others based on IEEE Std 1149.1, IEEE Std 1500, or on IEEE Std 1687. These architectures all have their specific strong and weak points. However, these ad-hoc 3D-DfT architectures do not inter-operate together. Hence, there is a need for a per-die 3D-DfT standard, such that if compliant dies (even if designed and developed by different teams or different companies) are brought together in a die stack, a basic minimum of test features should work across the stack. This is exactly the aim of IEEE Std 1838.

1.3 Scope of IEEE Std 1838

The aim of IEEE Std 1838 is to define at-die-level standardized and scalable 3D-DfT features, such that when compliant dies are stacked, a stack-level 3D-DfT test access architecture emerges with a minimum functionality and many optional extensions. IEEE Std 1838 provides a modular test access architecture, in which dies and interconnect layers between adjacent stacked dies can be tested individually. The focus of the standard is on testing the intra-die circuitry as well as the inter-die interconnects in pre-bond, mid-bond, and post-bond cases in pre-packaging, post-packaging, and board-level situations. The standard provides test access via a mandatory one-bit (‘serial’) input/output test port and optional multi-bit (‘parallel’) test ports.

The standard is die-centric, i.e., compliance to the standard pertains to a die (and not to a stack of dies). Standardized die-level DfT features comprise a stack-level test access architecture. In this way, the standard enables interoperability between die maker and stack maker.

The standard does not address stack-level challenges and solutions. The most prominent example of this is that the standard does not address compliance of the stack to IEEE Std 1149.1 Boundary Scan for board-level interconnect testing (although the standard certainly does not prohibit application thereof).

The current version of IEEE Std 1838 standardizes mandatory and optional on-chip hardware components for 3D test access. It is intended that in a future revision of this document to standardize a formal, computer-readable language in which implementation choices for the 3D-DfT hardware can be specified and described. The on-chip 3D-DfT hardware is based on and works with digital scan-based test access. The standard does not mandate specific defect or fault models, specific test generation methods, nor specific die-internal 2D-DfT features. IEEE Std 1838 leverages existing 2D-DfT wherever applicable and appropriate, including test access ports (such as in IEEE Std 1149.1), on-chip DfT such as internal scan chains and wrappers of embedded cores (such as in IEEE Std 1500), and on-chip design-for-debug and embedded instruments (such as in IEEE Std 1687). Stacking of dies requires that the vertical interconnects (micro-bumps and TSVs) are aligned with respect to footprint (i.e., matching .gds/layout locations), mechanical properties (i.e., matching materials, diameter, height, etc.), and electrical properties (i.e., matching driver/receiver pairs). As a generic DfT-only standard, IEEE Std 1838 does not govern these items. Similar to IEEE Std 1149.1 and IEEE Std 1500, it only defines a DfT architecture.
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Standard for Test Access Architecture for Three-Dimensional Stacked ICs

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1.4 Context

The Standard for Test Access Architecture for Three-Dimensional Stacked ICs is conceptually related to previously developed design-for-test (DFT) standards, in particular IEEE Std 1149.1, IEEE Std 1500, and IEEE Std 1687. The first two standards specify test access architectures for ICs on boards (IEEE Std 1149.1) and IP cores embedded within an IC (IEEE Std 1500). IEEE Std 1687 describes an access architecture to embedded instruments. These three previously developed standards have influenced and are referred to in this standard, so a solid understanding of these standards is strongly recommended.

1.5 Organization of the standard

Clause 1 provides an overview and context for this standard.
Clause 2 provides references necessary to understand this standard.
Clause 3 defines terminology and acronyms used in this standard.
Clause 4 is a tutorial that outlines the technologies addressed and utilized by this standard.
Clause 5 defines the serial access bus and structure which forms the mandatory basis of the standard.
Clause 6 specifies the construction of the mandatory die wrapper register.
Clause 7 defines the optional flexible parallel port: a mechanism to add a higher bandwidth channel to the die stack.

2. Normative references

The following referenced documents are indispensable for the application of this standard, document (i.e., they should be understood and used, so each referenced document is cited in text and its relationship to this document is explained). For dated references, only the edition cited applies. For undated references, the latest edition of the referenced document (including any amendments or corrigenda) applies.

1.1 IEEE Std 1149.1-2013 - IEEE Standard Test Access Port and Boundary-Scan Architecture
1.3 IEEE Std 1687-2014 - IEEE Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device

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3. Definitions, acronyms and abbreviations

3.1 Definitions

**Active:** When associated with a logic level (e.g., active-low), this term identifies the logic level to which a signal shall be set to cause the defined action to occur. When referring to an output driver (e.g., an active drive), this term describes the state in which the driver is capable of determining the voltage of the network to which it is connected.

**Active Functional Interface:** An active functional interface includes all of the terminals under test while using the DWR.

**Apply event:** A derivative event (in the sense that it is inferred from the operation of the other three events: Shift, Capture, and Update), whereby test data become active and effective as test stimuli. While the wrapper is in IF mode, the Apply event causes test data to be applied from input cells onto the internal die functional logic.

**Bidirectional terminal:** A die terminal that can either drive or receive signals from another die.

**Capture event:** An event whereby the value present on the CFI or CFO is stored in a storage element in the shift path.

**Capture mode:** The mode in which all required DWR cells apply the Capture Event. For instance, during an external test mode, only the DWR cells attached to die terminal inputs are required to capture, all other DWR cells can apply any event.

**Cell test input (CTI):** A DWR cell’s test data input.

**Cell test output (CTO):** A DWR cell’s test data output.

**Chip:** Active component typically mounted on a board or some other package with other components. The more general term “component” is normally used in this standard for a compliant object as there may be multiple integrated circuits in a package, even when they behave as a single object. Syn.: integrated circuit (IC).

**Chip-on-board testing:** A test of a component after it has been assembled onto a printed circuit board or other substrate. For example, the on-chip DIT features defined by this standard may be used.

**Clock:** A signal where transitions between the low and high logic levels (or vice versa) are used to indicate when a stored-state device, such as a flip-flop or latch, may perform an operation.

**Component:** An active or passive electronic part. For the sake of this standard, this usually refers to an integrated circuit, although it could include non-integrated-circuit devices mounted on a board. See also: chip.

**Control:** The process of applying test pattern stimuli.

**Core:** Predesigned circuit block that can be tested as an individual unit.

**Core test:** A test methodology that is applied to an embedded core.

**Dedicated shift path:** A shift path comprising storage elements that do not participate in functional operation.

**Dedicated wrapper (cell):** A wrapper style that does not share hardware with core functionality. This style allows certain test operations to occur concurrently and transparently during functional operation. This definition could apply to individual cells.

**Device under test:** The device under test (DUT) is the object that is currently tested. It can be a die, a core embedded in a die, the interconnects between two dies, etc.

**Die:** A die is a piece of a processed semiconductor that provides some functionality.

**Die-centric:** Focusing on the properties of the die, typically not a complete stack or system.
Die sequence: The first die in the stack is accessible to the outside world. The following dies are referred to as the second, third, etc. The sequence of the dies does not imply any orientation of the dies. A stack can have multiple dies that are last dies; this is called a multi-tower stack.

Die terminal: The physical connection point between dies or between the first die and the interposer or PCB.

Die wrapper register (DWR): The register surrounding the die for facilitating die test or die-to-die tests.

External safe state: A configuration of safe register values in which the outputs of a die are in a state that prevents them from interfering with a block of logic outside the die. See also internal safe state; safe state.

EXTEST: is a shortening of the two words external test.

External test: occurs when the DWR is used to test logic or interconnect external to the die while the DWR is in outward-facing mode. This may include logic on the die if the DWR cell is not at the die boundary.

Falling edge: A transition from a high to a low logic level. In positive logic, a change from logic 1 to logic 0. Events that are specified to occur on the rising (falling) edge of a signal should be completed within a fixed (frequency independent) delay specified by the component supplier.

First die: The first die is the die which is connected to the printed circuit board (PCB) or an equivalent carrier or interposer. It is typically the bottom die of the stack.

First die external-I/O: package-level connection to the board or system level.

Flexible parallel port (FPP): Optional multi-bit test access mechanism allowing test data and protocols to be transferred over a set of FPP lanes.

(FPP) channel: A set of identical FPP lanes controlled by common signals.

(FPP) clock lane: An FPP lane used to provide an FPP lane clock to registered FPP lanes.

FPP configuration element: A TAP-accessible TDR bit which controls the functionality and configuration of the FPP channels.

(FPP) lane: A collection of lane paths connecting: a primary interface terminal, a secondary interface terminal, die-level DFT, and/or other lanes.

(FPP) lane clock (signal): Clock signal used to drive registration within registered FPP lanes.

(FPP) lane path: A single-bit logical connection between a lane input terminal (source) and a lane output terminal (sink). This connection may contain sequential elements.

Fully-provisioned (cell): A DWR cell with full functionality, including capture, shift, and control features. In addition, it may have safe or update features.

Inactive: When referring to an output driver (e.g., an inactive drive), this term describes the state in which the driver is not capable of determining the voltage of the network to which it is connected.

Input cell: A DWR cell that is provided on a die.

Input pin: A component pin that receives signals from an external connection.

Instruction: A binary data word shifted serially into the test logic in order to define its subsequent operation.

Integrated circuit (IC): A collection of transistors, resistors, and capacitors and their interconnections constructed to perform specific functions on a single thin slice of a semiconductor crystal.

Internal safe state: A configuration of safe register values whereby a core is protected from the impact of a test outside the core. See also external safe state; safe state.

Interface: The collection of terminals connecting to another die or package substrate.

INTEST: is a shortening of the two words internal test.

Internal test: occurs when the DWR is used to test logic on the die while the DWR is in inward-facing mode.
Inward-facing (IF) mode: The test mode where core inputs are controlled by the DWR and core outputs are observed by the DWR.

Last compliant die: Die number \( k \) in a stack with \( n \) dies of which the first \( k \) dies are compliant with this standard \( (1 \leq k \leq n) \).

Last die: This is the last die in the stack. Last die refers to the logical position in the test hierarchy.

Least significant bit (LSB): The digit in a binary number representing the lowest numerical value. For shift registers, the bit located nearest to the serial output, or the first bit to be shifted out. The least significant bit of a binary word or shift-register is numbered 0.

Low: The lower of the two voltages used to convey a single bit of information. For positive logic, a logic 0.

Most significant bit (MSB): The digit in a binary number representing the greatest numerical value. For shift registers, the bit farthest from the serial output, or the last bit to be shifted out. Logic values expressed in binary form are shown with the most significant bit on the left.

Multi-tower stack: A system with a multi-tower design has a structure, where one base die is connected to two or more other dies or die stacks, where these dies or die stacks are not connected to each other.

No-connect: A system with a multi-tower design has a structure, where one base die is connected to two or more other dies or die stacks, where these dies or die stacks are not connected to each other.

Non-clock: A signal of the component, which is brought to an input-output pad of the die but not connected to a package pin due, for instance, to a constrained pin-count for the package.

Non-clock: A signal where the transitions between the low and high logic levels do not themselves cause operation of stored-state devices. The logic level is important only at the time of a transition on a clock signal.

Normal mode: The mode in which the DWR does not interfere with the functional operation of a wrapped die.

Observation: The process of monitoring pattern response.

Output cell: A DWR cell that is provided for a die output.

Output pin: A component pin that drives signals onto external connections.

Outward-facing (OF) mode: The test mode where wrapper functional outputs are controlled by the DWR and wrapper functional inputs are observed by the DWR.

Parallel configuration: Selected architecture of the DWR test logic wherein more than one serial input and serial output are used to access multiple DWR segments during the test.

Partially-provisioned (cell): DWR cell with less than the maximum functionality. It supports the Shift event and either the Capture event or the Apply event. In addition, it may have safe or update features. See also: fully-provisioned.

Pin: The point at which connection is made between the integrated circuit and the substrate on which it and other components are mounted (e.g., the printed circuit board). For packaged components, this would be the package pin; for components mounted directly on the substrate, this would be the bonding pad. The actual form of connection (bonding wire, landing pad, solder ball, or metal pin inserted into a via) is not material to the definition. See also: terminal.

Port: The connector which is accessible for a test. The access mechanism can be via a bond pad or BGA pad, a test pad and a probe, or a TSV which is connected to a TAM on another die.

Power-up reset: A reset of test or system logic that occurs when the power supply goes from OFF to ON. This can be achieved by design of latches that causes them to power up in a specific state, or by an ON-component or OFF-component circuit that generates an asynchronous reset signal that stays active for some nontrivial time after the power supply has reached its operating voltage. Synonym: power-on reset (POR).

Primary interface: The interface connecting towards the first die or to the package substrate.

Register: A set of typically contiguous or related storage elements.

Reset: The establishment of an initial logic condition that can be either logic 0 or logic 1, as determined by the context.
Rising edge: A transition from a low to a high logic level. In positive logic, a change from logic 0 to logic 1.

Events that are specified to occur on the rising (falling) edge of a signal should be completed within a fixed (frequency independent) delay, specified by the component supplier.

Sample: Action to capture the value of a signal at a specific moment in time, such as defined by a clock edge.

Safe data: Data that satisfy safe state configuration requirements. These data are user-defined.

Safe state: A property whereby a test of one block of logic is prevented from interfering with or damaging another block of logic. See also external safe state; internal safe state.

Scan design: A design technique that introduces shift-register paths into digital electronic circuitry, providing controllability and observability in deeply embedded regions of circuitry and thereby improving testability.

Scan path: The shift-register path through a circuit designed using the scan design technique.

Secondary interface: An interface connecting away from the first die or package substrate.

Segment: A set of contiguous (in terms of the scan chain) register bits obeying the rules for Test Data Registers and from which a Test Data Register may be assembled.

Segment insertion bit (SIB): A configuration of at least a shift and an update cell and a scan-multiplexor that is used to include or exclude a scan chain segment from the active scan path.

Selected test data register: A test data register is selected when it is required to operate as instructed by associated test logic.

Shared wrapper (cell): The wrapper style that shares logic between the test and functional modes of operation of a system storage element. This style prevents simultaneous functional and test operation uses of the shared storage element.

Shift event: An event whereby the data stored in the DWR shift path are advanced one storage position closer to the DWR’s TO. The data present at the DWR’s TI are loaded into the shift path storage element closest to the DWR’s TI. If multiple DWR segments are implemented, this definition applies individually to each DWR segment.

Shift mode: This mode occurs while the shift event is applied to all DWR cells with the intent of loading/unloading DWR scan chains.

StackID: A field in an ECID that describes the position of the die in the stack.

Stand-alone testing: A test of a component performed before it is assembled onto a board or other substrate, for example, using automatic test equipment (ATE).

Storage element: A bi-stable circuit element, such as a latch or a flip-flop, which retains state until certain enabling and/or clocking conditions are met that cause it to take on a new state.

Stuck-at fault: A failure in a logic circuit that causes a signal connection to be fixed at 0 or 1 regardless of the operation of the circuitry that drives it.


System logic: Any circuitry that is dedicated to realizing the non-test function of the component or is at the time of interest configured to achieve some aspect of the non-test function.

System pin: A component pin that feeds, or is fed from, the on-chip system logic and carries a digital signal. This term does not include analog signals, voltage references, or power sources.

System on chip (SoC): An entire system integrated on a single chip. It may include one or more cores with user-defined logic (UDL) integrated by the core user or system integrator.

Terminal: A terminal is a connection from one die to another. A terminal can be unidirectional or bidirectional. See also: pin.

Test access mechanism (TAM): A feature of a system-on-chip (SoC) design that enables the delivery of test data to and from dies, cores, or core wrappers.
Test access mechanism (TAM) harness: Die wrapper register (DWR) logic that enables the coupling of a TAM to cell test inputs (CTIs) and cell test outputs (CTOs).

Test input (TI): The serial test data input of a DWR segment.

Test logic: Any item of logic that is a dedicated part of the test logic architecture or is at the time of interest configured as part of the test logic architecture.

Test mode: The state of a component in which the component’s test logic interferes with the flow of signals to and from the system logic. In addition, the system logic may be controlled as needed to prevent an undesired response to system inputs, excessive heating, and so on.

Test output (TO): The serial test data output of a DWR segment.

Three-state pin: A component output pin where the drive may be either active or inactive (for example, at high impedance).

Through silicon via (TSV): A via that electrically connects the front side to the back-side of a (thinned-down) wafer substrate.

Top die: (Colloquial) the expression last die should be used.

Update: Transfer a logic value from the shift-register stage of a data register cell or an instruction register cell into the latched parallel output stage of the cell.

Update event: An optional event whereby data stored in a DWR cell’s shift path storage element is loaded into an off-shift-path storage element (e.g., update register).

Update register: The register used to prevent the outputs of a shift register from propagating to other circuitry during a Shift operation. After shifting is complete, the content of the associated shift register is parallel-loaded (updated) into the update register or otherwise applied.

User-defined logic (UDL): Logic added by the system chip integrator (i.e., not a reused design), as interface circuitry or part of the feature set that differentiates the system-on-chip (SoC) product.

Wrapper: A wrapper is a test access and isolation ring at the boundary of a test module, being either an embedded core or a stacked die. A wrapper is typically based on scannable flip-flops.

3.2 Acronyms and Abbreviations

ATE automatic test equipment
ATPG automatic test pattern generation
AUXCK auxiliary clock
Bidi short for bidirectional
BGA ball grid array (packaging style)
BIST built-in self-test
BSDL Boundary-Scan Description Language or a file containing BSDL statements
CFI cell functional input
CFO cell functional output
CMOS complementary metal-oxide semiconductor
CTI cell test input
CTO cell test output
DC direct current
DFI die functional input
<table>
<thead>
<tr>
<th></th>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>DFO</td>
<td>die functional output</td>
</tr>
<tr>
<td>2</td>
<td>DFT</td>
<td>design-for-test</td>
</tr>
<tr>
<td>3</td>
<td>DUT</td>
<td>device under test</td>
</tr>
<tr>
<td>4</td>
<td>DWR</td>
<td>die wrapper register</td>
</tr>
<tr>
<td>5</td>
<td>ECID</td>
<td>electronic chip identification (ID)</td>
</tr>
<tr>
<td>6</td>
<td>FPP</td>
<td>flexible parallel port</td>
</tr>
<tr>
<td>7</td>
<td>IC</td>
<td>integrated circuit</td>
</tr>
<tr>
<td>8</td>
<td>ICL</td>
<td>Instrument Connectivity Language</td>
</tr>
<tr>
<td>9</td>
<td>IF</td>
<td>inward facing</td>
</tr>
<tr>
<td>10</td>
<td>I/O</td>
<td>input/output</td>
</tr>
<tr>
<td>11</td>
<td>IP</td>
<td>intellectual property</td>
</tr>
<tr>
<td>12</td>
<td>LSB</td>
<td>least significant bit</td>
</tr>
<tr>
<td>13</td>
<td>MSB</td>
<td>most significant bit</td>
</tr>
<tr>
<td>14</td>
<td>OF</td>
<td>outward facing</td>
</tr>
<tr>
<td>15</td>
<td>PDL</td>
<td>Procedural Description Language or a file</td>
</tr>
<tr>
<td></td>
<td></td>
<td>containing PDL statements</td>
</tr>
<tr>
<td>16</td>
<td>PLL</td>
<td>phase-locked loop</td>
</tr>
<tr>
<td>17</td>
<td>POR</td>
<td>power-on reset</td>
</tr>
<tr>
<td>18</td>
<td>PTAP</td>
<td>primary test access port</td>
</tr>
<tr>
<td>19</td>
<td>SIB</td>
<td>segment insertion bit</td>
</tr>
<tr>
<td>20</td>
<td>SoC</td>
<td>system on chip</td>
</tr>
<tr>
<td>21</td>
<td>STAP</td>
<td>secondary test access port</td>
</tr>
<tr>
<td>22</td>
<td>TAM</td>
<td>test access mechanism</td>
</tr>
<tr>
<td>23</td>
<td>TAP</td>
<td>test access port</td>
</tr>
<tr>
<td>24</td>
<td>TCK</td>
<td>test clock</td>
</tr>
<tr>
<td>25</td>
<td>TDR</td>
<td>test data register</td>
</tr>
<tr>
<td>26</td>
<td>TI</td>
<td>test input</td>
</tr>
<tr>
<td>27</td>
<td>TO</td>
<td>test output</td>
</tr>
<tr>
<td>28</td>
<td>TSV</td>
<td>through silicon via</td>
</tr>
<tr>
<td>29</td>
<td>UDL</td>
<td>user-defined logic</td>
</tr>
<tr>
<td>30</td>
<td>WIR</td>
<td>wrapper instruction register</td>
</tr>
<tr>
<td>31</td>
<td>WRCK</td>
<td>wrapper clock</td>
</tr>
<tr>
<td>32</td>
<td>KGD</td>
<td>known good die</td>
</tr>
<tr>
<td>33</td>
<td>KGS</td>
<td>known good stack</td>
</tr>
</tbody>
</table>

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4. Technology

4.1 Stack Model

IEEE Std 1838 is defined at the logical level and abstracts from the physical implementation of the stack. To that end, it avoids terms such as ‘top’, ‘bottom’, ‘up’, and ‘down’ (which intuitively seem obvious terms to use in the context of vertical chip stacking). Instead, IEEE Std 1838 has adopted terminology based on the logical position of the interconnects relative to the external stack I/Os, which the standard assumes are concentrated in a single die, referred to as the first die. Relative to a die, the adjacent die connected in the direction of the external I/Os is referred to as the previous die; the collection of signals going to the previous die is referred to as the primary interface of this die. IEEE Std 1838 assumes that every die has a single primary interface, which connects to its unique previous die; an exception is the first die, for which its primary interface connects to the external system. Relative to the external stack I/Os, an adjacent die connected to this die in the opposite direction, (i.e., away from the external I/Os), is referred to as a next die; the collection of signals going to a next die is referred to as a secondary interface of this die. The idea is that pairs of primary and secondary interfaces form the interconnect between two stacked dies; the primary interface of one die plugs into the secondary interface of its previous die. A die can have zero or more secondary interfaces. A die with zero secondary interfaces is called a last die, whereas a die with one or more secondary interfaces that is not a first die is called a middle die.

![Diagram of Stack Implementations](image_url)

Figure 2: Three physically different implementations of a logically equivalent stack.

The stacks consist of three active dies. Die 1 holds all external I/Os as its primary interface and hence is the first die. The secondary interface of Die 1 connects to the primary interface of Die 2 and the secondary interface of Die 2 connects to the primary interface of Die 3. Hence, Die 2 is a middle die. Die 3 has no secondary interfaces and therefore is the last die in the stack. The stacks in Figure 2(a) and Figure 2(b) are both single-tower 3D stacks. In Figure 2(a), all dies are face-down (i.e., with the processed, active side down) and the external I/Os are implemented as interposer bumps at the bottom-side of the stack. Consequently, the primary interfaces are implemented at the bottom-side of each die and the secondary interfaces are implemented at the top-side of each die. In Figure 2(b), all dies are face-up and the external I/Os are implemented as wire-bonded pads at the top-side of the stack. As a result, in Figure 2(b), ‘up’ and ‘down’ are reversed in comparison to Figure 2(a); the primary interfaces are implemented at the top-side of each die.
and the secondary interfaces are implemented at the bottom-side of each die. The stack in Figure 2(c) is a 2.5D-SIC, with the three active dies stacked side-by-side on top of and interconnected by a passive interposer die. In this example, the primary and secondary interfaces of a die are both located on the same bottom-side of that die.

4.2 Wafer-level die access

When die are manufactured for stacking, micro-bumps are fabricated, perhaps on each side of the die, that form the interconnecting endpoints between each die in the stack. The size of these micro-bumps and the pitch (space between bumps) make physical contact to them for test purposes difficult. At the wafer level, only a single side of each die is likely to be contacted at all during manufacturing test phases. For these reasons, extra test pads (so called sacrificial pads) may be fabricated and used for test at the wafer levels.

Several proposals were discussed which outline methodologies to support die-level and stack-level test access “switching mechanisms”. Specifically, as mentioned, it is likely that physical access contacts at the die level may be different from stack-level access. This section will review some of these switching proposals. But it should be noted that none of these proposals were adopted by this standard. So, users are free to develop their own physical (and electrical) access structures to support their specific needs.

At the wafer level, it was noted that the physical contact area required for automatic test equipment (ATE) might be larger and farther apart when compared to the micro-bump size and pitch. When these sacrificial pads are used, the die needs to know how to route ATE signals. One such “switching mechanism” proposal, shown in Figure 3, defines a “die detector” which, based on the value of the selection signal, switches between the sacrificial pads and the micro-bumps. By default, the value of the “die detector” is pulled to ground.

Another proposal shown in Figure 4 uses the power rails to make this selection.
In this case, at the wafer level, the power supply rail would select the sacrificial pads. When the die is stacked, no power supply would be sourced via the sacrificial pads, so the internal TSV route would be taken.

4.3 Stacke

Once a die is stacked upon another die, access to one side of each die may disappear (considering the physical proportions of each die). This standard enables access to stack-level DFT resources through familiar serial and even parallel paths up and down the stack. Partial die stacks might still use the sacrificial pads in the early stages of the manufacturing process. Later, when larger contacts are available on the interposer of other substrate levels, the sacrificial pads may no longer be required or even accessible.

At different levels of integration, then, the driver of the signals supported by sacrificial pads might at one time be ATE probe pins, and at another time be a die in the stack. For this reason, a selection scheme may be necessary to select the driver source or disable a driver source to avoid signal interference with the test process. This selection might be made automatically (by a pull-up or pull-down, overridden by a connecting die) or using more manually or via software selection mechanisms. That being said, this standard will not recommend or standardize on such selection schemes. Such schemes may be simple and ad-hoc, but should otherwise not interfere with the architectures defined in this standard.

4.4 Physical attributes

In addition to the exclusions mentioned in the previous section, physical aspects of construction are also not addressed by this standard. It is assumed that any die stacked upon another die will have aligned micro-bumps and other physical geometries that allow such a prospect to occur. As such, it is likely that port directionality and other design attributes will also be shared amongst teams participating in building the stack so that their design goals can be met. But this standard will only focus on the logical design to enable interoperability between die in the stack and tools interfacing to the databases produced by such a flow and methodology.

5. Serial Test Access Ports

Each die is a separate logical plug-and-play entity enabling a three-dimensional (3D) chip to be assembled with test and debug features. Being a per-die standard, terminals and terminal behavior will be defined. The mating of terminals from one die within a 3D stack to the complementary terminals of an abutting die enables a contiguous test and debug access architecture that spans multiple die within the stack.

It should be noted, though, that this standard defines the functional, behavioral, and logical but not physical terminal connections – defining the physical location of terminals, pads or bumps and the sizing and pitch of physical connections is beyond the scope of this standard.
The goal of this section is to define the signals/terminals, terminal behavior, and associated logic associated with the serial access and control of test and debug features on each die, and how those features are extended by abutting, bonding, or otherwise connecting to other die.

The serial test and debug connections are the focus of this section. One subset of the Primary Test Interface shall be the Primary Serial Test Access Port (Serial TAP) that will contain the signals and internal die logic connections that are associated with the Primary Interface; and a subset of the Secondary Test Interface will be the one or more Secondary Test Access Ports (STAPs) that will contain the signals and internal die logic connections that are associated with the Secondary Interface. Note that the primary and secondary interfaces may also include an optional Flexible Parallel Port (FPP), which will be further discussed in Section 7.

Figure 5: Example of a stack comprised of two semiconductor dies.

5.1 Primary Test Access Port

In support of a per-die standard, the mandatory test interface and access to all on-die test and debug features is the serial Primary Test Access Port (PTAP). The (PTAP) is associated with the surface closest to the board connection or package interface and is represented by five die terminals: TCK, TMS, TDI, TDO and TRSTN.

5.1.1 Specifications

Rules:

a) Each compliant die shall have a serial test access port as part of its primary interface and it shall be referred to as the Primary Test Access Port (PTAP).

b) The PTAP shall consist of five signals named TCK, TMS, TDI, TDO and TRSTN.

c) The TCK (Test Clock) signal shall be a clock input signal that synchronizes test architecture operations and registers.

d) The signal presented at TMS (Test Mode Select) shall be sampled into the test logic on the rising edge of TCK.

e) The signal presented at TDI (Test Data Input) shall be sampled into the test logic on the rising edge of TCK.

f) Changes in the state of the signal driven through TDO (Test Data Output) shall occur only on the falling edge of either TCK or upon assertion of Reset*.

g) The TRSTN (Test Reset) signal shall be an asynchronous active-low control input signal which provides an asynchronous reset function to test registers defined by this standard.
The TCK, TMS, and TDI signals shall be driven from dedicated terminals.

j) The TRSTN signal for a first die shall be driven from either a dedicated terminal or logic providing a power-on-reset function (POR).

k) The TRSTN signal for a non-first die shall be driven from a dedicated terminal.

Recommendation:

l) The TRSTN signal for a first die should be driven from a dedicated terminal.

5.1.2 Description

The five die terminals represent the signals normally associated with a compliant IEEE Std 1149.1 interface – and in the case of an IEEE Std 1838 die used as a first die (i.e. a die nearest to the board attachment), the five die terminals may actually represent the IEEE Std 1149.1 TAP interface to the board connection if an IEEE Std 1149.1 compliance mandate is required (note that IEEE Std 1838 compliance does not require IEEE Std 1149.1 compliance – IEEE Std 1149.1 compliance is only mandated if there is a separate IEEE Std 1149.1 compliance imposed on the final chip). The five signals are: the input test clock, TCK, that synchronizes all test architecture registers; the test mode select, TMS, that provides the input control signal to the test controller finite-state-machine (FSM) that generates the operation protocol for all test architecture registers; the active-low test reset, TRSTN, that provides the input asynchronous reset signal that can be used to put all test architecture registers into a known default state; the serial test data input, TDI, that allows serial data to be delivered to test architecture data registers on the rising-edge of the TCK clock when the test controller FSM is in one of the shift states; and the serial test data output, TDO, that allows serial data from the test architecture data registers to be presented to the die interface on the falling-edge of the TCK clock when the test controller FSM is in one of the shift states.

TMS, TCK, TDI and TDO are connected to dedicated test terminals. For a first die, the TRSTN signal should be connected to a dedicated test terminal unless there is POR logic that can drive this signal.

5.2 Primary Test Access Port Controller

The PTAP signals drive the PTAP controller which is an IEEE Std 1149.1 compatible TAP Controller. The register architecture associated with the PTAP controller includes registration to support the 3D features that are required or optional in IEEE Std 1838.

5.2.1 Specifications

Rules:

a) The PTAP signals shall be connected to a PTAP controller and associated register architecture.

b) The PTAP controller shall operate in accordance with the sequence of operations defined by the IEEE Std 1149.1 TAP controller finite-state-machine based on the TMS input control signal and synchronized by the TCK input clock signal. (See Clause 6.1 of IEEE Std 1149.1-2013)

c) The PTAP controller register architecture shall contain an instruction register, a bypass register, and a die wrapper register.

d) The PTAP controller register architecture shall contain a secondary TAP (STAP) configuration register named 3D Configuration Register (3DCR, see Clause 5.5) if one or more STAPs are implemented on the die.

e) The test access controller register architecture shall contain a device identification register that shall operate in accordance with IEEE Std 1149.1-2013 as described in Clause 12 and Clause 8.13.

f) If a die position register field is included (see 5.2.1 recommendation h)), there shall be a field in the ECID called StackID.

g) The StackID value shall not be all 1s.
5.2.2 Description

Like the IEEE Std 1149.1 TAP, the PTAP can access any number of die-internal registers available in the stack. However, the PTAP controller register architecture shall, at a minimum, have the bypass register, one or more die wrapper register (DWR) segments, the 3DCR register, and all required instructions that support these registers.

The PTAP Controller operates in the same manner as the IEEE Std 1149.1 TAP controller described in Clause 6.1 of IEEE Std 1149.1-2013. Figure 6 shows the PTAP controller state diagram and names the states with hexadecimal numbering which coincides with the waveforms of the PTAP controller shown in Figure 7.

Note: The hexadecimal state numbering of the PTAP Controller shown here is for illustration purposes only. The actual state numbering of the PTAP controller is determined by the designer.

Figure 6: PTAP controller state machine diagram and state definitions
A secondary TAP configuration register called 3DCR should exist (see Clause 5.5) if one or more STAPs exist (see Clause 5.3).

The StackID numbering system is user-defined. The correlation between the die StackID value and the actual die should be maintained by the stack producer and/or user. The die provider should make their StackID fields wide enough to handle a unique value within a collection of die in a stack when the number of die will not be known when the individual die is fabricated.

### 5.3 Secondary Test Access Port (STAP)

The baseline IEEE Std 1149.1 architecture is extended to the secondary interface with the addition of Secondary Test Access Ports (STAPs) and their associated selection and configuration control logic. This control logic is composed of the STAP itself, and control from the Primary TAP Controller’s three-dimensional configuration register (3DCR, see 1.1). The Secondary Interface may support multiple STAPs, each with a mandated five-pin test interface enabling it to plug into a next die’s PTAP.
5.3.1 Specifications

Rules:

a) Each die shall have N selectable STAPs, one for each directly connected die.
   
   Note: N may be zero if the die does not support any next dies to be stacked.

b) Each STAP shall comprise the terminals named TDI_Sn, TDO_Sn, TMS_Sn, TCK_Sn, and TRSTN_Sn,
   
   where n represents the STAP number, where 0 < n ≤ N.

c) The TCK_Sn output terminal shall be driven from the PTAP TCK terminal with no added in-line
   
   registration or combinational gating logic.

d) The TRSTN_Sn output terminal shall be driven from the PTAP TRSTN signal with no added in-line
   
   registration or combinational gating logic.

e) The TMS_Sn output terminal, when driven by the PTAP TMS terminal, shall be driven without added
   
   in-line registration.

f) The TDI_Sn input terminal shall sample data on the rising-edge of TCK.

g) The TDO_Sn output terminal shall present new data on the falling-edge of TCK.

Permissions:

h) It is permitted to buffer signals driving the TCK_Sn, TMS_Sn and TRSTN_Sn terminals for drive

   strength.
5.3.2 Description

The TCK and TRSTN signals are delivered directly to the STAP, as is, except for some buffering (but no additional in-line registration is allowed). They should always be enabled to the next die whether or not the STAP is selected. The TMS, TDI, and TDO signals are only enabled to or from the next die when the STAP is selected. Each of these signals has at least one multiplexer or in-line gate delay as part of the handling process to enable the selection and deselection.

The STAP terminals drive terminals on the secondary interface of the current die that then connect to the PTAP terminals on the next die: TCK, TMS, and TRSTN, respectively. The STAP serial data terminals, the associated PTAP terminals on the next die: TCK_S, TMS_S, and TRSTN_S, outputs drive the associated PTAP terminals on the next die: TCK, TMS, and TRSTN, respectively. The STAP serial data terminals, the TDI_S output and the TDI_S input, are meant to, respectively, drive and receive the next die PTAP terminal counterparts, the TDI input and TDO output.

TDI_Sn and TDO_Sn also require registration, as they react on the rising or falling edge of TCK_Sn. TDI_Sn should sample data on the rising edge of TCK_Sn and TDO_Sn should present data on the falling edge of TCK_Sn.

5.4 Secondary Test Access Port Control Logic

The STAP Control Logic (or STAP, for short) consists of several sub-components: the selector and the retiming elements.

5.4.1 Specifications

Rules:

a) After a power-on-reset (POR), or when TRSTN is asserted, or upon entering the TLR state when persistence is disabled, all STAPs shall be deselected with the RTI_or_TLR_Sn signals configured to drive a logic-0.

NOTE – A logic 0 on RTI_or_TLR_Sn would cause die connected to the STAP to be held in the Run-Test-idle (RTI) state.

b) Each STAP shall be selectable using the corresponding Select_Sn signal from the 3DCR.

c) The Select_Sn signal shall change on the falling-edge of TCK in the Update-DR state.

d) When the Select_Sn signal is asserted, it shall enable the associated STAP to be selected between TDO_Sn and TDI_Sn.

e) The last STAP (numbered k) shall source TDO_Sk from TDI_Sk of the PTAP.

f) STAPs (n-k) shall source TDO_Sn from TDI_Sn+1 of STAPn+1.

g) If any STAPs are enabled (at least 1 Select_Sn is asserted) the PTAP shall source TDO from TDI_S1 of STAP1.

h) The last STAP (numbered k) shall connect TDI_Sk int from a point prior to the hold-time element (clocked by the rising edge of TCK) of the PTAP TDO.

i) TDO_Sn int shall be driven by a register element (clocked by the rising edge of TCK only in the ShiftDR and ShiftIR states) with data driven by TDI_Sn or TDI_Sn int.

j) TDO_Sn int shall be driven by a hold-time element (clocked by the falling edge of TCK) with data driven by TDI_Sn int.

k) When STAP_Sn is not selected (Select_Sn is 0), TMS_Sn shall be driven by RTI_or_TLR_Sn. (see section 1.3).

l) When STAP_Sn is selected (Select_Sn is 1), TMS_Sn shall be driven by TMS.

m) If no STAPs are selected (all Select_Sn signals are deasserted), PTAP shall source TDO from TDI_Sn int. (See Figure 10).
1) Shift register elements in the serial data path shall be clocked by the rising edge of TCK, and hold state in all but the ShiftDR and ShiftIR states.

Note – Shift register elements are supported by recommendations o) and p), and permission q).

Recommendations:

o) If required, extra shift register elements should be added along the serial data path between the PTAP TDI_Sn_int output and the STAP_Sn_TDI_Sn_int input.

p) If required, extra shift register elements should be added along the serial data path between the STAP_S1_TDO_S1_int output and the PTAP TDO_S1_int input.

Permissions:

q) If required, extra shift register elements may be added along the serial data paths within each STAP.

5.4.2 Description

At power-up, the STAPs are de-selected. Prior to being selected and activated, each STAP should be in a configuration that keeps its associated next die’s PTAP Controller parked in an idle state so that it processes no Capture, Shift, or Update operations. The default parked state is the Test-Logic-Reset (TLR) state, however, the STAP configuration register (3DCR) allows selection of the Run-Test-Idle (RTI) state.

To activate an STAP, the Select3DCR instruction is loaded into the PTAP Controller’s instruction register which selects the 3DCR. The 3DCR can then be configured and assert its new configuration on the falling-edge of TCK when the PTAP Controller is in the Update-DR state. De-activation requires a similar operation.

Registration within the STAP Control Logic block is required along the serial scan path through each STAP to maintain a negative-edge TCK register to present serial data to the TDO_Sn terminal that goes off-die and a positive-edge TCK register to sample serial data presented from off-die to the TDI_Sn terminal. These shift-only timing-adjust (resynchronizing) data bits are used in the scan data path to help ensure that the current shift data rate and TCK frequency is maintained.

Any of the STAPs may be active and included in the active scan path; or may be deselected and bypassed and not part of the active scan path.

Figure 9: STAP Control Logic.
The behavior of the STAP control terminals, when selected to be active, shall follow the port operations of the PTAP and shall be synchronized to the operation of the PTAP. However, when not selected, each STAP may be configured to operate the PTAP of the associated next die to be held in a parked state: Run-Test-Idle (RTI) or Test-Logic-Reset (TLR). The selected parking state depends on the state of the RTI or TLR Sn configuration bit for that numbered STAP within the STAP Configuration Register. The selection and parking requirement is accomplished by managing the TMS signal as it passes from the PTAP interface of the current die to the STAP interface on the same die (see the example in Figure 9).

When an STAP is selected, the PTAP TMS, is passed on to the STAP via TMS_Sn, with no modifications or registration. When an STAP is not selected, the TMS_Sn should be driven to logic-0 to hold the TAP FSM on the associated next die in a parked Run-Test-Idle (RTI) state or to a logic-1 if the parking state of the TAP FSM on the associated next die is desired to be Test-Logic-Reset (TLR). Note that selecting (un-parking) an STAP mandates a protocol sequence as follows: un-parking requires exiting the UpdateDR state directly to the RTI state.

The STAPs’ physical location in relation to each other may incur a large physical separation such that the actual terminals associated with the various TDI_Sn and TDO_Sn connections may be connected through long wire routes. Because of these possible impacts to shift-data timing, the positive timing adjust registers should not be isolated to only the secondary TDI_Sn ports returning from the connected die, but should exist in the main scan path between secondary serial test access ports themselves. Figure 9 shows a preferred configuration where the timing-adjust registers remain in the active scan path whether the secondary serial test access port is selected or deselected.

Since the path to the one or more STAPs include registration, IEEE Std 1149.1 compliance is difficult to maintain. For example, the BYPASS instruction datapath would include the bypass register and the STAP registration, as well, even when no STAPs are selected. For this reason, a short path is enabled upon power-up or assertion of the TRSTN pin. This path simply bypasses the STAP paths. This short-cut path is enabled until the user decides to enable an STAP pathway. So, other instructions (other than BYPASS, for example) will also enable this short path. In effect, the stack will actually resemble an IEEE Std 1149.1 compliant die until the user enables an STAP. Once an STAP is enabled, the short path is no longer used, and the STAP registration will be added to the serial data path. Figure 10 shows the decoding of the Select_Sn signals (through the OR gate) selecting the stack bypass path when no STAPs are selected.
Figure 10: The per-die PTAP and register architecture with signal connections for 3D extensions units and feature Config-Registers.

It should also be noted that some die could be targeted to be the very top or terminating die of a stack and would therefore not require a Secondary Interface – for this reason, the support of a STAP is designated as an option. The requirement is that a secondary interface may support zero to n Secondary Test Access Ports.

5.5 Registers

5.5.1 Secondary Test Access Port Configuration Register (3DCR)

5.5.1.1 Specifications

The 3DCR is the source of three basic types of signals:

1) the mandatory 3DCR Config-Hold signal, which resets to a deasserted state (logic 0), that makes STAP configuration bits and the STAP’s persistent through the Test-Logic-Reset action of the PTAP controller’s FSM;

2) the Select Sn signals, which reset to a deasserted state (logic 0), that select and activate the individual numbered STAP Sn and

3) the RTI or TLR Sn individual parking state definition signals, which reset to a logic 1 state (corresponding to the TLR state), that defines the parking state of the individually distributed TMS Sn signals associated with the individual numbered STAP Sn.

All of these signals are generated from a one-hot encoding (logic-1 equals assert) of the update bits, which are matched one-to-one with the shift bits in the 3DCR and have a specified order from the LSB to the MSB.
Architecture and the PTAP Controller

The STAP represents the processor interface to the secondary interface for use by the next die in the stack. This feature requires an STAP, so may not have a 3DCR.

5.5.1.2

Recommendations:

- The STAP should be selected and configured from the on-die IEEE Std 1838 PTAP Controller and Register Architecture and the PTAP Controller should remain in the active serial scan path with the requirement that

Rules:

a) Any die containing one or more STAPs shall have a 3DCR.

b) The 3DCR shall be designed as defined in Clause 9 of IEEE Std 1149.1-2013 describing capture-
deassertion actions of these signals occur on the falling edge of TCK in the
Update-DR state of the PTAP Controller.

c) Each 3DCR shift register element has an associated update element.

d) The 3DCR shall be selected as the active register in the scan path by the Select3DCR instruction.

e) The 3DCR shall have one selection bit (i.e.: Select_Sn) for each STAP.

f) The 3DCR shall have one TMS hold bit (i.e.: RTI_or_TLR_Sn) for each STAP.

g) When reset, each Select_Sn bit shall be set to a logic 0 value.

h) When reset, each RTI_or_TLR_Sn bit shall be set to a logic 1 value.

i) The 3DCR selection configuration bit (Select_Sn) shall be asserted with a logic 1 value.

j) Setting the 3DCR TMS hold bit for STAP_Sn to logic 0 shall drive STAP_Sn terminal TMS_Sn to
logic 0 when STAP_Sn is deselected.

k) Setting the 3DCR TMS hold bit for STAP_Sn to logic 1 shall drive STAP_Sn terminal TMS_Sn to
logic 1 when STAP_Sn is deselected.

l) The 3DCR shall have a Config-Hold bit (e.g.: ConfigHold_3DCR) as the least significant bit.

m) The 3DCR Config-Hold bit shall power-up in the deasserted state (i.e.: the “not holding” configuration).

n) The 3DCR Config-Hold bit shall be reset to its deasserted state when TRSTN is asserted.

o) When the 3DCR Config-Hold bit is deasserted, STAP controllers and associated 3DCR register bits
shall be reset when the PTAP controller enters the Test-Logic-Reset state.

p) When the 3DCR Config-Hold bit is asserted, STAP controllers and associated 3DCR register bits
shall not change state when the PTAP controller enters the Test-Logic-Reset state.

Recommendations:

q) The capture scan register of each 3DCR bit should capture the value of the update register of the
associated update element in the Capture-DR state.

NOTE – One of the reasons for the recommendation is to avoid having unknown data in the capture-
scan register transfer to the update register when entering the Update-DR state without passing
through the Shift-DR state.

5.5.1.2 Description

The STAP 3D Configuration Register (3DCR) is a register selected by an instruction encoding placed in the
PTAP controller instruction register. If there are no STAPs on the die, there is no need for a 3DCR
therefore, it is a dependent option that is mandated only if the die has at least one STAP. A last die does not
require an STAP, so may not have a 3DCR.

The STAP-3DCR provides a selection and configuration method to propagate the TAP signals associated
with the Primary Interface to the Secondary Interface for use by the next die in the stack. This feature
represents the process of passing data and control up and down, and to and from, the next die.
the source of the scan path to the STAP TDO signal (TDO_Sn) should be placed at a point after the register architecture of the PTAP register architecture (see TDI_S1_int in Figure 10).

When one or more STAPs are implemented and selected, the PTAP Controller may select any on-die data register. When the 3DCR is not the selected register in the scan path, it should hold its data state.

The 3DCR should have a reset-persistent configuration (Config-Hold), allowing the PTAP controller to pass through the Test-Logic-Reset (TLR) state without affecting the test function. Asserting TRSTN should then reset the 3DCR. Specific rules are defined to enable the Config-Hold function.

![Diagram of Example STAP Configuration Register (3DCR)](image)

**Figure 11: Example STAP Configuration Register (3DCR).**

shows a compliant 3DCR. The command bits of the STAP configuration register are organized in the configuration register beginning with the persistence command bit, ConfigHold_3DCR, at the scan-output end (the LSB). The select signals: the select bits, Select_Sn, and the hold state bits, RTI_or_TLR_Sn may be placed anywhere else in the register. The 3DCR is a data-persistent register that will hold its state when the 3DCR is not the selected active data register in the scan path. When the ConfigHold_3DCR bit is asserted, then the 3DCR becomes ‘reset persistent’, as well, in that the update bits that hold the Select_Sn, RTI_or_TLR_Sn, and the ConfigHold_3DCR values will not revert to a reset state when the PTAP Controller FSM passes through the TLR state. A TRSTN assertion will modify all the 3DCR register values, resetting them to their deasserted state.

### 5.5.2 Die Wrapper Register (DWR)

The Die Wrapper Register (DWR) is required in this standard and enables controllability and observability of the logic to and from die terminals for both INTTEST and EXTEST modes. There may be multiple modes for the DWR. There may also be multiple configurations of the DWR. The rules, recommendations and permissions for the DWR are described in Clause 6. Control of the modes and the configuration of the DWR is done using either IEEE Std 1838 instructions and/or descriptions with a language such as PDL, ICL, and supporting hardware such as SIBs.

#### 5.5.2.1 Specifications

**Rules:**

a) Each die shall have a DWR.

   Note – the DWR is further defined in Clause 6.
5.5.2.2 Description

The DWR can be built using different structures. For instance, it may use only IEEE Std 1838 DWR cells at the boundary of the die. It may reuse one or more segments of an IEEE Std 1500 WBR as part of the DWR. It may reuse the IEEE Std 1149.1 BSR as part of the DWR. It may contain SIBs in the path for local configuration capability.

5.5.3 Flexible Parallel Port Configuration Register

Another expansion of the IEEE Std 1149.1 two-dimensional architecture is the addition of a Flexible Parallel Port and associated Flexible Parallel Port configuration elements that are meant to select and configure the Flexible Parallel Port. This will be discussed and defined further in Clause 7.

5.5.4 ECID Register

Rules:

a) If the StackID is implemented per recommendation 5.2.1h), the ECID register and associated ECID CODE instruction as described by 1149.1-2013, Clause 13 and Clause 8.15, respectively, shall also be implemented.

5.5.5 Bypass Register

Rules:

a) There shall be a 1-bit Bypass register that is operated in accordance with IEEE Std 1149.1.

b) The all-zeros Instruction register opcode shall select the Bypass register between TDI and TDO and leave the device in normal operational (mission) mode.

c) Unused Instruction register opcodes should decode to selecting the Bypass register between TDI and TDO and leave the device in normal operational (mission) mode.

5.5.6 Instruction Register and Instructions

5.5.6.1 Specifications

Rules:

a) Each PTAP controller and register architecture shall include an instruction register.

b) There shall be one instruction, Select3DCR, to select the 3DCR for operation and to place it in the active scan path.

c) There shall be at least one instruction opcode called BYPASS that selects the Bypass register.

Recommendations:

d) If a DWR test mode can be controlled exclusively from the PTAP instruction register, then the instructions SelectDWR-EXTEST, SelectDWR-INTEST, and SelectDWR-TRANSPARENT should be used.

NOTE – Configuration elements, including SIB bits or distributed control elements, could select various DWR elements into the scan path. The instruction register may provide multiple instructions to select and operate the DWR in the various configurations instead of just these three SelectDWR instructions.
e) The 3DCR can be concatenated with any other register.

5.5.6.2 Description

Elements that need instruction (access) consideration are:

1) the optional 3D Configuration Register used to enable, configure, and render reset-persistent STAPs; and is mandated if STAPs are present,

2) the Die Wrapper Register (DWR),

3) the optional FPP configuration elements used to enable and configure FPP connections, and

4) the single bit Bypass Register.

For die with STAPs, there is a requirement to have an instruction, Select3DCR, to select, activate and place into the active scan path the configuration register, 3DCR, that enables and configures access to dies stacked above the current die.

Figure 12: Primary and secondary DWR segment concatenation

This standard provides access to DFT structures inside a die stack, but does not specifically mandate test functionality (for the most part). How this access to use is customizable. Figure 12 shows an example of Primary and Secondary Die Wrapper Register segments that may be selected as a whole (viewed as one contiguous register), perhaps using existing IEEE Std 1149.1 instructions such as EXTEST, INTEST, SAMPLE, and PRELOAD. Segments may also be configured into and out of the active scan path using in-line SIB elements or even elements not directly accessible in the active scan path. As an example, using the IEEE Std 1149.1 PRELOAD instruction, accessing the DWR or setting the DWR mode could be set up prior to taking these registers off-line for test purposes.

A more complex DWR may be composed of boundary-scan cells, wrapper elements from IEEE Std 1500 compliant cores, and individual IEEE Std 1838 compliant wrapper cells. Control of this complex DWR might come from the instruction loaded into the Instruction register, SIBs, scannable TDR bits, WIRs, or other serially accessible elements. These elements may, in turn, not be available in the fully composed DWR. So, accessing the DWR might take several scan operations and various configuration settings before the proper
content and test mode is established. But, in some cases, a single instruction such as SelectDWR-EXTEST, SelectDWR-INTEST, and SelectDWR-TRANSPARENT could be used.

Flexible Parallel Port configuration could also involve multiple scan operations to completely configure the optional channels for broadband access.

The Bypass register should be available to enable within the active scan path to quickly bypass the die while, perhaps, accessing other die in the stack using the IEEE Std 1149.1 Standard BYPASS instruction.

5.6 Configuration Elements

The DWR and FPP configuration elements specify the functionality and configuration of the DWR and FPP lanes.

5.6.1 Specifications

Rules:

a) Configuring elements shall be accessible by the TAP using one or more instruction encodings.

b) The configuration elements shall be designed in accordance with the rules in Clause 7.4.2 of IEEE Std 1149.1 describing capture-update test data registers (TDR).

c) The configuration element capture-scan and update registers shall be set to their reset value when TRSTN or POR is asserted.

d) If a configuration element has a Config-Hold function, and the Config-Hold bit is asserted, all configuration elements associated with that Config-Hold function shall not change when the PTAP FSM asserts RESET*.

e) There shall be a description in a machine-readable language of the control of the modes and configuration of the DWR, if a single instruction is not sufficient.

f) All cells which control register segmentation multiplexers (SIBs) shall include a shift, capture, and update capability; the update shall be with delay such that the output of the inline segment select cell does not change until at least one half TCK cycle after UPDATE-DR.

Recommendations:

g) SIB control registers should be placed after their corresponding segment selection multiplexer.

Permissions:

h) There may be a single instruction to configure the DWR.

i) There may be a single instruction to configure the FPP.

5.6.2 Description

The DWR segments and FPP lanes can have numerous settings to adjust their resources as appropriate for the tests being applied. These settings are controlled by test data registers accessible from the PTAP. These settings should be able to hold their state for as long as the test access is required, but will definitely be reset when TRSTN is asserted.

There should be a way to control the configuration and the modes of the DWR and FPP. The DWR and FPP is not required to have a configuration register such as the 3DCR, though it is allowed to do so. It can be configured through distributed control such as SIBs. If distributed control is used, then there should be a description of how to enable the distributed control for every possible mode and every possible configuration.

This should be described in a machine-readable language such as ICL and PDL.
The configuration elements for the DWR and FPP can be scattered throughout the serial network. SIB selection mechanisms might be placed to gate access to these configuring elements. When a SIB is used to gate the access, the select signal from the SIB will be used to block segment element upsets by turning off the control signals to that segment like Capture, Shift, and Update. This select signal will change with the Update timing. As such, the segment’s Update signal might be gated off too soon. A delay in the selection signal will solve this timing issue as described in rule f).

6. Die Wrapper Register

This standard mandates a serial test interface and supports an optional parallel test interface for accessing an IEEE Std 1838 compliant wrapped die. The serial mode of the Die Wrapper Register (DWR) incorporates a single chain composed of all DWR cells accessed by the IEEE Std 1838 serial test interface. The parallel mode of the DWR may make use of one or more IEEE Std 1838 wrapper chain segments, accessed by the FPP. Figure 13 shows the DWR in an IEEE Std 1838 serial test interface architecture.

The DWR is constructed of DWR cells, each of which may include four data terminals: cell functional input (CFI), cell functional output (CFO), cell test input (CTI), and cell test output (CTO).

Figure 13 shows the following:

— Die functional input terminals (DFIs) are connected to the CFI terminals of DWR cells provided for die functional input logic.

— CFO terminals of DWR cells provided for functional die inputs are connected to the corresponding functional logic.

— Functional die output logic is connected to the CFI terminals of corresponding DWR cells provided for that die functional output logic.

— The CFO terminals of DWR cells provided for die functional output logic are connected to corresponding die functional output terminals (DFOs).

Figure 13: Example of DWR in serial test interface configuration to be accessed from IEEE Std 1149.1 Test Access Port.

DFI and DFO are generic names for wrapped die terminals that are to be connected within a die stack. It is often the case that identical DWR cell types are used for wrapping both die input terminals and die output.
terminals. These DWR cells are connected differently and may receive different control signals (not shown).

The DWR shift path is formed by connecting the CTO terminal of one DWR cell to the CTI terminal of the next DWR cell in a daisy chain fashion. TI and TO are defined to be the scan input and scan output terminals of the DWR as a whole, as shown in Figure 13.

In Figure 14, an implementation of an IEEE Std 1838 DWR interface using two parallel scan chains is depicted. Although this figure shows all input terminals (DFI) placed on one scan chain and all output terminals (DFO) on a second scan chain, the IEEE Std 1838 parallel test interface is not limited to this configuration. In addition, although TCK is shown in both Figure 13 and Figure 14, IEEE Std 1838 does not mandate the use of TCK for clocking the wrapper cells. A different clock, i.e. a system clock, may be used although the TCK is required for serial wrapper access at the die wrapper level.

In Figure 13 and Figure 14, the DFI_k terminals are DFI terminals, while the DFO_k terminals are DFO terminals.

![Diagram of DWR in parallel test interface configuration to be accessed from the IEEE Std 1838 Flexible Parallel Port. DWR structure and operation.](image)

**6.1 General**

**6.1.1 Specifications**

**Rules:**

a) Every digital signal connected to a die terminal shall be provisioned with a fully-provisioned DWR cell, except for signals that cause data to be loaded into a sequential element or dedicated test signals specified in this standard.

Note: Examples of signals that cause data to be loaded into a sequential element include the clock of a flip-flop, the gate of a latch, and the asynchronous set or reset of either a flip-flop or a latch.

b) The DWR shall have at least one configuration in response to the state of the configuration registers, allowing serial access to and from all DWR cells between TI and TO and utilizing TCK as the clock.

c) Every wrapped terminal shall be uniquely associated with at least one DWR cell, except as exempted under permission 6.1.1u)

d) While a DWR or DWR segment is not selected, its UpdateDR signal shall not cause the output of the DWR cell with the update capability to change state.
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A selected DWR segment shall place all of its DWR cells between the TI and TO of the DWR during
Shift mode.

All DWR cells in a selected DWR segment shall support the shift event.

All DWR cells connected to an active functional interface shall be included in a selected DWR segment
during the associated test mode.

All DWR cells in selectable DWR segment combinations shall support a common shift frequency.

For DWR configurations mandated in this standard in which the DWR segment is accessed through the
TAP, the DWR segment clock shall be TCK during shift.

NOTE – This rule verifies that TAP-only access to DWR segments can shift using only TCK. Other
configurations defined by the user could use other clock sources.

The configuring elements of the DWR shall be accessible by the TAP using one or more instruction
encodings.

The DWR configuration elements shall be designed in accordance with the rules in Clause 7.4.2 of
IEEE Std 1149.1 describing capture-update test data registers (TDR).

NOTE – An example TDR is illustrated within IEEE Std 1149.1-2013 figure 9-6.

DWR configuration element capture-scan and update registers shall be set to their reset value when
TRSTN or POR is asserted.

Recommendations:

Every digital input signal connected to a die terminal exempted from wrapper cell insertion per rule
6.1.1a) should be provided with an alternate access mechanism for observability.

Every digital output signal connected to a die terminal exempted from wrapper cell insertion per rule
6.1.1a) should be provided with an alternate access mechanism for controllability.

NOTE – Care should be taken when adding DWR cells to test outputs so they don’t interfere with the
performance of an active test.

The primary and each secondary functional interface of the die should provide for separately selectable
DWR segments.

For DWR configurations mandated in this standard in which the DWR segment is accessed through the
TAP, the DWR segment clock should be TCK during the update event.

Any digital output terminal that has a possibility of connecting to an analog input terminal on another
die should be provisioned with a fully-provisioned DWR cell, and a three-state driver between the DWR
cell and the output terminal that is initially disabled in test mode and controlled by a fully-provisioned

Differential AC-coupled terminals should follow the boundary scan cell rules, recommendations and
permissions from IEEE Std 1149.6, Clause 6.

Permissions:

Primary or secondary port terminals connected to optional dedicated flexible parallel port lanes may
be provisioned with a DWR cell that does not interfere with the operation of the flexible parallel port.

Note – If so provisioned, any test mode that utilizes the FPP should not include wrapper cells in these
DWR configurations.

Any die terminal may be provisioned with a DWR cell, provided doing so does not alter the behavior
of standard instructions.

In a case in which a die input terminal is used solely as the source of data for an output terminal, a
single DWR cell may be shared between the input and the output terminals.

A die terminal may be provisioned with more than one DWR cell.

There may be combinational logic between the die terminal and the DWR cell.

The mode on a deselected DWR segment may be set to a normal or test mode.

An IEEE Std 1149.1 boundary scan cell may be shared as a DWR cell and used in the DWR scan
chain(s).
z) An IEEE Std 1500 wrapper cell may be shared as a DWR cell and used in the DWR scan chain(s) if it is compliant to all P1838 DWR cell rules.

aa) An auxiliary clock (AUXCLK) may be used for clock control of the DWR cells.

6.1.1 Description

Rule 6.1.1a), and Recommendations p), and q) define which terminals shall have a wrapper cell and the minimum requirement of those wrapper cells.

A shift path in a DWR cell is composed of one or more storage elements serially connected between CTI and CTO. The DWR should have a single, uniform shift path between its TI and TO to enable serial access. DWR structure rule 6.1.1b) supports this. Likewise, for the serial mode of the IEEE Std 1838 wrapper, a shift path is composed of the storage elements of all the cells in the DWR concatenated into a single serial path. While any DWR is selected, there should be at least one DWR cell between TI and TO.

Rule 6.1.1d) pertains to small set of die outputs per permission 6.2.1g). For example, die outputs equipped with output enable control may use DWR with update functionality. Likewise, signals known to be controlling important signals connected to other dies such as power control, clock gate control, reset, etc. may want to use the protection of update functionality. If the DWR segment in which the wrapper cell with update capability resides is not selected then the output of that wrapper cell cannot change, even if an UpdateDR occurs.

If the FPP has wrapper cells, the scan chain(s) should be separate from any other wrapper chains or internal scan chains. This allows separate modes for internal or external tests that use the FPP in its mission mode without enabling the FPP wrapper. There should also be a mode to enable access to the FPP wrapper, to allow for the interconnect test of the FPP.

If a primary or secondary functional interface is active during a test, there should be a selected DWR segment which attaches to all terminals, per rule 6.1.1g), and is selected between TI and TO. The selected DWR segment should be able to shift values through all DWR cells whether or not they are attached to die terminals. In addition, the DWR segment that contains the DWR cells connected to the active primary or secondary functional interface should be selected during that test.

Though Rule 6.1.1a) exempts the requirement of a fully-provisioned DWR cell from some types of signals, it is recommended that the input signals have the capability to be observed. For instance, an asynchronous reset is exempt from this rule as direct controllability may need to be enabled. However, there may still be a desire to observe whether the signal has been properly connected from another die. For this reason, it is recommended that observability be added to the terminal (i.e. partially-provisioned DWR cell). The output signals that are exempt from Rule 6.1.1a) should provide controllability to the neighboring die to prevent putting it into an unknown state or prevent it from being damaged.

There is a requirement that one configuration of the DWR is a single scan chain per rule 6.1.1b). However, it is recommended that each functional interface have its own DWR segment so that testing of each interface can be accomplished while using a shorter DWR scan chain. One area where this may be used is mid-bond stacking where a second die is bonded to the first die in a package. Before placing a third die on top of the second die, it may be desirable to test that the second die is properly connected. This can be done by just enabling the primary DWR segment of the second die and the secondary segment(s) of the first die, if these configuration options are available. This creates much shorter DWR scan chains than if the entire DWR is a single scan chain. However, EXTEST is likely a very short test and it is up to the die creator to decide whether this is a good configuration option to add to the DWR.

It is permissible to use a clock other than TCK to control the DWR cell during test when the DWR is selected.

This clock is called AUXCK in this standard. For instance, functional registers may be reused as DWR cells. These are called shared wrapper cells and the functional clock would be connected to these DWR cells. However, at least one configuration of the DWR should be implemented where TCK is used to clock all
DWR cells (see Rule 6.1.1b). This indicates that if AUXCK is used to clock a DWR cell in a selected DWR segment during a test, there should be a way to switch to TCK to clock that same DWR cell in a separate DWR configuration or mode. Typically, on-chip clock controllers provide a mux that chooses between a test clock and a functional clock and can be used to supply the required clock in different configurations. All timing interactions between TCK and AUXCK should be considered if permission if 6.1.1a) is employed.

If the DWR segment can only be accessed through the TAP, then the segment clock should be TCK. It is generally assumed and recommended that any update element in a DWR cell is clocked by TCK. However, there may be reasons to have the update element clocked by AUXCK, so this is allowed.

If the die under test contains a boundary scan register, the boundary scan register can be used as part of the DWR as it follows the rules of IEEE Std 1838 DWR cell.

If the die under test incorporates an IEEE Std 1500 WBR cell and it is connected to a die terminal, then it should follow all IEEE Std 1838 DWR cell rules. An IEEE Std 1500 cell that allows transfer is not compliant to IEEE Std 1838 so cannot be utilized on a die terminal that requires a fully-provisioned DWR cell or utilizes a partially-provisioned DWR cell. However, if the IEEE Std 1500 WBR cell with transfer is in the shift path of the DWR and not connected to a die terminal, then it can be included in the DWR scan chain to be used during shift only. If the IEEE Std 1500 WBR cell with transfer is connected to a die terminal, a dedicated DWR cell should be used instead of the WBR cell to communicate with that terminal during test.

6.2 DWR cell structure and operation

The DWR cell operation relies on the Shift, Capture, Update, and Apply events more fully defined in 6.3.1

6.2.1 Specifications

Rules:

a) Every DWR cell shall have at least one storage element connected between its CTI and CTO terminals.

b) Every fully-provisioned DWR cell shall have at least one storage element connected between its CFI and CFO terminals.

c) Every fully-provisioned DWR cell shall have a storage element provisioned for the purpose of servicing the Capture event and this element shall be in the shift path.

d) Every fully-provisioned DWR cell shall have a storage element provisioned for the purpose of servicing the Apply event.

e) A partially-provisioned DWR cell shall support the Shift event and either the Capture event to observe the CFI/CFO terminal or the Apply event to control the CFO terminal.

Recommendations:

f) Partially-provisioned DWR cells should be implemented on die terminals exempted from being wrapped per rule 6.1.1a)

Permissions:

g) Any DWR cell may have a storage element provisioned for servicing the Update event.

6.2.2 Description

DWR cell structure rules 6.2.1a and 6.2.1b provide for a minimal implementation consisting of a means to select test data or functional data as inputs to a shared storage element.
DWR cell structure rule 6.2.1(a) allows for multiple storage elements in the shift path in order to support test methodologies requiring the application of sequential patterns (e.g., path-delay, transition delay, piecewise functional).

DWR cell structure rule 6.2.1(c) requires that captured data enter the shift path of a cell at a storage element.

Unidirectional IEEE Std 1149.1 boundary-scan cells are usable as IEEE Std 1838 DWR cells. DWR cell structure permission 6.2.1(g) supports this.

The DWR cell is fully self-sufficient for the processing of a test so that, after shifting in test data and before shifting out test data, all data for the test are sourced from and/or sampled into one or more storage elements in the single cell, i.e., the terminals’ test needs are met solely by their respective DWR cells.

DWR cells on die terminals that need not be wrapped per rule 6.2.1(a) may have reduced functionality cells as described in recommendation 6.2.1(f). For instance, one may wish to have an observe-only cell on clocks as defined in rule 6.2.1(a) or other types of observe cells supporting the Shift or the Capture event in outward facing (OF) mode. If the die terminal provided with a reduced-functionality cell is a clock terminal and gets connected to the clock input of the reduced-functionality cell, then this clock would be considered an AUXCK and would have to follow AUXCK requirements and allow for proper operation of the DWR.

### 6.3 DWR operation events

An event is an uninterrupted, predefined sequence of one or more steps. Within the interval of the predefined sequence there may be a particular instant that characterizes the event, when the nominal action of the event occurs. This is referred to as the characteristic instant. Predefined events are Shift, Update, Capture, and Apply. Some events may overlap with others as indicated in permission 6.3.1(e). Events apply to the DWR as a whole.

#### 6.3.1 Specifications

While the wrapper is in OF mode, the Apply event causes test data to be applied from output cells onto DWR functional outputs. The test data are the data stored in the shift path storage element unless the Update event is supported, in which case the test data shall be the data in the DWR cell storage element loaded during the Update event.

#### Rules:

- a) The Shift mode shall not occur simultaneously with either Capture or Update events.
- b) While the DWR is selected, the DWR wrapper cell shall only change state in the presence of an event that it supports, such as Shift, Capture or Update.
- c) In the absence of an active edge from the clock or a reset state, DWR storage elements in a selected segment shall not change state.

#### Recommendations:

- d) While accessing TDRs, TCK should not cause a deselected TDR storage element to change state.

#### Permissions:

- e) Except where excluded by rule a), events may be discrete, simultaneous, or overlapping.

### 6.3.2 Description

During Shift mode, the shift event is applied to all DWR cells so that data is able to be loaded and unloaded from any active scan chain. During Shift mode, no other event, such as capture, is allowed to occur on any DWR cell in an active scan chain.
DWR events are enabled by the active edge of the DWR clock signal(s) (rising edge for Capture, Shift, and UpdateDR) as shown in Figure 6 and Figure 7. The DWR clock pulses or edges applied in the absence of active DWR control signals do not result in any event. This requirement comes from the need to enforce interoperability between various types of wrapper cells which are operated simultaneously. A generic wrapper cell services the shift, capture, and/or update events when, respectively, the IEEE Std 1838 TAP Controller output signals ShiftDR, CaptureDR, or UpdateDR are asserted, and holds state when none of these signals are asserted. However, IEEE Std 1838 also allows wrapper cells which do not implement an update stage and hence do not service the update event. Such a wrapper cell should be able to hold state whenever UpdateDR is asserted. IEEE Std 1838 also allows wrapper cells with a single control signal which, if asserted, allows the DWR cell to shift and if deasserted, allows the DWR cell to capture. This situation is common for shared wrapper cells with only a ShiftEnable signal connected to the multiplexer of a DWR storage element. Such a wrapper cell should be able to hold state whenever none of the control signals ShiftDR, CaptureDR, and UpdateDR is asserted or when UpdateDR is asserted while the DWR is selected.

DWR clock signal(s) may be held in a high or low state for arbitrarily long intervals without loss of DWR state.

The TCK signal should not cause TDR cells of unselected TDRs to change state. This will help ensure a known or safe state to the external or internal logic, if the TDR cell does not have a static output. For example, an unselected TDR holding the test mode of a core should not be disturbed while other TDRs in the die are accessed.

While a scan chain is in Shift mode, all active DWR segments should be shifting all internal DWR cells; in other words, every DWR cell in the aforementioned segments should be performing the Shift Event. However, during any other mode (e.g. Capture Mode) other than Shift mode, then different DWR cells may support different events. For instance, during a capture cycle while in INTEST, it may be preferable to leave all DWR cells that are attached to input terminals in the Shift Event. Since they are attached to inputs, they can only capture unknowns from the input terminals. Unknowns can grow the pattern size and prevent delay test on the cone of logic connected to the input terminals (after the DWR cell). Controlling the DWR in this manner may help to facilitate delay testing in IF mode, while isolating these inputs from the outside function logic paths. In this scenario, the DWR cells connected to input terminals would apply the shift event, while all output scan cells would apply the capture event. This is allowable under permission 6.3 (i.e).

6.4 DWR operation modes

A mode is a static condition or configuration of the DWR that exists in response to the state of the test mode control signals. This subclause describes the normal mode, the IF mode, the OF mode, and the Safe Operation mode.

6.4.1 Specifications

Permissions:

a) IF mode and OF mode may be operative at the same time.

b) Whereas the four modes defined in this subclause (i.e., normal, IF, OF, and nonhazardous) are applied homogeneously across the entire DWR, other modes may be defined in which the DWR cells respond on an individual basis.

6.5 DWR Normal operation mode

The normal mode is the mode in which the DWR does not interfere with the functional operation of the die.
6.5.1 Specifications

Rules:

a) While in normal mode, the DWR shall not interfere with the operation of the die or with the flow of signals to and from the die.

Permissions:

b) While in normal mode, the DWR may respond to the Capture or Shift events, provided that such response does not conflict with rule 6.5.1a)

6.6 DWR Inward facing (IF) operation mode

The IF mode is a test mode where die inputs are controlled by the DWR and die outputs are observed by the DWR.

6.6.1 Specifications

Rules:

a) While in IF mode, DWR cells provided for die inputs shall respond to Shift, Apply, and, if provisioned for them (permission 6.2.1g), the Update events.

b) While in IF mode, DWR cells provided for die outputs shall respond to the Capture and Shift events.

Recommendations:

c) While in IF mode, DWR cells provided for die outputs should present safe data at their CFO terminals (i.e., external safe state).

6.7 DWR Outward facing (OF) operation mode

The OF mode is a test mode where die outputs are controlled by the DWR and die inputs are observed by the DWR.

6.7.1 Specifications

Rules:

a) While in OF mode, DWR cells provided for die outputs shall respond to Shift, Apply, and, if provisioned for them (permission 6.2.1g), the Update events.

b) While in OF mode, DWR cells provided for die inputs shall respond to Capture and Shift.

Recommendations:

c) While in OF mode, DWR cells provided for die inputs should present safe data at their CFO terminals (i.e., internal safe state).

6.8 Safe Operation

The goal of Safe Operation is to ensure that entering or configuring a particular test mode does not affect the die or inter-die circuitry in a hazardous manner.
6.8.1 Specifications

Rules:

a) The control signals of three-state drivers for output and/or bidirectional terminals of a die shall be controlled by a fully-provisioned DWR cell.

b) During the DWR shift event, three-state drivers for output and/or bidirectional terminals of a die shall be controlled such that a persistent safe drive state is maintained on the associated die terminals.

c) If the update storage element of a DWR cell that controls a three-state driver is reset in the Test-Logic-Reset TAP state, it shall be reset to the state that will cause the connected three-state drive to be disabled.

Recommendations:

d) The design of DWR output terminals should allow the user to bring them to a safe state upon entering test mode.

e) If changing logic levels of the output terminal that is connected to an input terminal of an adjacent die can damage or cause inappropriate activity in that adjacent die, the DWR cell of that output terminal should have an update storage element or a safe gate to control the output data during test.

Permissions:

f) A DWR control cell may enable and disable one or more three-state drivers on die terminals.

6.8.2 Description

While configuring or entering a test mode, hazardous conditions (e.g. contention) on all ports should be avoided. Whenever there is a three-state driver, the control to that driver should be controllable so that during test mode a hazardous state does not occur on logic external to the die. In addition, there should be capability to observe logic connected to the control port of the three-state driver. For these reasons, a fully-provisioned wrapper cell should be attached to the control port of a three-state driver.

There shall be a persistent drive state on the control of a three-state driver during Shift mode to help ensure that the output of the three-state driver remains in a safe state no matter what value is shifted into the terminal’s wrapper cell. Disabling the three-state driver is one way to help ensure a safe state. Two options for delivering a persistent drive state on the control of a three-state driver are 1) a safe gate or 2) an update capability to the wrapper cell.

If an output terminal of a die that connects to an input terminal of an adjacent die can damage or cause inappropriate activity to the adjacent die, the terminal should output a safe value during the DWR shift event for both INTEST and EXTEST mode. In addition, during INTEST mode, a safe value should be output during the capture event. An example is an output terminal that connects to a bidirectional signal; if both dies enable the drive capability, there will be contention, which can damage the circuit. A second example is if the output terminal of one die can wake or put to sleep an adjacent die, there should be control to put the adjacent die in a stable mode during shift and capture events. In addition, control may need to be considered on the input terminal of the adjacent die for this type of signal.

6.9 Parallel access to the DWR

In addition to its mandatory serial wrapper access mechanism using the IEEE Std 1838 test access port (TAP), IEEE Std 1838 provides for an optional parallel wrapper access mechanism called the Flexible Parallel Port (FPP).

6.9.1 Specifications

Rules:
Each parallel configuration of DWR segments and the associated configuration registers (see Section 5.5.1) shall be setup and enabled by means of the die-level TAP.

Recommendations:

b) A selected DWR segment should have a scan chain length that is the same or close to the length of other scan chains that are selected simultaneously.

Permissions:

c) The test input (TI) and test output (TO) of each DWR segment may be connected to one of the following:
   — to the output or input, respectively, of another DWR segment,
   — to the output or input, respectively, of an FPP lane,
   — to a die-internal scan chain output or input, respectively.

d) There may be more than one parallel configuration of the DWR.

e) In a parallel configuration, the DWR may use serial control signals.

6.9.2 Description

The DWR should have a serial configuration, but may have multiple DWR segments for various reasons including to support any parallel configurations desired. Parallel configurations of the DWR allow the flexibility to access multiple short DWR segments simultaneously. After an appropriate IEEE Std 1838 instruction which enables access to the segmentation control infrastructure is input to the TAP controller, a parallel configuration of the DWR can be enabled in one of multiple ways (e.g. configuration register, segment select bit).

The flexibility in connectivity allows DWR segments that are controlled and/or observed external to the die under test to be connected via their test inputs and outputs to FPP or to internal scan chains. FPP data signals that are distinct from TAP signals are used for the DWR segments that require external control/observe during the application of a parallel test. TDI and TDO pins may be re-used for access to a DWR segment during parallel DWR configurations at the same time as the FPP. However, like other FPP resources, this DWR segment might not be accessible when the package is soldered to the PCB.

6.10 DWR cell naming

IEEE Std 1838 mandates a naming convention for DWR cells.

6.10.1 Specifications

Rules:

a) All IEEE Std 1838 DWR cell names shall match the following regular expression:

\[DW]/([D][W][C](_[S][F](S)(D)+)(N)?(_U)?(_O)?(_G?[01Z]?)?/. 

b) The first field shall be “DC” unless an existing IEEE Std 1500 WBR cell in the die is reused in the DWR as allowed by permission 6.10.1h), in which case the first field shall be “WC”.

c) The second field shall be one of the following:

1) “_SD” followed by a decimal integer indicating the number of shift path storage elements for a shift path with dedicated storage element(s), or

2) “_SF” followed by a decimal integer indicating the number of shift path storage elements for a shift path with functional storage element(s).

d) The third field shall be one of the following:
DWR cell structures are defined in a regular expression format to ease software tool automation. The regular expression defined in 6.10.1a allows for the identification of any IEEE Std 1838 DWR cell.

The naming of the various types of DWR cells shall be done in a descriptive, parsable method. Each cell type name shall begin with DC (DWR cell). This prefix is followed by a sequence of characters that describe the capabilities and structure of the cell. The information will indicate whether a particular storage element is shared or dedicated to wrapper operation, how many shift path storage elements exist, the existence and type of the optional update cell, and the existence of safe operation.

To support this, several fields will exist in the name in a specified order. Each field begins with an underscore.

1. The second field is mandatory and describes the nature and number of shift path storage elements. The first two characters of this field shall be “_S” (shift). The third character is either “D” (dedicated) or “F” (shared functional), followed by an integer indicating the number of shift path storage elements. This second field has the following regular expression format: /_S[DF][d+]/.

2. The third field is mandatory and describes the data capture source. The first two characters of this field shall be “_C” (capture). The third character of this field shall specify the origin of captured data: “I” (CFI), or “O” (CFO), followed by an integer indicating location of the capture site counting from CTI. In cases where the wrapper cell being described does not perform the capture function, both the third character and the following integer in this field should be replaced by “N” (none) to indicate that there is no origin for captured data and that the capture site does not exist. The regular expression matching this second field is /(_C([IO][d+]|N)?)|(_O)?)?/. The absence of this field indicates the absence of a capture site.

3. The fourth field is optional describing the nature of the update element. It is composed of two characters which are “_U” (update). Its regular expression format is /(_U)/>. The absence of this field indicates the absence of an update storage element.

4. The fifth field is optional indicating the presence or absence of an observe-only element. It is composed of two characters which are “_O” (observe). Its regular expression format is /(_O)/>. The absence of this field indicates the absence of an observe-only storage element.
The sixth field is optional indicating the presence or absence of safe data support in nonhazardous mode. It is composed of two characters "_G" (guarded data) followed by a 0, 1, or Z indicating the static value. Its regular expression format is /(_G[01Z])?/. 

### 6.11 DWR cell examples

Table 1 describes IEEE Std 1838 DWR cell example names, and a gallery of bubble diagrams depicting each example follows the table. The bubble diagrams used in these examples are defined in Annex A. It is understood that the means of data path selection shown in these bubble diagram figures is to be configured by the content of the WIR.

<table>
<thead>
<tr>
<th>Cell description</th>
<th>Name</th>
<th>Figure number</th>
</tr>
</thead>
<tbody>
<tr>
<td>One storage element shared with functional operation.</td>
<td>DC_SF1_CI1</td>
<td>Figure 15</td>
</tr>
<tr>
<td>One storage element shared with functional operation with a safe gate that outputs the 1.</td>
<td>DC_SF1_CI1_G</td>
<td>Figure 16</td>
</tr>
<tr>
<td>One dedicated shift path storage element capturing from CFO.</td>
<td>DC_SD1_CO1</td>
<td>Figure 16</td>
</tr>
<tr>
<td>Two dedicated shift path storage elements, capturing from CFI into the shift storage element closest to CTO (the 2nd storage element).</td>
<td>DC_SD2_CI2</td>
<td>Figure 18</td>
</tr>
<tr>
<td>One dedicated shift path storage element with an update storage element, capturing from CFI.</td>
<td>DC_SD1_CI1_U</td>
<td>Figure 19</td>
</tr>
<tr>
<td>One dedicated shift path storage element with an update storage element and a safe gate which outputs a 0, capturing from CFI.</td>
<td>DC_SD1_CI1_U_G0</td>
<td>Figure 20</td>
</tr>
<tr>
<td>A reduced-functionality cell with one dedicated shift path storage element performing an observe-only function, capturing from CFI.</td>
<td>DC_SD1_CI1_O</td>
<td>Figure 21</td>
</tr>
</tbody>
</table>


IEEE Std 1500: /(WC)((WH)((_S[DF]d+)(_C(I[IO])d+))(C)(IOB))((IO))N)(U)[(DF)](O)[(G[01Z])]!!. 

The DC_SF1_CI1 cell types have the least circuitry. As this cell services both normal operation and test operation, the two operations are likely mutually exclusive. Also, the CFO terminal toggles as data are shifted from CTI to CTO and when a capture occurs. DC_SF1_CI1_G may drive a safe value in addition to supporting the functionality described for DC_SF1_CI1. See Figure 16.
DC_SD1_CO1 has a dedicated shift path, and its CFO may toggle during Shift or Capture operations. However, compared to the DC_SD1_CI1 cell, the CFI to CFO connection has superior testability since more of the functional path is tested. See Figure 17.

The DC_SD2_CI2 cell has the capability to apply a sequential pattern for delay testing applications. See Figure 18.
Figure 18: DC_SD2_CI2 DWR cell

DC_SD1_CI1_U has a dedicated shift path and an update storage element. See Figure 19.

Figure 19: DC_SD1_CI1_U DWR cell

DC_SD1_CI1_U_G shows an example where in addition to the update cell, there is also a gated safe value as shown in Figure 20.
DC_SD1_CI1_O is an observe-only harnessing cell. This cell is to be used only in accordance with rule 6.2.1d) and recommendation 6.2.1f) See Figure 21.

6.12 Wrapper states

The Test-Logic-Reset state can be used to force the DWR logic into a state that enables functional operation of the die. The DWR is forced unconditionally to a Wrapper Disabled state when the Test-Logic-Reset state is entered. In Wrapper Disabled state, the DWR is inactive and functional operation of the die logic can continue unhindered. Test operations are performed while the DWR is in Wrapper Enabled state.

6.12.1 Specifications

Rules:

a) While in the Test-Logic-Reset state, the DWR shall be in Wrapper Disabled state.

b) While in the Test-Logic-Reset state, all DWR segments shall be deselected.
6.12.2 Description

Independent of the current state of a wrapper, this wrapper will enter Wrapper Disabled state when the TAP controller enters the Test-Logic-Reset state. The wrapper will remain in this state while the TAP controller is in this state. In the Wrapper Disabled state, the wrapper is forced to its inactive state. This is achieved by ensuring the DWR mode is set to functional mode by setting all configuration elements appropriately. This is the default state of the DWR configuration elements.

7. Flexible Parallel Port

The flexible parallel port (FPP) provides parallel test access to the die and stack under test.

The flexible parallel port can also be used to establish a connection between the primary interface, the secondary interface, and the core of functional logic on the die.

7.1 General introduction

7.1.1 Application of the flexible parallel port

The optional flexible parallel port (FPP) is intended for carrying arbitrary test data independent of the die wrapper, including clock and test control signals.

The configuration of the FPP can vary depending on the application. The FPP is composed of a set of lanes. Each lane implements a one-bit wide path. Lanes with identical properties and control may be grouped into channels.

7.1.2 Flexible parallel port connectivity

Figure 22: Die with primary and optionally secondary interface

Figure 22a) shows a die with only a primary interface. The die functional logic can be supplied with test data using the FPP connected to the primary interface.

Figure 22b) illustrates a channel connecting the primary interface to the secondary interface. In this case, the channel is used for transferring test data through the die. Multiple channels may exist in a die.

In Figure 23a), two channels are required because one channel is bidirectional whereas the other channel is unidirectional.

In Figure 23b), a channel originates from a set of primary interface terminals and connects to 2 secondary interface sets of terminals. The primary interface terminal for 2 lanes could even be the same, such that a broadcast set of connections could be created.
7.1.3 Interface connectivity

The purpose of the FPP is to enable parallel data flow between dies in the stack. In addition to the inter-die connection, it is also possible to connect the lanes with the core logic of the current die. A lane with the maximal connectivity is shown in Figure 24. In addition, lane-to-lane connections can be made, as illustrated.

A lane allows connections to system terminals, named as follows:

Figure 23: Different connection types

Figure 24: Example lane connectivity
Table 2: FPP Terminal Definitions

<table>
<thead>
<tr>
<th>Terminal</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPP_PRI</td>
<td>Input, Output, or Bidirectional; Connection to a die terminal closer to the PCB interface</td>
</tr>
<tr>
<td>FPP_SEC</td>
<td>Input, Output, or Bidirectional; Connection to a die terminal further away from the PCB interface</td>
</tr>
<tr>
<td>FPP_FROM_CORE</td>
<td>Input; Connection from the core of the die into the lane</td>
</tr>
<tr>
<td>FPP_TO_CORE</td>
<td>Output; Connection from the lane into the core of the die</td>
</tr>
<tr>
<td>FPP_FROM_SIDE</td>
<td>Input; Connection from the FPP_TO_SIDE terminal of another lane</td>
</tr>
<tr>
<td>FPP_TO_SIDE</td>
<td>Output; Connection to the FPP_FROM_SIDE terminal of another lane</td>
</tr>
<tr>
<td>FPP_CLK_OUT</td>
<td>Output; Connection terminal on a clock lane driving a lane clock signal</td>
</tr>
<tr>
<td>FPP_CLK_IN</td>
<td>Input; Connection terminal of a clock signal for registers contained within the lane</td>
</tr>
</tbody>
</table>

Connections to primary and secondary die terminals can be bidirectional. Table 3 provides possible paths between FPP terminals. An X in the table represents a valid path between an input terminal (Source) and an output terminal (Sink).

Table 3: Unidirectional Lane Connectivity

<table>
<thead>
<tr>
<th>Source</th>
<th>Sink</th>
<th>FPP_PRI</th>
<th>FPP_SEC</th>
<th>FPP_TO_CORE</th>
<th>FPP_TO_SIDE</th>
<th>FPP_CLK_OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPP_PRI</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FPP_SEC</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FPP_FROM_CORE</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
<tr>
<td>FPP_FROM_SIDE</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

A path describes the data flow from one input (source) terminal of a lane to one output (sink) terminal of a lane. There may be more than one path active in a lane at the same time. An input terminal can be the source for more than one path. The number of paths that are supported by a lane depends on the lane implementation. The number of simultaneously active paths and their functionality at a certain point in time depends on the settings of the FPP configuration elements.

7.2 FPP lane examples

The following schematics show example implementations for FPP lanes. The drivers on the primary or secondary interfaces should be able to enter a high impedance state for test reasons, in particular for testing before thinning. The FPP configuration elements are the source of the control signals. The control terminal names in the examples are chosen to describe their functionality; they are not part of the standard.
Figure 25: Bidirectional lane examples

Figure 25 provides two examples of a bidirectional lane. Figure 25a) is a variant supporting a connection to a die functional core signal via lane sink terminal FPP_TO_CORE and from a die functional core signal via lane source terminal FPP_FROM_CORE. If the lane does not support a connection to the core, Figure 25b) illustrates a potential implementation, showing only connections to the FPP_PRI and FPP_SEC bidirectional terminals.

Figure 26 shows the two possible lane implementations for a unidirectional connection, a) with and b) without a connection to the functional core logic of the die.

Figure 26: Unidirectional lane examples from primary to secondary port (up)

Figure 27 shows a similar set of examples, but going in the other direction.
7.3 Structure of the Flexible Parallel Port

7.3.1 Specifications

7.3.1.1 Top-Level

Rules:

a) A Flexible Parallel Port shall be composed of FPP lanes and/or FPP channels.

b) An FPP channel shall be composed of identical lanes with identical clocking and control.

c) FPP lane control terminals shall only be controlled by FPP configuration elements accessible via the PTAP.

d) If the FPP_PRI or FPP_SEC terminals share functional output ports of the die, the signal that controls the selection of the lane terminal shall be derived from FPP configuration elements and/or other signals sourced by FPP lanes.

Note: This rule defines how to share a functional port with an FPP lane terminal. Care should be taken to verify that the reset state of the FPP lane also enables the functional pathway.

Recommendations:

e) The connection from the FPP_PRI terminal to the primary port terminal should be driven by three-state drivers.

f) The connection from the FPP_SEC terminal to the secondary port terminal should be driven by three-state drivers.

Permissions:

g) Different channels may be driven by separate clock lanes.

h) A clock lane may drive more than one channel.

i) Combinational logic may be between the FPP configuration elements and the FPP lane control terminals.
The FPP_PRI and FPP_SEC terminals of each lane may be connected to functional ports of the die.

7.3.1.2 Lanes

Rules:

a) All lane terminals except FPP_PRI and FPP_SEC shall be unidirectional.
b) Lanes shall be defined as either registered or non-registered.
c) If a lane has an FPP_PRI terminal, it shall connect to a terminal of the primary interface of the die.
d) If a lane has an FPP_SEC terminal, it shall connect to a terminal of a secondary interface of the die.
e) If a lane has an FPP_TO_CORE terminal, it shall connect to circuitry on the same die outside of the FPP.
f) If a lane has an FPP_FROM_CORE terminal, it shall connect to circuitry on the same die outside of the FPP.
g) If a lane has an FPP_FROM_SIDE terminal, it shall connect to the FPP_TO_SIDE terminal of another lane.
h) If a lane has an FPP_TO_SIDE terminal, it shall connect to the FPP_FROM_SIDE terminal of another lane.
i) If the FPP_PRI terminal is bi-directional, it shall provide an output driver with a high-impedance state.
j) If the FPP_SEC terminal is bi-directional, it shall provide an output driver with a high-impedance state.
k) If the output driver of the FPP_PRI terminal of a lane can be set to a high-impedance state, then
   1) there shall be a dedicated lane control terminal which controls the high-impedance state,
   2) a signal derived from the FPP configuration elements shall control the enable of the output driver, and
   3) if the FPP configuration elements are reset, this signal shall select its high-impedance state.
l) If the output driver of the FPP_SEC terminal of a lane can be set to a high-impedance state, then
   1) there shall be a dedicated lane control terminal which controls the high-impedance state,
   2) a signal derived from the FPP configuration elements shall control the enable of the output driver, and
   3) if the FPP configuration elements are reset, this signal shall select its high-impedance state.
m) Each FPP lane shall be configurable into at least one FPP lane path.
n) An FPP lane sink shall be driven by only one selected source at a time.
o) If an FPP lane sink may be driven from multiple sources, then one or more FPP lane control terminals shall be provided which select one source.

Recommendations:

p) A lane specified as a clock lane should be dedicated for the purpose of sourcing a lane clock.
q) If the FPP_PRI terminal is unidirectional, it should provide an output driver with a high-impedance state.
r) If the FPP_SEC terminal is unidirectional, it should provide an output driver with a high-impedance state.

Permissions:

s) The FPP_PRI terminal may be unidirectional or bi-directional.
t) The FPP_SEC terminal may be unidirectional or bi-directional.
u) The design of the circuitry fed from the FPP_PRI and FPP_SEC terminals may be such that an undriven source produces a logical response identical to either the application of a logic 0 or a logic 1.
v) Each lane may be configurable into up to three FPP lane paths simultaneously.

w) Multiple FPP lanes may share a connection to the same source terminal.

NOTE – For example, the FPP_PRI terminals of two lanes could be connected to the same primary interface input terminal.

7.3.1.3 Registered lane

Rules:

a) A registered lane shall have at least one terminal with a unique name from each list of Sources and Sinks shown below:

1) Sources: FPP_PRI, FPP_FROM_CORE, FPP_FROM_SIDE, FPP_SEC

2) Sinks: FPP_SEC, FPP_TO_SIDE, FPP_TO_CORE, FPP_PRI.

b) A registered lane shall contain at least one pipeline register and at least one hold-time element.

c) Between the FPP_PRI and FPP_SEC terminals, if they both exist, shall be at least one pipeline register and one hold-time element.

NOTE – Permissions 7.3.1.3n) and 7.3.1.3o) indicate that these storage elements may be bypassable. In addition, these storage elements, though they may be different, should be between the two terminals in either direction.

d) In a registered lane, the FPP_CLK_IN input terminal shall be provided that connects a lane clock to the pipe-line registers and hold-time elements within the lane.

e) In a registered lane, pipe-line registers and hold-time elements shall be clocked by the lane clock.

f) If pipe-line registers are provided in the lane, then at least the first of these registers shall be clocked by the rising edge of the lane clock.

g) If a hold-time element is provided in the lane, it shall be clocked by the falling edge of the lane clock.

h) A hold-time element, if provided, shall be formed out of a single storage element, and shall be the last storage element prior to the FPP_PRI and/or the FPP_SEC and/or the FPP_TO_CORE and/or the FPP_TO_SIDE terminals.

i) If pipe-line registers within a lane are resettable, then an FPP lane control terminal, FPP_RESET, shall be provided that resets these registers.

j) The signal driving the FPP_RESET terminal shall be asserted upon resetting the Flexible Parallel Port configuration elements.

NOTE – This means that the pipe-line bits could follow the same resetting rules as the FPP configuration elements.

Recommendations:

k) In a registered lane, the lane clock should be provided by a dedicated clock lane via the primary interface.

Permissions:

l) A registered lane may connect its source and sink terminals in all cases where “X” is indicated in Table 4.

Table 4: Lane Connectivity

<table>
<thead>
<tr>
<th>Source</th>
<th>Sink</th>
<th>FPP_PRI</th>
<th>FPP_SEC</th>
<th>FPP_TO_CORE</th>
<th>FPP_TO_SIDE</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPP_PRI</td>
<td></td>
<td>X</td>
<td>X</td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>FPP_SEC</td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
</tbody>
</table>

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This is an unapproved IEEE Standards Draft, subject to change.
m) In a registered lane, the lane clock may be sourced from TCK.

n) In a registered lane, a mechanism may be implemented for bypassing the registration in that lane.

o) In a registered lane, a mechanism may be implemented for bypassing the hold-time element in that lane.

p) Registered lane paths may provide more than one pipe-line register bit per registered lane path.

q) Pipe-line register bits may be clocked by either the rising or falling edge of the lane clock except as noted in Rule 7.3.1.3f).

r) The FPP configuration elements may be equipped with a Config-Hold function which causes the elements not to revert to a default state when the test controller associated with the primary serial test interface synchronously enters the Test-Logic-Reset state.

NOTE – TRSTN is not asserted.

s) The FPP_RESET terminal may be driven by the RESET* signal from the PTAP controller.

7.3.1.4 Non-registered lane

Rules:

a) A non-registered lane shall have at least one terminal with a unique name from each list of Sources and Sinks shown below:

1) Sources: FPP_PRI, FPP_FROM_CORE, FPP_FROM_SIDE, FPP_SEC

2) Sinks: FPP_SEC, FPP_TO_SIDE, FPP_TO_CORE, FPP_PRI, FPP_CLK_OUT.

b) A non-registered lane shall not contain pipe-line registers or hold-time elements.

c) Non-registered lanes defined as clock lanes shall use the FPP_CLK_OUT terminal to generate a lane clock for the FPP_CLK_IN terminals of registered lanes.

Permissions:

d) A non-registered lane may connect its source and sink terminals in all cases where “X” is indicated in Table 5.

Table 5 Lane Connectivity

<table>
<thead>
<tr>
<th>Source</th>
<th>Sink</th>
<th>FPP_PRI</th>
<th>FPP_SEC</th>
<th>FPP_TO_CORE</th>
<th>FPP_TO_SIDE</th>
<th>FPP_CLK_OUT</th>
</tr>
</thead>
<tbody>
<tr>
<td>FPP_PRI</td>
<td></td>
<td>X</td>
<td>X</td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>FPP_SEC</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td>X</td>
</tr>
<tr>
<td>FPP_FROM_CORE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>X</td>
<td></td>
</tr>
<tr>
<td>FPP_FROM_SIDE</td>
<td></td>
<td></td>
<td>X</td>
<td></td>
<td></td>
<td>X</td>
</tr>
</tbody>
</table>

7.3.2 Description

The optional FPP may be composed of registered, non-registered, and clock lanes. The configuration of each of the lane elements is done with PTAP-accessible register bits (TDRs) that will hold their state as the FPP is being used to apply tests. The lanes, themselves, can each be controlled (if supported) to connect terminals on the primary, secondary, and core-level areas to each other. These pathways might be registered,
themselves, to enable higher-frequency data communications across them. If registered, a clock can be provided from various sources. But it is envisioned that a clock might be easily connected through a non-registered lane, so special clock terminal names were selected (FPP_CLK_IN and FPP_CLK_OUT). The registration can be bypassed if desired.

Due to wafer-level manufacturing requirements, it might be desirable to have connection to the primary and secondary interfaces be able to be set in a high-impedance state if the lane connection is an output or a bi-directional terminal.

7.4 Allocation of FPP configuration elements to the FPP lane control terminals

7.4.1 Specifications

Rules:

a) Each control terminal of each FPP lane shall be driven by one true or inverted bit of an FPP configuration element, or by a value derived from a combinational circuit driven by multiple FPP configuration elements.

Recommendations:

b) Each FPP configuration element should control only one FPP control terminal.

7.4.2 Description

The registers that configure the FPP can directly drive a lane configuration terminal (such as a multiplexer select or a tri-state enable signal). But, the bits can also be combined with some sort of combinational circuit to select the control function.

8. IEEE Std 1838 DWR relationship with other standards

As mentioned throughout this document, IEEE Std 1149.1 is leveraged for the serial control and datapath. The stack-level and die-level interface is specified with respect to the 5 TAP interface signals.

The PTAP controller and register architecture is based off of an IEEE Std 1149.1 TAP controller and register architecture. The instruction register addresses device-level registers to be placed in the TDI-to-TDO pathway.

The DWR is quite flexible in its construction. As such, an IEEE Std 1500 core wrapper could become part of its content. Selection of elements into and out of its construction at any given time could be accomplished with WIRs from the core, or SIBs (as described in IEEE Std 1687). As well, the construction of the DWR could be described by IEEE Std 1149.1 (BSDL), 1687 (ICL), or 1450.6 (CTL).

The flexibility of the DWR hardware can also extend to including boundary-scan register bits and segments as described in IEEE Std 1149.1 and by BSDL from that standard.

To describe the content of the stack, IEEE Std 1149.7 offers some HSDL language constructs. IEEE Std 1687 may also be leveraged to describe the hierarchy.

IEEE Std 1687 may also be able to use its ICL language to describe the serial pathway from the PTAP through the connected STAPs.

The optional FPP may be able to be described by IEEE Std 1450.6.
Annex A Bubble Diagrams

(informative)

In IEEE Std 1838, an attempt has been made to focus on architecture and remain neutral to implementation styles. In this spirit, a graphical vocabulary has been implemented to describe hardware behavior visually without describing the physical implementation of the hardware. Informally, diagrams drawn using these symbols have been called bubble diagrams because the much-used symbol for a storage element is a circle.

The symbols to describe behavior are few. In fact, there are only four as shown in Figure 29. The first is the symbol for a storage element, which is a circle. The second is a data path, which is represented as a line with an arrowhead indicating data flow direction. The third is a dataflow decision point, which is represented as a vertical line with no arrowhead. The fourth symbol is a connection point, represented as a small filled circle located at the junction of two data paths.

Figure 28: 3D die stack using 1838 compliant dies.

Figure 29: The four symbols used in bubble diagrams

The storage element has a characteristic associated with it that indicates the events to which it responds. This characteristic is displayed as the presence of one or more characters inside the circle from the set \( \{ S, C, U \} \).
and \( F_i \) indicating the Shift, Capture, Update, and any Functional event, respectively. Figure 30 shows various storage elements.

\[
\begin{array}{ccc}
S & SC & SCF \\
\end{array}
\]

Figure 30: Various storage elements

Shift data flows from CTI to CTO and can go through multiple storage elements represented by the bubbles. Capture data come into a storage element from the CFI terminal or the CFO terminal. Update data come from the shift path storage element. Functional data come from CFI.

To show how these elements are used together, an IEEE Std 1149.1 BC_1 cell using the IEEE Std 1500 cell notation is shown Figure 31. The BC_1 cell supports the Shift, Capture, Update, and Apply events. It should be noted that the Apply event is a virtual event, composed of other events or modes, and, therefore, is not specifically represented in these diagrams.

\[
\begin{array}{c}
\text{CTO} \\
\text{CFI} \\
\text{SC} \\
\text{U} \\
\text{CFO} \\
\end{array}
\]

Figure 31: Example of IEEE Std 1149.1 BC_1 or IEEE STD 1838 DC_SD1_CI1_U cell

Annex B Bibliography

(informative)

Readers unfamiliar with IEEE Std 1838 may find it helpful to study some of the following books and papers:

1. Erik Jan Marinissen, Jouke Verbree, and Mario Konijnenburg, ‘A Structured and Scalable Test Access Architecture for TSV-Based 3D Stacked ICs’, IEEE VLSI Test Symposium (VTS’10), Santa Cruz, California, USA, April 2010, pp. 269-274, DOI: 10.1109/VTS.2010.5469556

2. Erik Jan Marinissen, Chun-Chuan Chi, Jouke Verbree, and Mario Konijnenburg, ‘3D DfT Architecture for Pre-Bond and Post-Bond Testing’, IEEE Intl. 3D Systems Integration Conference (3DIC’10), Munich, Germany, November 2010, Paper 3B.1, DOI: 10.1109/3DIC.2010.5751450


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(JETTA), Special Issue on 3D-Testing, Volume 28, No. 1 (February 2012), pp. 73-92, DOI: 10.1007/s10836-011-5269-9


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Jean Durupt, Pascal Vivet, Jürgen Schlöffel, 'JTAG Supported 3D DfT Using Chiplet-Footprints for Testing Multi-Chips Active Interposer System', 21st IEEE European Test Symposium (ETS), Amsterdam, the Netherlands, May 2016, DOI: 10.1109/ETS.2016.7519310

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