Status Update of IEEE P1838

Erik Jan Marinissen
Working Group Chair
IMEC
Leuven, Belgium

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Working Group Vice-Chair
Synopsys
Hilton Head, SC, USA

3D-TEST Workshop 2011
Anaheim, California – September 22+23, 2011

Presentation Outline

1. History
2. Organization
3. PAR
4. To-the-Point Please
5. Today in Your Working Group
6. Conclusion

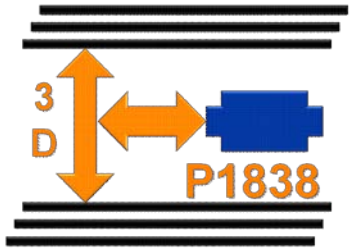
3D-Test Standardization Study Group

- Active January 2010,
  initiated by Erik Jan Marinissen (IMEC)
- Charter:
  inventory need for and timeliness of
  standards in 3D test and DfT
- ~60 members, weekly WebEx conference calls
  (hosted by Cisco Systems)
- Regular status updates: VTS'10, ETS'10, ITC'10

TTSC
Standardization
Study Group
on
3D Test

- Formulated Project Authorization Request P1838:
  *"Standard for Test Access Architecture for
  Three-Dimensional Stacked Integrated Circuits"*
  - PAR submitted to IEEE-SA NesCom : November 23, 2010
  - PAR approved : February 2, 2011

3D-Test Working Group



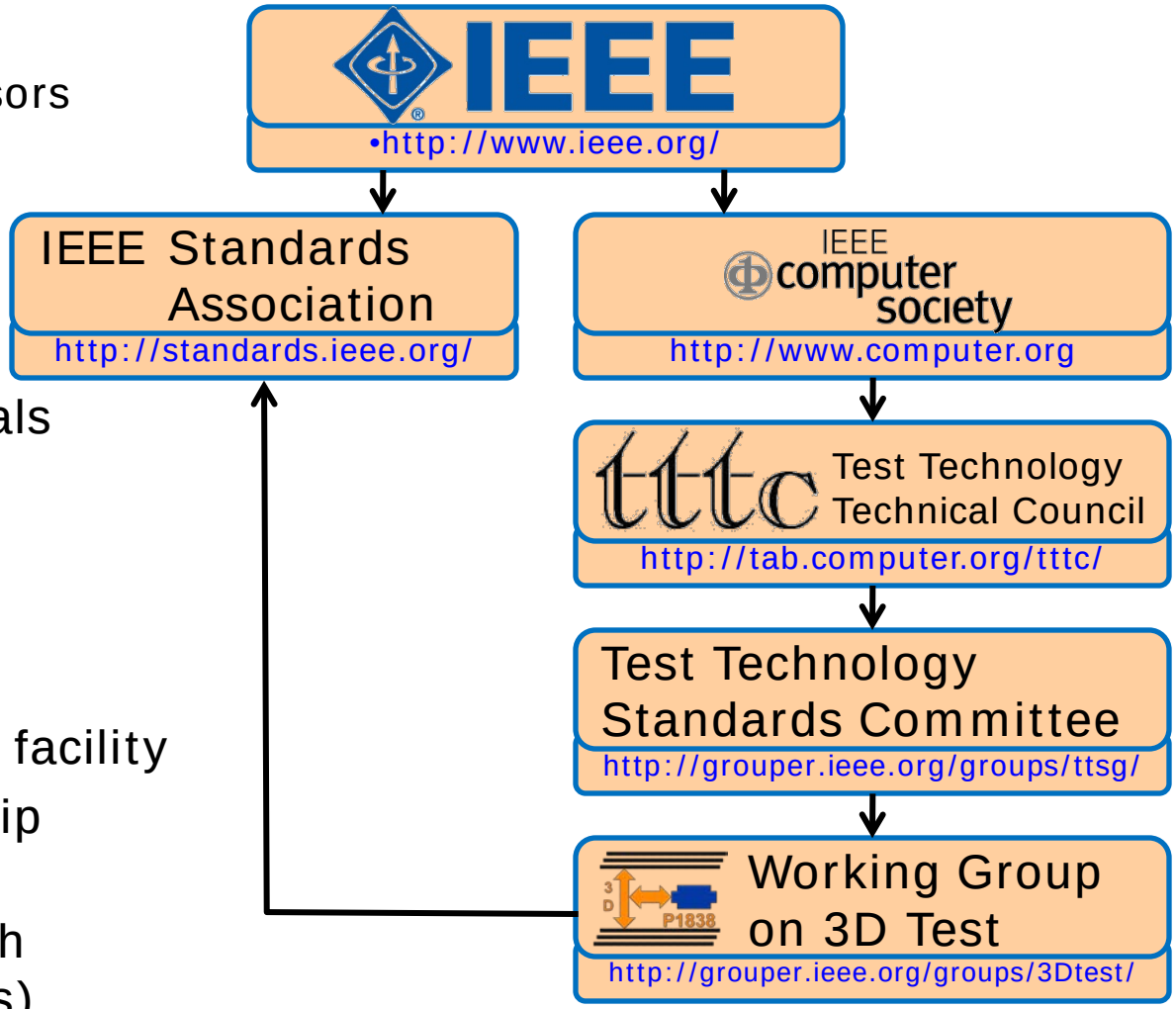
- Active February 2011, after approval of PAR P1838

- Charter:
  define standards in 3D test and DfT

- Current project:
  - P1838: *"Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits"*

Embedding in IEEE Organization

- **IEEE** sponsors
  Computer Society sponsors
  TTTC sponsors
  TTSC sponsors
  WG on 3D-Test
- **WG Membership**
  - Open to professionals
  - No dues or fees
- **IEEE-SA**
  - Provides facilities
    - Web hosting
    - E-mail reflector facility
  - IEEE-SA membership required for ballot
  - Will own and publish resulting standard(s)



WG Leadership and Officers

- **Chair** : Erik Jan Marinissen (IMEC)
- **Vice-Chair** : Adam Cron (Synopsys)
- **Secretary** : Sophocles Metsis (AMD)
- **Co-Editor** : Al Crouch (Asset-Intertech)
- **Co-Editor** : Michael Wahl (University of Siegen)
- **Web-Masters** : Saman Adham (TSMC), Erik Jan Marinissen (IMEC)

- **WebEx Hosts** : Ted Eaton; Bill Eklow, Hongshin Jun (Cisco Systems)

2. Organization

Working Group Members*

Saman Adham
Sandeep Bhatia
Sudipta Bhawmik
Craig Bullock
Tapan Chakraborty
Vincent Chalendard
Sangeetha Chellappa
Ji-Jan Chen
Chen-An Chen
Vivek Chickermane
CJ Clark
Zoe Conroy
Eric Cormack
Adam Cron
Al Crouch
Ted Eaton
Heiko Ehrenberg
Bill Eklow
Paul Emmett
Sandeep K. Goel
Michelangelo Grosso
Ruifeng Guo
Michael Higgins
Chun-Lung Hsu
Hongshin Jun
Stephane Lecomte
Prasad Mantri
Arie Margulis
Erik Jan Marinissen
Cedric Mayor
Teresa McLaurin
Sankaran Menon
Harrison Miles
Sophocles Metsis
Suriyaprakash Natarajan
Jay Orbon
Ken Parker
John Potter
Bill Price
Joseph Reynick
Mike Ricchetti
Ben Rogel
Arani Sinha
Roger Sowada
Craig Stephan
Brian Turmell
Manuel Umlauf
Michael Wahl
Min-Jer Wang
Lee Whetsel

+ 34× “followers”

* status 2011/08/27

2. Organization

3D-Test WG Participating Companies

2. Organization

Operation

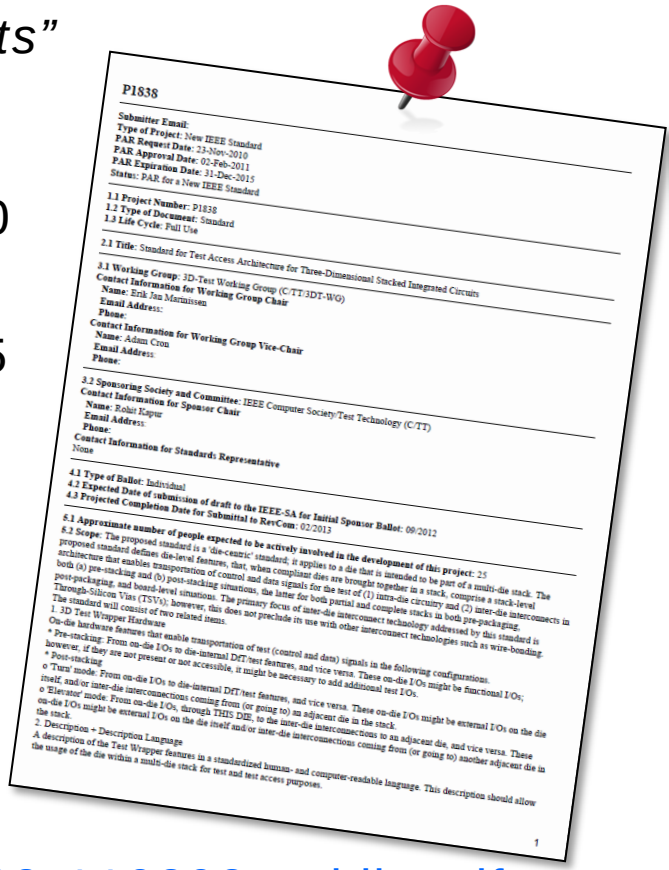
- **Communication**
  - Public websites:
    - 3D-Test WG : http://grouper.ieee.org/groups/3Dtest/
    - Project P1838: http://grouper.ieee.org/groups/1838/
  - Private web site and e-mail reflector for internal communication

- **Meetings**
  - Weekly conference calls: Thursdays 5-6pm Europe / 8-9am Pacific
    Kindly hosted by Cisco Systems
  - Ad-hoc face-to-face meetings (e.g., here at ITC'11)

Project Authorization Request (PAR)

- **Title**
  "Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits"

- **Dates**
  - PAR request date : November 23, 2010
  - PAR approval date : February 2, 2011
  - PAR expiration date : December 31, 2015
  - Expected initial sponsor ballot : 09/2012
  - Projected completion date : 02/2013



P1838

Submitter Email:
Type of Project: New IEEE Standard
PAR Request Date: 23-Nov-2010
PAR Approval Date: 02-Feb-2011
PAR Expiration Date: 31-Dec-2015
Status: PAR for a New IEEE Standard

1.1 Project Number: P1838
1.2 Type of Document: Standard
1.3 Life Cycle: Full Use

2.1 Title: Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits

3.1 Working Group: 3D-Test Working Group (C/TT/3DT-WG)
Contact Information for Working Group Chair
Name: Erik Jan Marinissen
Email Address:
Phone:
Contact Information for Working Group Vice-Chair
Name: Adam Cron
Email Address:
Phone:

3.2 Sponsoring Society and Committee: IEEE Computer Society/Test Technology (C/TT)
Contact Information for Sponsor Chair
Name: Rohit Kapur
Email Address:
Phone:
Contact Information for Standards Representative
None

4.1 Type of Ballot: Individual
4.2 Expected Date of submission of draft to the IEEE-SA for Initial Sponsor Ballot: 09/2012
4.3 Projected Completion Date for Submittal to RevCom: 02/2013

5.1 Approximate number of people expected to be actively involved in the development of this project: 25
5.2 Scope: The proposed standard is a 'die-centric' standard, it applies to a die that is intended to be part of a multi-die stack. The proposed standard defines die-level features, that, when compliant dies are brought together in a stack, comprise a stack-level architecture that enables transportation of control and data signals for the test of (1) intra-die circuitry and (2) inter-die interconnects in both (a) pre-stacking and (b) post-stacking situations, the latter for both partial and complete stacks in both pre-packaging, post-packaging, and board-level situations. The primary focus of inter-die interconnect technology addressed by this standard is Through-Silicon Vias (TSV); however, this does not preclude its use with other interconnect technologies such as wire-bonding. The standard will consist of two related items.
1. 3D Test Wrapper Hardware
On-die hardware features that enable transportation of test (control and data) signals in the following configurations.
* Pre-stacking: From on-die I/Os to die-internal DfT/test features, and vice versa. These on-die I/Os might be functional I/Os; however, if they are not present or not accessible, it might be necessary to add additional test I/Os.
* Post-stacking
o 'Turn' mode: From on-die I/Os to die-internal DfT/test features, and vice versa. These on-die I/Os might be external I/Os on the die itself, and/or inter-die interconnections coming from (or going to) an adjacent die in the stack.
o 'Elevator' mode: From on-die I/Os, through THIS DIE, to the inter-die interconnections to an adjacent die, and vice versa. These on-die I/Os might be external I/Os on the die itself and/or inter-die interconnections coming from (or going to) another adjacent die in the stack.
2. Description + Description Language
A description of the Test Wrapper features in a standardized human- and computer-readable language. This description should allow the usage of the die within a multi-die stack for test and test access purposes.

1

- **PAR On-Line:**
  http://grouper.ieee.org/groups/1838/PAR1838-110202-public.pdf

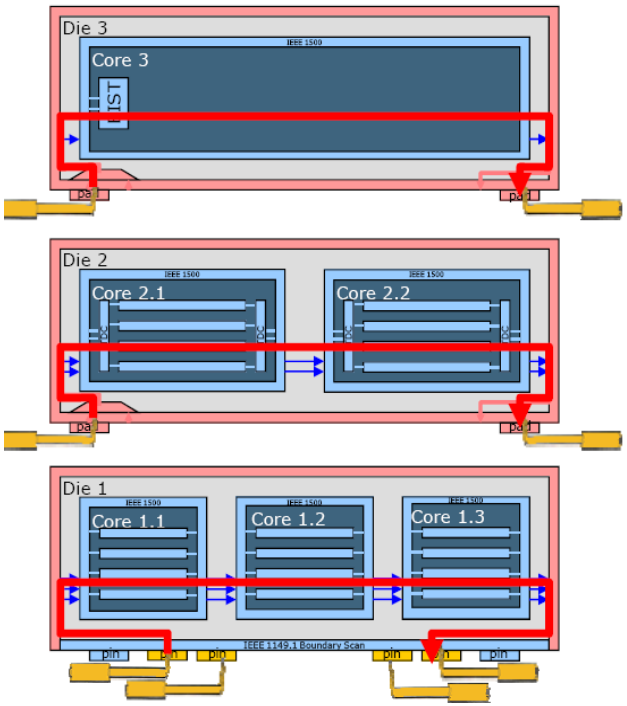
PAR Summary – 1/2

- **Focus**
  - Generic test access to and between dies in a multi-die stack
  - Prime focus on stacks with TSV-based interconnects
- **Test**
  - Pre-bond, mid-bond (partial stack), post-bond (complete stack)
  - Intra-die circuitry and inter-die interconnects
  - Pre-packaging, post-packaging, board-level situations
- **Die-Centric Standard**
  - Die-level features comprise a stack-level architecture
    - Compliance to standard pertains to a die (not to the stack)
    - Enables interoperability between Die and Stack Maker(s)
  - Standard does *not* address stack/product-level challenges/solutions
    - E.g. Boundary Scan for board-level interconnect testing
    - However, standard should not prohibit application thereof

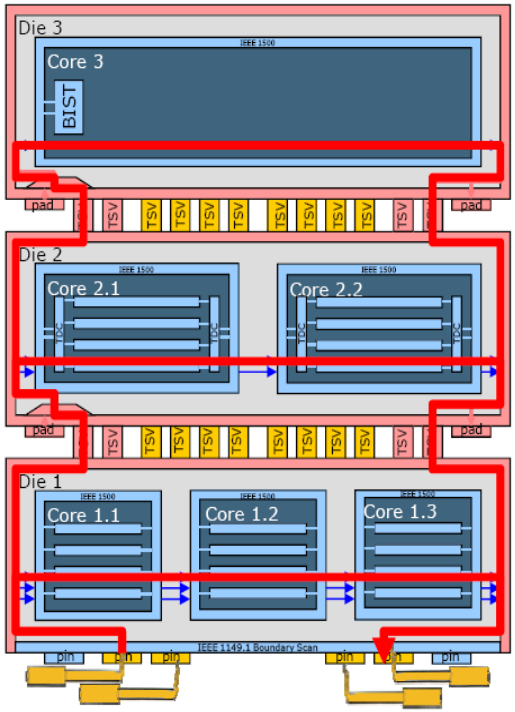
PAR Summary – 2/2

- **Two Standardized Components**
  1. 3D Test Wrapper hardware per die
  2. Description + description language
- **Scan-Based**
  - Based on and works with digital scan-based test access
- **Leverage Existing DfT Wherever Applicable/Appropriate**
  - Test access ports (such as IEEE 1149.x)
  - On-die design-for-test (such as IEEE 1500)
  - On-die design-for-debug (such as IEEE P1687)
- **Standard does *not* mandate**
  - Specific defect or fault models
  - Test generation methods
  - Die-internal design-for-test

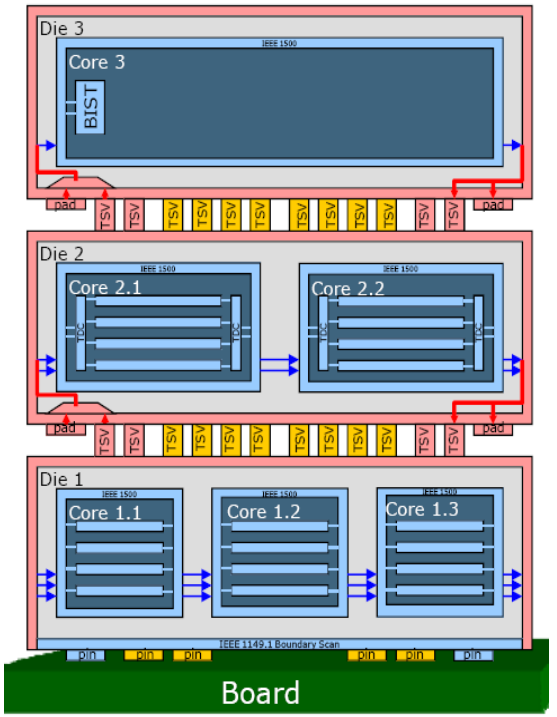
A Glimpse Of What We Are Thinking Of…



Pre-Bond
- Die test



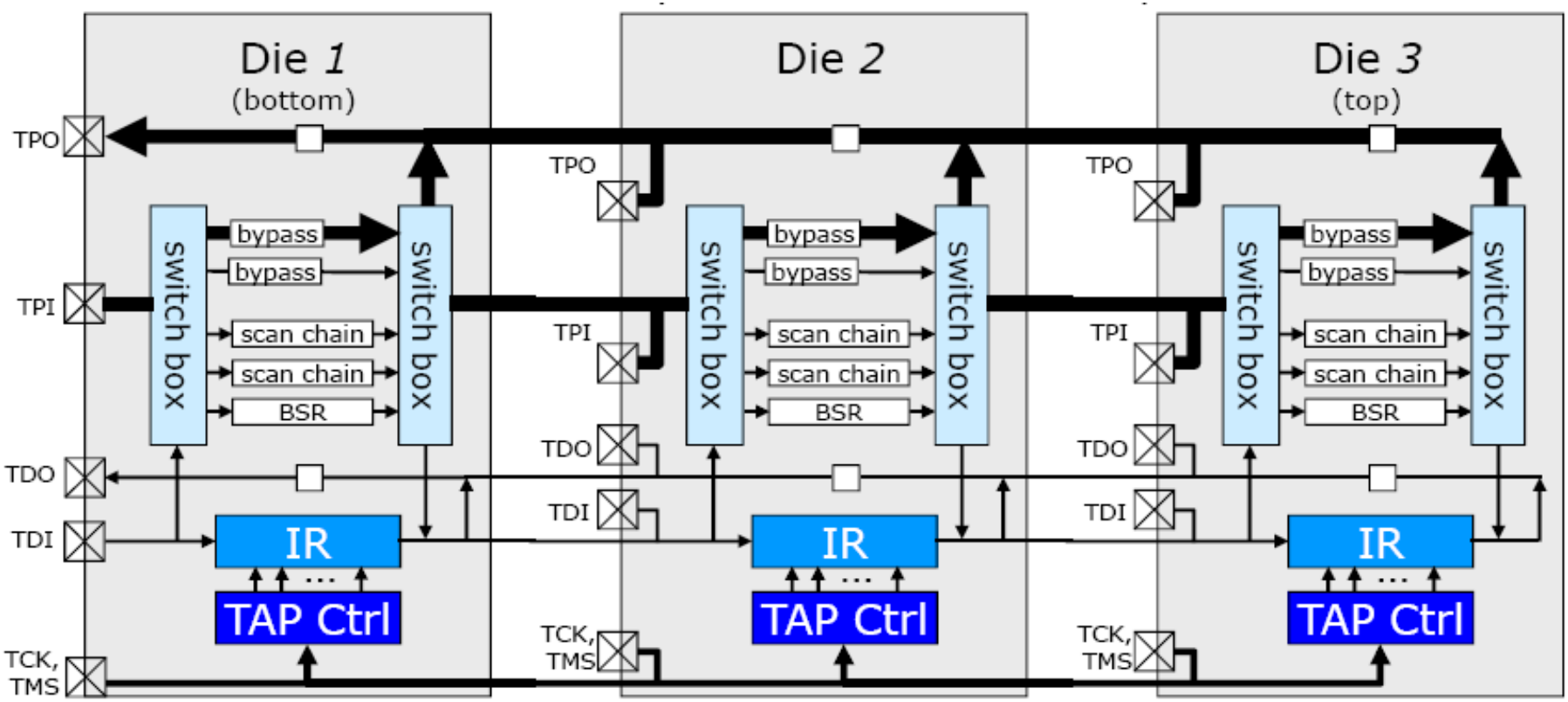
Mid / Post-Bond
- Die (re-)test
- Interconnect test



Post-Packaging
- Die (re-)test
- Interconnect (re-)test

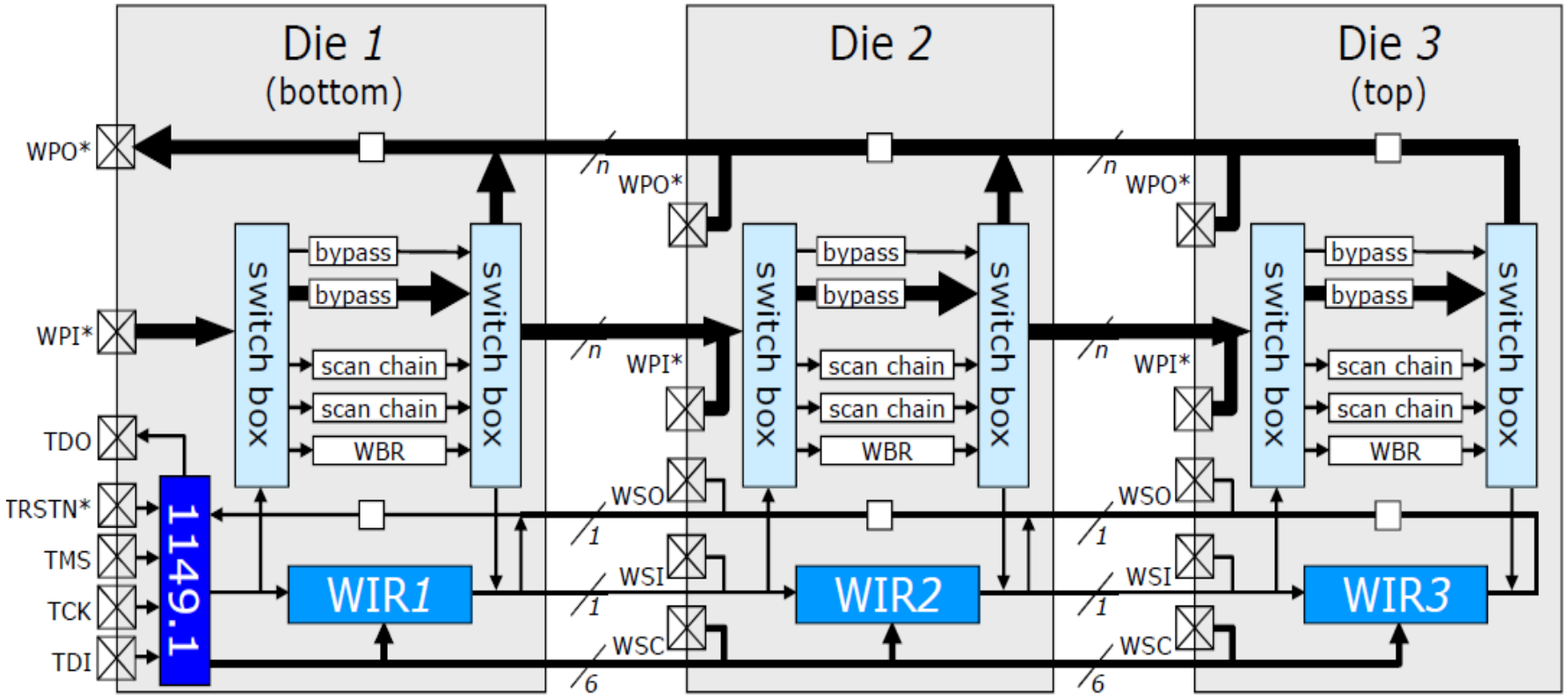
4. To-The-Point Please

An IEEE 1149.1-Based Die Wrapper…



4. To-The-Point Please

… Or An IEEE 1500-Based Die Wrapper



Ongoing Discussions

- After looking at several solution proposals,
  the Working Group took a step back for Requirements Engineering

- Some of the ongoing discussions
  - Die stacks under consideration:
    single-tower, multi-tower,
    multi-tower with roof or overhang,
    passive interposer base, passive interposer intermediate layers,
    TSV-interconnects only, wire-bonds (connecting non-adjacent tiers)
  - Digital only, or also support for non-digital dies/tests
  - Die wrapper based on IEEE 1149.1, IEEE 1500, or both

Conclusion

- 3D-SIC: hot topic w.r.t. processing, design, and now also test
- 3D-Test Standardization Study Group yielded approved PAR
- 3D-Test Working Group working on Project P1838
  - Die Wrapper
  - Generic test access to and between dies in a multi-die stack

- **More information**
  - Websites: http://grouper.ieee.org/groups/3Dtest/
    http://grouper.ieee.org/groups/1838/
  - WG Chair : Erik Jan Marinissen – erik.jan.marinissen@imec.be
  - WG Vice-Chair : Adam Cron – adam.cron@synopsys.com