Status Update of IEEE Std P1838

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IEEE International Test Conference (ITC’13)
Anaheim, CA, USA – September 8, 2013
3D-Test Standardization Study Group

- Active January 2010, initiated by Erik Jan Marinissen (IMEC)
- Charter: inventory need for and timeliness of standards in 3D test and DfT
- ~60 members, weekly WebEx conference calls (hosted by Cisco Systems)
- Regular status updates: VTS’10, ETS’10, ITC’10

  - PAR submitted to IEEE-SA NesCom : November 23, 2010
  - PAR approved : February 2, 2011
3D-Test Working Group

- Active February 2011, after approval of PAR P1838

- Charter:
  define standards in 3D test and DfT

- Current project:
  - P1838: "Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits"
Embedding in IEEE Organization

- **IEEE** sponsors
  - Computer Society sponsors
  - TTTC sponsors
  - TTSC sponsors
- **WG Membership**
  - Open to professionals
  - No dues or fees
- **IEEE-SA**
  - Provides facilities
    - Web hosting
    - E-mail reflector facility
  - IEEE-SA membership required for ballot
  - Will own and publish resulting standard(s)

Diagram:
```
IEEE
  ▼
  IEEE Standards Association
    ▼
  IEEE-4155 Working Group on 3D Test

  ▼
  Computer Society
    ▼
  Test Technology Technical Council
    ▼
  Test Technology Standards Committee
```

http://www.ieee.org/
http://www.computer.org
http://tab.computer.org/tttc/
http://grouper.ieee.org/groups/ttsg/
http://grouper.ieee.org/groups/3Dtest/
### WG Leadership and Officers

- **Chair**: Erik Jan Marinissen (IMEC)
- **Vice-Chair**: Adam Cron (Synopsys)
- **Secretary**: Sophocles Metsis (AMD)
- **Co-Editor**: Al Crouch (Asset-InterTech)
- **Co-Editor**: Michael Wahl (University of Siegen)
- **Web-Masters**: Saman Adham (TSMC), Erik Jan Marinissen (IMEC)
- **WebEx Host**: Bill Eklow (Cisco Systems)
Working Group Members*

Paul Abelovski  Bill Eklow  Harrison Miles
Saman Adham    Sandeep Goel  Benoit Nadeau-Dostie
Tahir Ahmad     Michelangelo Grosso  Christos Papameletis
Shantanu Bhalerao  Gurgen Harutyunyan  Ken Parker
Sandeep Bhatia  Michael Higgins  Joseph Reynick
Sudipta Bhawmik  Chun-Lung Hsu  Mike Ricchetti
Tapan Chakraborty  Marc Hutner  Ben Rogel
Vincent Chalendard  Hongshin Jun  Angarai Sivaram
Chen-An Chen   Shuichi Kameyama  Roger Sowada
Vivek Chickermane  Clark Liu  Craig Stephan
CJ Clark       Amit Majumdar  Brian Turmell
Zoe Conroy  TM Mak  Pascal Vivet
Eric Cormack  Rafic Zein Makki  Michael Wahl
Adam Cron     Arie Margulis  Min-Jer Wang
Al Crouch     Erik Jan Marinissen  Lee Whetsel
Damon Domke  Cedric Mayor
Ted Eaton     Teresa McLaurin
Heiko Ehrenberg  Sophocles Metsis

+ 53× “followers”

* status 2013/08/26
3D-Test WG Participating Companies
Working Group Operation

• **Communication**
  - Public website: [http://grouper.ieee.org/groups/3Dtest/](http://grouper.ieee.org/groups/3Dtest/)
  - Private web site and e-mail reflector for internal communication

• **Meetings**
  - Weekly conference calls: Thursdays 5-6pm Europe / 8-9am Pacific
    Kindly hosted by Cisco Systems
  - Ad-hoc face-to-face meetings (e.g., here at ITC’13)
Project Authorization Request (PAR)

- **Title**
  "Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits"

- **Dates**
  - PAR request date: November 23, 2010
  - PAR approval date: February 2, 2011
  - PAR expiration date: December 31, 2015

- **PAR On-Line:**
PAR Summary – 1/2

• **Focus**
  – Generic test access to and between dies in a multi-die stack
  – Prime focus on stacks with TSV-based interconnects

• **Test**
  – Pre-bond, mid-bond (partial stack), post-bond (complete stack)
  – Intra-die circuitry and inter-die interconnects
  – Pre-packaging, post-packaging, board-level situations

• **Die-Centric Standard**
  – Die-level features comprise a stack-level architecture
    • Compliance to standard pertains to a die (not to the stack)
    • Enables interoperability between Die and Stack Maker(s)
  – Standard does *not* address stack/product-level challenges/solutions
    • E.g. Boundary Scan for board-level interconnect testing
    • However, standard should not prohibit application thereof
PAR Summary – 2/2

• Two Standardized Components
  1. 3D Test Wrapper hardware per die
  2. Description + description language

• Scan-Based
  – Based on and works with digital scan-based test access

• Leverage Existing DfT Wherever Applicable/Appropriate
  – Test access ports (such as IEEE 1149.x)
  – On-die design-for-test (such as IEEE 1500)
  – On-die design-for-debug (such as IEEE P1687)

• Standard Does Not Mandate
  – Specific defect or fault models
  – Test generation methods
  – Die-internal design-for-test
Current Focus: Simple (Linear) Stacks

Definition
• Interconnected dies electrically form one sequence
• External I/Os all at one extreme of that sequence

Practical Set-Ups
• Abstraction from physical set-up, only electrical connections considered
• Electrically, a single tower consisting of
  – One or more active dies
  – Zero or more passive interposer dies in between
• Interconnects only between dies adjacent in the sequence

Examples
For Later: Complex Stacks

Extensions from Simple Stacks (= Not Allowed in Simple Stacks)
1. Multiple towers and sub-towers, possibly with “roof”
2. Interconnects between non-adjacent dies
3. External I/Os in multiple dies

Examples
Die Naming In The Stack

- Focus on simple (linear) stacks allows to number dies:
  - Die 1: die that holds external I/Os
  - Die 2, Die 3, ...

- Die naming (depending on relative role in the stack):
  - **First die**: Die 1
  - **Middle die**: Die $i$ in stack with $n$ dies (with $1 < i < n$)
  - **Last die**: Die $n$ in stack with $n$ dies
  - **Last compliant die**:
    Die $k$ in stack with $n$ dies of which first $k$ dies are compliant ($1 \leq k \leq n$)
- This supports the notion that perhaps not all dies in the stack will be P1838 compliant
- Full P1838 compliance benefits are only obtained if there is an uninterrupted sequence of compliant dies from Die 1 onwards
- Non-compliant dies at the end of the stack might still be testable and benefit from P1838 infrastructure. Example:
  - JEDEC Wide-I/O DRAM on top of stack of compliant dies
Primary and Secondary Test Ports

- **Primary Test Port:**
  Test interface (*in*: test control, test stimuli; *out*: test responses)
  - At external I/O (in case of first die)
  - To be connected to the previous die (in case of a middle or last die)

- **Secondary Test Port:**
  Test interface (*out*: test control, test stimuli; *in*: test responses)
  - To be connected to the next die (in case of first or a middle die)
  - Non existent (in case of last die or last compliant die)
P1838: DfT Architecture Standard Only

- Stacking of dies requires that vertical interconnects (micro-bumps, TSVs) are aligned
  - Footprint: matching x,y-location
    (limited correction by RDL, at a cost)
  - Mechanical: matching materials, diameter, height, etc.
  - Electrical: matching driver/receiver pairs

- As a generic DfT standard, P1838 will not define the footprint and/or mechanical/electrical properties of its test ports
  - P1838 defines architecture only (like IEEE 1149.x and IEEE 1500):
    - Number, name, type, and function of test port I/Os
    - Clock-cycle accurate test operation protocol
    - Test hardware and protocol description language

- Consequence: off-the-shelf P1838-compliant dies are not guaranteed to ‘plug-n-play’ with each other without further alignment
  - Test ports require more parameters: footprint, mechanical, electrical
  - The same is also true for the functional interfaces!
Ongoing Discussions in the WG (1/2)

1. Serial Test Port
   - For configuration instructions and low-bandwidth test data
   - Based on IEEE 1149.1: TAP and TAP Controller per die
     • Connect to board-level test infrastructure
     • Protects large investment in TAP-based test access
   - Discussion: synchronization and pipeline flip-flops

2. Die Wrapper
   - Wrapper cells at all die I/Os (external I/Os and TSVs)
   - Based on flexible IEEE 1500 wrapper cell definition: allows shared/dedicated, single/multiple FFs, ripple protection, etc.
3. Parallel Test Port
   - Discussion on minimum width, if any
     a. Multi-lane version of TDI/TDO, leveraging serial port controls, or
     b. More general version, transporting generic data and controls
IEEE Std 1149.1 and IEEE Std 1500

- TAP on each die
- TAP provides interface to 1500 bus for access and control
- 1500 wrapper cells provide die-to-die interconnect capability
Summary

• 3D-Test Standardization Study Group yielded approved PAR (2010)

• 3D-Test Working Group working on Project P1838 (since 2011)
  – Standardized per-die DfT creates stack-level test access architecture
  – Standardized components
    • On-die DfT hardware
      (1) Die wrapper, (2) Serial test port, (3) Parallel test port
    • Test hardware and test operation description (language)

• **More information**
  – Website: [http://grouper.ieee.org/groups/3Dtest/](http://grouper.ieee.org/groups/3Dtest/)
  – WG Chair : Erik Jan Marinissen – erik.jan.marinissen@imec.be
  – WG Vice-Chair : Adam Cron – a.cron@ieee.org