SSG on 3D-Test

- **Charter**
  - Inventorize need for and timeliness of standards in 3D test and DFT
  - If appropriate, formulate Project Authorization Requests (PARs) for starting up an IEEE Standard Development Working Group (SDWG)

- **Organization & Participation**
  - 54+2 participants from companies/institutes around the globe
  - Chair: Erik Jan Marinissen (IMEC)

- **Activities to date**
  - Active per January 2010
  - Public web site: [http://grouper.ieee.org/groups/3Dtest/](http://grouper.ieee.org/groups/3Dtest/)
  - Private web site and e-mail reflector for internal communication
  - Weekly WebEx conference calls (provided by Cisco Systems)
**Organization Chart + URLs**

- IEEE sponsors
  - Computer Society sponsors
  - TTTC sponsors
  - TTSC sponsors
  - SSG on 3D-Test

- SSG membership is open to professionals

- IEEE-SA
  - Provides facilities
    - Web hosting
    - E-mail reflector facility
  - Will own and publish resulting standards

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**SSG Members**

<table>
<thead>
<tr>
<th>Saman Adham</th>
<th>Jan Olaf Gaudestad</th>
<th>John Potter</th>
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<tr>
<td>Neetu Agrawal</td>
<td>Michelangelo Grosso</td>
<td>Bill Price</td>
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<td>Lorena Anghel</td>
<td>Said Hamdioui</td>
<td>Herb Reiter</td>
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<td>Patrick Y Au</td>
<td>Klaus Helmreich</td>
<td>Mike Ricchetti</td>
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<td>Paolo Bernardi</td>
<td>Michael Higgins</td>
<td>Andrew Richardson</td>
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<td>Sandeep Bhatia</td>
<td>Gert Jervan</td>
<td>Daniel Rishavy</td>
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<td>Craig Bullock</td>
<td>Hongshin Jun</td>
<td>Jochen Rivoire</td>
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<td>Krishnendu Chakrabarty</td>
<td>Rohit Kapur</td>
<td>Volker Schöber</td>
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<td>Ji-Jan Chen</td>
<td>Ajay Khoche</td>
<td>Eric Strid</td>
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<td>Vivek Chickermane</td>
<td>Santosh J Kulkarni</td>
<td>Thomas Thaerigen</td>
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<td>CJ Clark</td>
<td>Michael Laisne</td>
<td>Jouke Verbree</td>
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<td>Eric Cormack</td>
<td>Philippe Lebourg</td>
<td>Ioannis Voyiatzis</td>
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<td>Adam Cron</td>
<td>Stephane Lecomte</td>
<td>Michael Wahl</td>
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<td>Al Crouch</td>
<td>Hans Manhaeve</td>
<td>Min-Jer Wang</td>
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<td>Shinichi Domae</td>
<td>Erik Jan Marinissen</td>
<td>Lee Whetsel</td>
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<td>Ted Eaton</td>
<td>Teresa McLaurin</td>
<td>Yervant Zorian</td>
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<td>Heiko Ehrenberg</td>
<td>Brandon Noia</td>
<td>+ Frans de Jong</td>
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<tr>
<td>Bill Eklow</td>
<td>Jay Orbon</td>
<td>+ Frank Pöhl</td>
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<td>Klaus Förster</td>
<td>Ken Parker</td>
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**Identified Standardization Needs**

During the SSG discussions, the following standardization needs were identified:

- **Die and Stack Test**
  1. DfT test access architecture
  2. Wafer probe interface

- **Access for Board-Level Users**
  3. Board-level interconnect test
  4. Access to embedded instruments

- **Test Data Formats**
  5. Wafer map and device tracking
  6. Standard Test Data Format (STDF)

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**1. DfT Architecture for Manufacturing Test**

- **Motivation**
  - Die makers need to provide DfT, also for stack- and board makers
  - Interoperability between various dies required

- **Requirements**
  - Support (1) pre-bond die test and (2) post-bond stack test
  - Support modular test approach
  - Generic and scalable
  - Low cost
    - Few extra product pins
    - Leverage of existing DfT and DfT standards

- **Status**
  - Two proposals by IMEC, based 3D extension of IEEE Std 1500 and IEEE Std 1149.1
1. DfT Architecture for Manufacturing Test

IMEC Proposals

Functional Design
- ≥2 stacked dies, possibly core-based
- Inter-connect: TSVs
- Extra-connect: pins

Existing Design-for-Test
- Core: internal scan, TDC, LBIST, MBIST; IEEE 1500 wrappers, TAMs
- Product: IEEE 1149.1
1. DfT Architecture for Manufacturing Test

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3D DfT Architecture
Test wrapper per die
- Based on IEEE Std 1500/1149.1
- Two entry/exit points per die:
  1. Pre-bond: extra probe pads
  2. Post-bond: extra TSVs

IMEC Proposal: 1500-Based Die Wrapper

- Conventional (2D) IEEE 1500 Features
  - WSC Control:
    WRCK, WSTN, SelectWIR, ShiftWR,
    CaptureWR, UpdateWR, TransferDR*
  - Serial interface: WSI-WSO
  - Parallel interface: WPI*-WPO*
  - Wrapper Instruction Register (WIR)
  - Wrapper Boundary Register (WBR)
  - Serial and parallel* Bypass

* = optional

Note: Figure abstracts from functional circuitry and only shows DfT features
1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1500-Based Die Wrapper

- **Conventional (2D) IEEE 1500 Features**
- **New 3D Features**
  1. *TestTurns*
     - Serial and parallel interface towards bottom die
     - Flip-flops for clean timing
  2. *Probe pads on non-bottom dies*
     - Mandatory on WSC, WSI-WSO
     - Scalable on WPI-WPO
  3. *TestElevators* to higher-up die(s)
     - Mirrored standard 1500 interface: WSCs, WSI-WSOs, WPIs-WPOs

Note: Figure abstracts from functional circuitry and only shows DfT features

4. **Hierarchical** WIR chain (not shown here)

**Bottom Die:** no extra product pins
- Serial interface multiplexed onto IEEE 1149.1 interface
- Parallel interface multiplexed onto existing functional pins

**Top Die:** no TestElevators (as no other die above)
1. DfT Architecture for Manufacturing Test

IMEC Proposal: 1149.1-Based Die Wrapper

- Conventional IEEE 1149.1 Features
  - TAP: TCK, TMS, TDI, TDO
  - Regular 16-state TAP Controller
  - Instruction Register
  - Bypass

- New 3D Features
  0. Scalable parallel test data port
     • For higher-bandwidth access
  1. TestTurns
     • Interface towards bottom die
     • Flip-flops for clean timing
  2. Probe pads on non-bottom dies
     • Mandatory on TCK, TMS, TDI-TDO
     • Scalable on TPI-TPO
  3. TestElevators to higher-up die(s)
     • Mirrored bottom interface: TCKs, TMSs, TDI-TDOs, TPI-TPOs
  4. Hierarchical test control IRs+WIRs for free

Note: Figure abstracts from functional circuitry and only shows DfT features.
1. DfT Architecture for Manufacturing Test

**IMEC Proposal: 1149.1-Based Die Wrapper**

- No extra product pins
  - IEEE 1149.1 interface on bottom die present anyway
  - Parallel interface multiplexed onto functional pins

- **Die 1** (bottom)
- **Die 2**
- **Die 3** (top)

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**1. DfT Architecture for Manufacturing Test**

**1149.3D Instructions = 1149.1 User Instr.**

<table>
<thead>
<tr>
<th>Field 1</th>
<th>Field 2</th>
<th>Field 3</th>
<th>Field 4</th>
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<tbody>
<tr>
<td>Serial</td>
<td>Prebond</td>
<td>Bypass</td>
<td>Turn</td>
</tr>
<tr>
<td>Parallel</td>
<td>Postbond</td>
<td>Intest</td>
<td>Elevator</td>
</tr>
<tr>
<td>Extest</td>
<td></td>
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</tbody>
</table>

**Pre-Bond Instructions**
- SerialPrebondBypassTurn
- SerialPrebondIntestTurn
- ParallelPrebondBypassTurn
- ParallelPrebondIntestTurn

**Post-Bond Instructions**
- SerialPostbondBypassTurn
- SerialPostbondIntestTurn = INTEST
- SerialPostbondExtestTurn = EXTEST
- SerialPostbondBypassElevator
- SerialPostbondIntestElevator
- SerialPostbondExtestElevator
- ParallelPostbondBypassTurn
- ParallelPostbondIntestTurn
- ParallelPostbondExtestTurn
- ParallelPostbondBypassElevator
- ParallelPostbondIntestElevator
- ParallelPostbondExtestElevator

* = functional start-up mode
1. DfT Architecture for Manufacturing Test

**Example 1: Testing Die 2**

Die 1: ParallelPostbond
BypassElevator

Die 2: ParallelPostbond
IntestTurn

Die 3: ParallelPostbond
BypassTurn

**Example 2: Test of Interconnect Die 2-3**

Die 1: SerialPostbond
BypassElevator

Die 2: SerialPostbond
ExtestElevator

Die 3: SerialPostbond
ExtestTurn
2. Wafer Probe Interface

Wafer Probing on TSVs / Micro-Bumps is Challenging

- Small pitch; small probe area
- Probe damage might impair downstream bonding

Wafer Probe Industry Would be Helped by Standardization

- Standard pad pitches
- Standard pad footprints
- Standard pad materials and designs

Benefits also for design, assembly, second sourcing, ...

Status

- Idea only, no proposals yet
- Planning to start dedicated sub-team on this topic

3. Board-Level Interconnect Test

Board-Level Interconnect Test

- Via on-chip DFT, a.k.a. "JTAG":
  IEEE Std 1149.1 Test Access Port (TAP)

External I/Os distributed over Multiple Dies

- For example due to
  - Stacks with TSVs + wire-bonds
  - Pass-through-only TSVs
  - JTAG distributed over multiple dies
  - Board-level test needs to know this in a standardized view

Status

- Idea only, no proposals yet
- Discussion in SSG how likely this would happen in products
4. Access to Embedded Instruments

For Today’s 2D Chips and Boards
- JTAG TAP reused for alternative purposes
  - BIST, diagnosis, silicon debug, FPGA progr., SW debug, etc.
  - Access to ‘embedded instruments’: monitors, sensors, etc.
    (IEEE P1687, a.k.a. “Internal-JTAG”)

Extension to 3D-SICs
- Purpose: enable this type of usage also for 3D-SICs
- Stack might contain multiple TAP Controllers
- Status: three proposals so far
  - Mix of Existing Standards:
    1149.7 (stack), 1149.1/6 (die), 1500 (core) (Asset-Intertech)
  - TAP Linking Module (Texas Instruments)
  - iMajik (Intellitech)
4. Access to Embedded Instruments

**TI Proposal: TAP Linking Module + OCT**

![TI Proposal Diagram]

**Intellitech Proposal: iMajik**

![Intellitech Proposal Diagram]
5+6. Test Data Formats

- **Wafer Maps**
  - Pass/fail information per die

- **Inkless Assembly and Single-Device Tracking**
  - Die to wafer location and wafer processing
  - Die to assembly, packaging, and test processes
  - All dies in multi-chip package

- **Standard Test Data Format (STDF)**
  - File format for (diagnostic) IC test data collection
  - Currently at STDF-v4 (2007), developing JTDF

**Standards**

- SEMI G81/G85 
  - obsolete

- SEMI E142 
  - Already handles 3D?

- SEMI STDF-v4 
  - Requires extension to 3D

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5. Wafer Maps

**SEMI E142**

Source: Dave Huntley, Kinesys
Conclusion

- 3D-SIC: hot topic w.r.t. processing, design, and now also test
- 3D-Test Standardization Study Group active per January 2010
- Topics under discussion
  - Die and Stack Test
    1. DFT test access architecture
    2. Wafer probe interface
  - Access for Board-Level Users
    3. Board-level interconnect test
    4. Access to embedded instruments
  - Test Data Formats
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