3D-IC Defect Investigation

Provisional Report of the IEEE P1838 Defect Tiger Team

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Kenneth P. Parker, Editor

1. Introduction

This report is generated by the IEEE P1838 Working Group Tiger Team assigned to investigate 3D-IC defect mechanisms that may occur in individual die, and as die are stacked together. Once the defects are enumerated, then various Design for Test (DfT) technologies can be postulated for these defects, and the implications on how such DfT technologies should be accessed can be assessed.

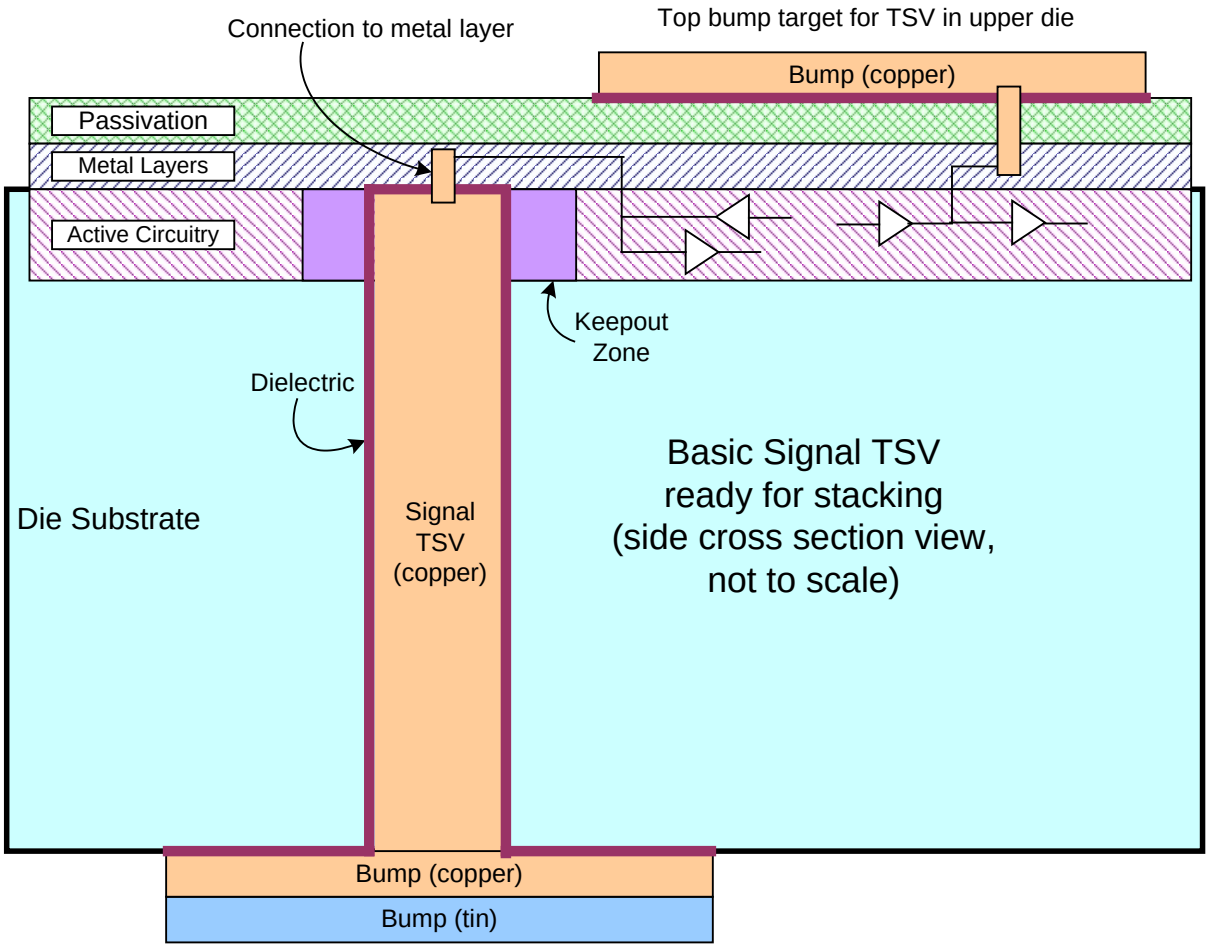


Figure 1: Basic signal TSV in a die.

Three-dimensional IC technology uses "Through-Silicon Vias" (TSV) connections to link dies within a stack. On the bottom surface of a die, TSVs are exposed and have "micro-bumps" attached to them. Figure 1 shows a

simplified, schematic diagram (not to scale) of a single die with a TSV and micro-bumps. These micro-bumps are later attached to micro-bumps on the top of a lower die and bonded electrically and mechanically. TSV protrude from the bottom of a die and travel up through a substrate where they pass through the active circuit region of the top of the die and then into the metal layer region. There, a connection to the metal layer may be made. The very top layer of the die is a passivated, insulating layer. Other micro-bumps on the top of a die may be positioned at will (including over TSV below the passivation. They may have a connection to the metal layer, and/or down to an underlying TSV. The metal layers provide connectivity between circuit elements within the active circuit region, and to TSVs and micro-bumps, for inter-die connectivity. The dielectric layer shown between the TSV copper and the die substrate is very thin and does not materially increase the effective diameter of a TSV body. The "Keepout Zone" (KOZ) is an area of the circuitry layer that should not contain active circuits. This zone is determined by the mechanical tolerances that exist when drilling/etching and filling the TSV. It may also include an area where stresses induced in the copper-silicon interface can interfere with stressed-silicon transistors. This area varies across the range of TSV fabrication technologies and is potentially significant in size.

Note that the diameter of the micro-bumps is much wider than that of the TSVs, by a factor of (today) around five to one. With 5 µm diameter TSVs, the micro-bumps are around 25 µm. But the achievable pitch of a dense array of TSV-micro-bumps, is around 40 µm. This is shown in Figure 2. Note that the TSV copper and keepout zone subtract from the area that can be used for active circuitry, but the micro-bump rests on non-circuit area and does not subtract from usable area.

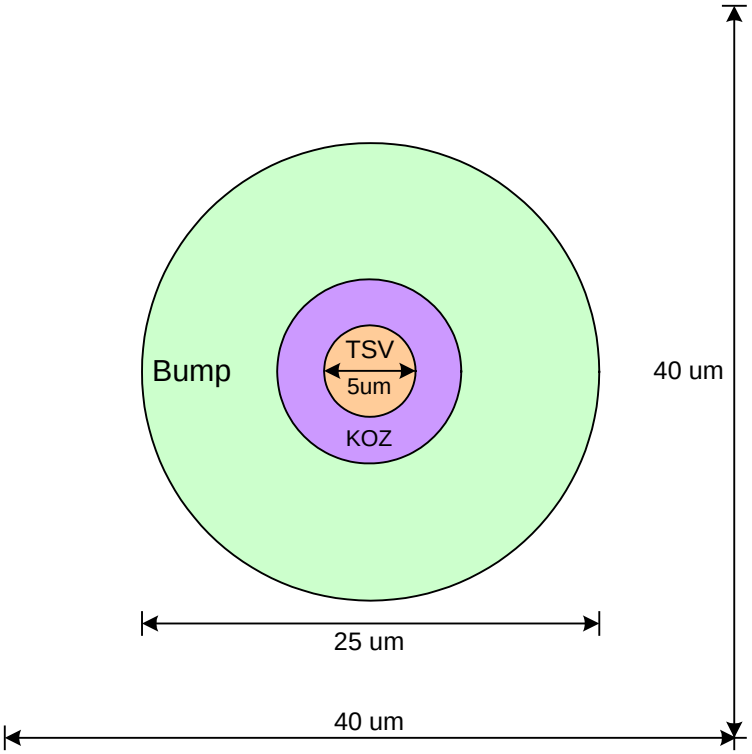


Figure 2: Top view of TSV and micro-bump dimensions and pitch.

There are other flavors of TSVs. One is a vertically stacked TSV-micro-bump pair intended for distributing power upwards in a stack of dies. An example is shown in Figure 3. The redundant connections between the TSV and the topside micro-bump are there to enhance current delivery. There may be a tap from the TSV to the metal layers if power is also being delivered to this die by this TSV.

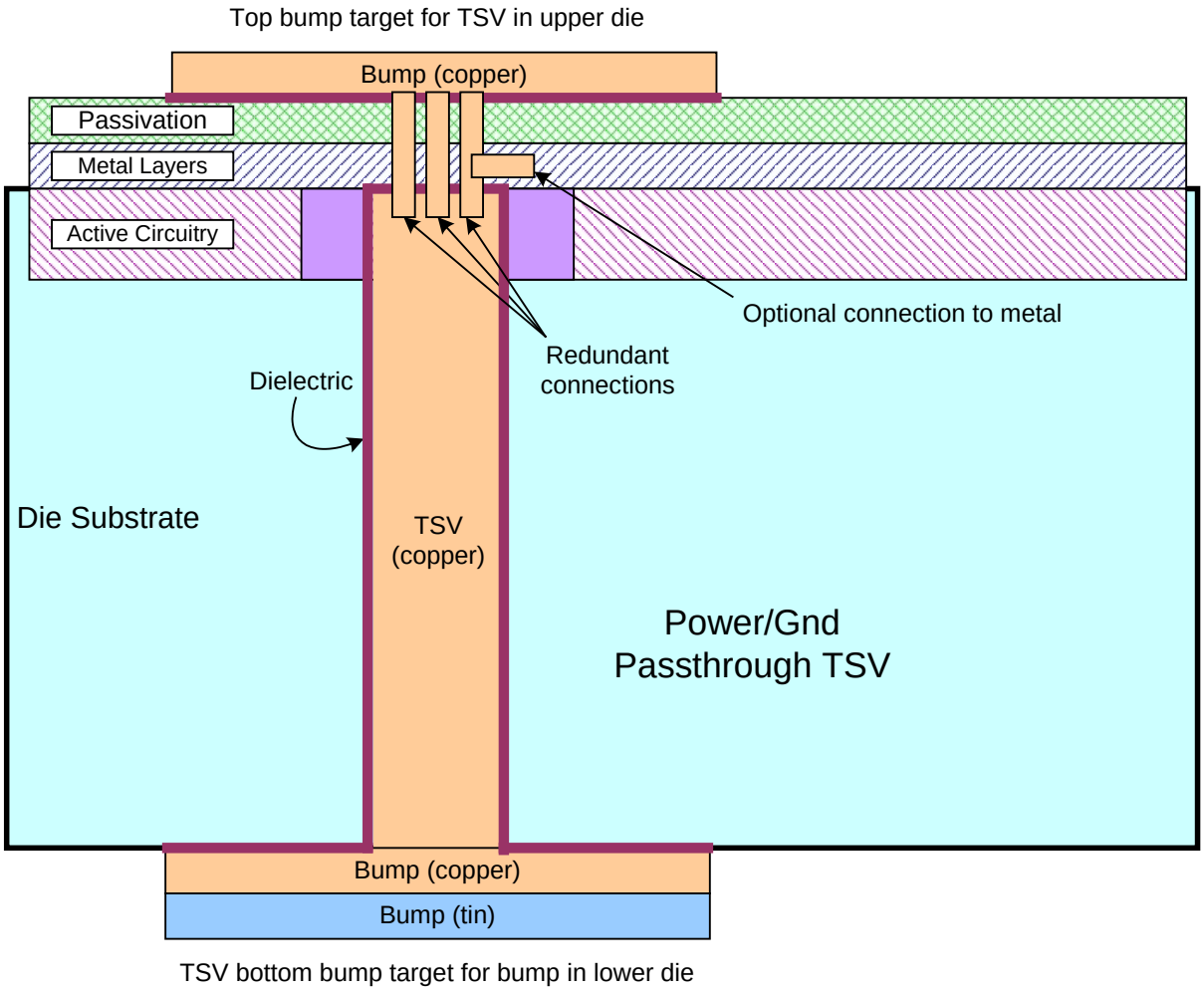


Figure 3: A power/ground TSV.

The option to tap this TSV pathway into the metal layer offers the opportunity to use die circuitry to monitor the TSVs performance. Since the TSV is intended to pass power (it is a constant voltage conductor) we would not be able to stimulate/control it.

Such TSV structures may also be used for mechanical reasons, such as providing mechanical support or strength across an area of low TSV density, or for providing additional thermal conduction pathways. Internal defects in such TSVs are likely not a concern, but if such a TSV was close enough to a signal TSV, then if they shorted together, a larger capacitive load might be presented to the signal TSV. Thus, an engineering decision may be justified about adding control/observe capability into such a TSV.

Another flavor of vertical stacked TSVs comes from the case where signal distribution across several dies is required. An obvious example would be the TCK and TMS signals of 1149.1, if that standard was implemented in several stacked dies. See Figure 4.

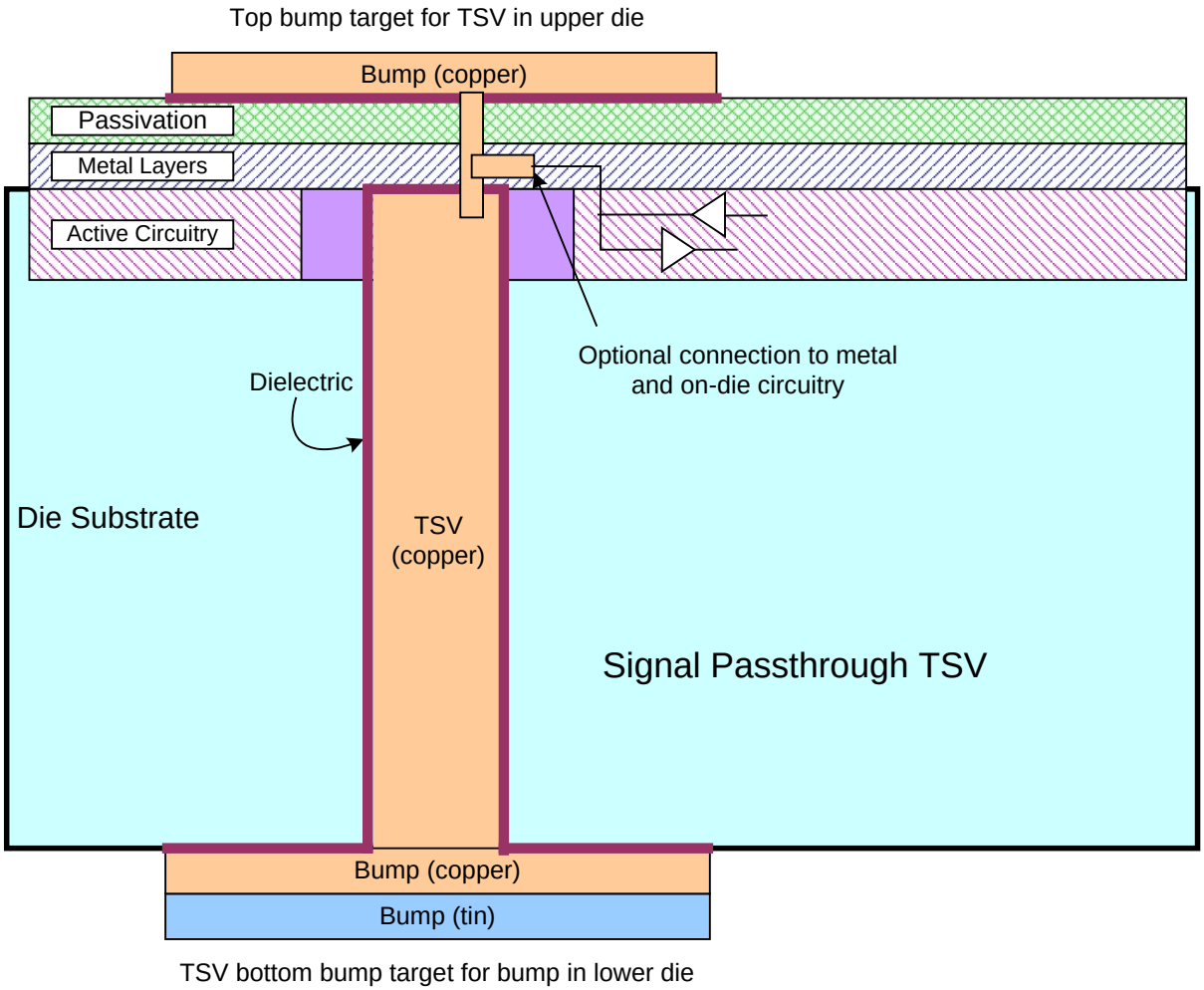


Figure 4: A passthrough signal TSV.

The option to tap this TSV pathway into the metal layer offers the opportunity to use die circuitry to monitor and control the TSV for testing purposes.

When two dies are bonded together, the goal is to successfully connect all topside micro-bumps on the lower die with their associated bottomside TSV micro-bumps on the upper die. This is shown in Figure 5. The tin material is the "solder" that makes a low resistance connection between the copper surfaces between the two dies. The alignment process is crucial so that each bottomside TSV micro-bump properly connects to the topside micro-bump.

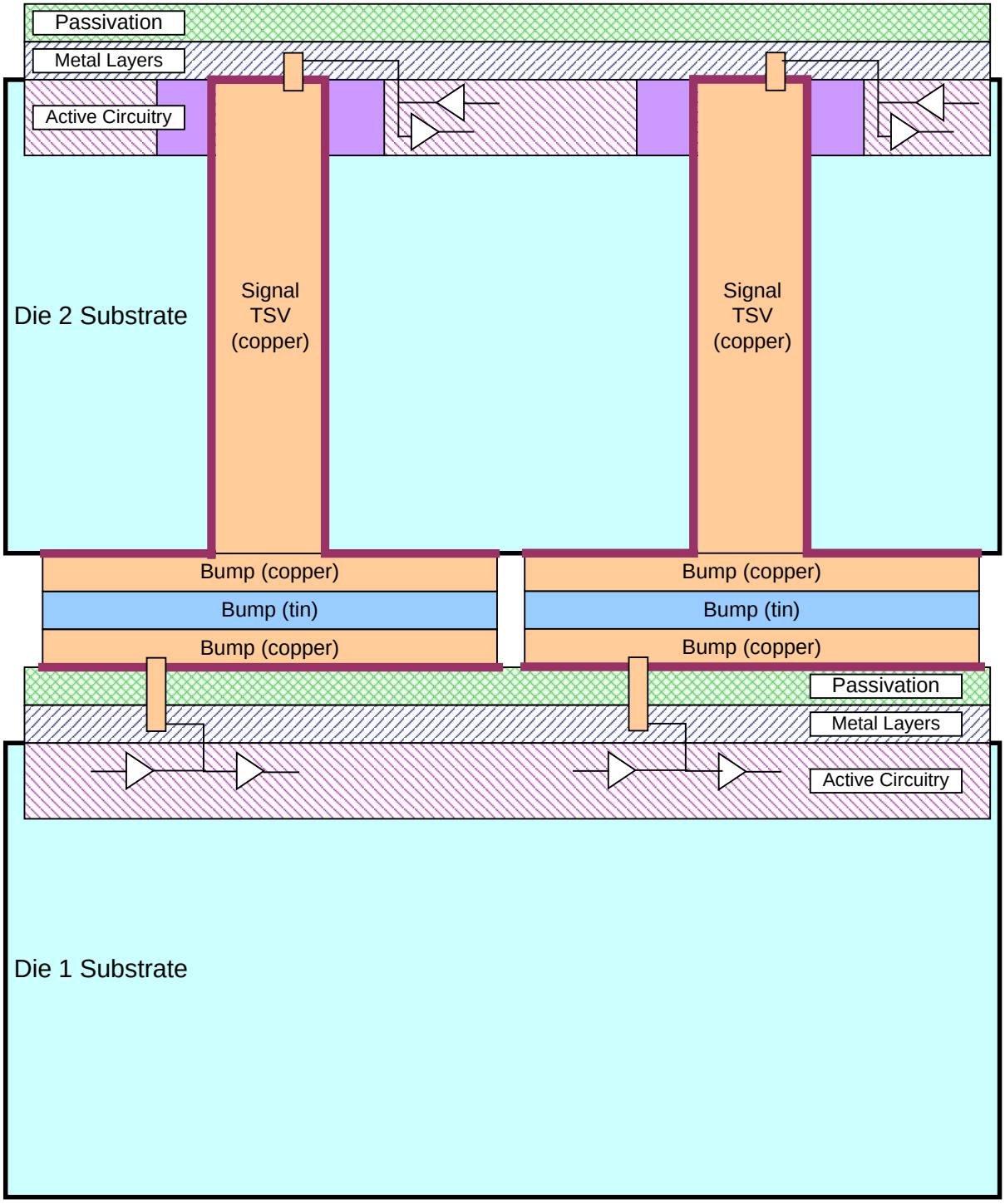


Figure 5: Two dies bonded together at two TSV sites.

Note that Figure 5 shows the location of a TSV in the upper die has the same XY coordinates as the mating micro-bump in the lower die. There are cases where a redistribution layer on the top die, or a passive interposer

between die, allow there to be different locations. The additional wiring of this mapping adds new opportunities for shorts or opens to occur. This is omitted since they do not add new defects cases to our simplified model. Rather, they add new members to open/short ambiguity sets.

Figure 6 shows a base die that uses classic wire bonding technology to connect to the device substrate. In this case, the base die has topside micro-bumps to mate with a 2nd level die's TSV micro-bumps. More levels (not shown) could be bonded atop this 2nd level die.

If the base die were flip-chip technology, then it would not use wire bonding to attach to the device substrate, but would use package micro-bump technology and would be mounted face-down. This would mean the interface to the 2nd level die would use TSVs from the base die rather than topside micro-bumps. The 2nd level die would interface that to array of TSVs with topside micro-bumps also facing down.

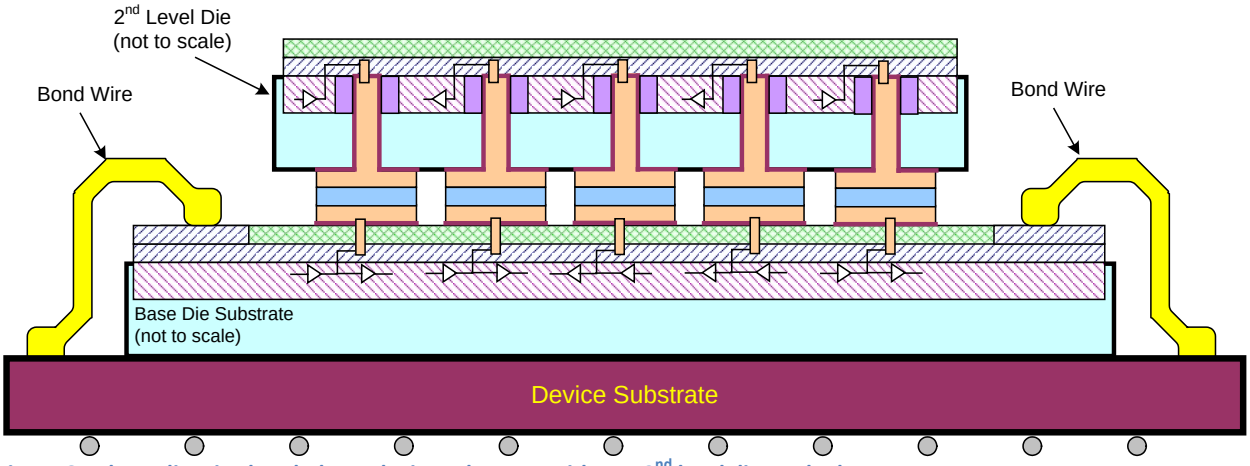


Figure 6: A base die wire-bonded to a device substrate, with one 2nd level die stacked on top.

There are cases where dies may be stacked together using only micro-bumps, that is, without TSVs. In this case two dies are stacked "face to face". This is not believed to affect this defect analysis or implications on DFT.

2. 3D-IC Defects

The P1838 standard may ultimately supply the access mechanisms for testing in several situations:

- Pre-bond: Bare die before "thinning" that exposes TSVs.
- Pre-bond: Bare die after thinning and micro-bump deposition.
- Mid-bond: Stacked die assemblies as each new die is attached.
- Post-bond: Stacked die assemblies after the last die is attached.
- Final test: Finished 3D-ICs attached to printed circuit boards.

By examining the nature of defects and their context (for example, bare die before thinning), one can determine what sort of test resources might be needed to detect them, which leads to DfT requirements and how these resources are accessed. When a collection of such scenarios are to be targeted, then DfT ideally will have sufficient capabilities to adequately address all of them. This chapter examines defects in TSV structures, while the next chapter looks at how they could be tested.

2.1.Die-based defects

Die-based defects affect TSVs and micro-bumps, and are created during the drilling/etching and filling and micro-bumping processes. We do not consider "ordinary" defects related to logic or metallization formation that are unrelated to TSVs or micro-bumps, as it is understood these must also be tested using known test approaches. Refer to Figure 1 for a defect-free TSV and Figure 7 for cases of physical defects and their electrical models.

In the defect-free case, the series resistance of the TSV (from top to bottom) is typically quite small, perhaps less than 10 milliohms[1], which means less than 10 millivolts of IR drop per ampere of current (dissipating 10 mW of power). Most TSVs should never conduct such a high current with the possible exception of power delivery TSVs. There is always some capacitance across the dielectric barrier to the substrate (see Figure 7A). This capacitance is a function of the TSV surface area surrounded by the substrate and the thickness of the dielectric.

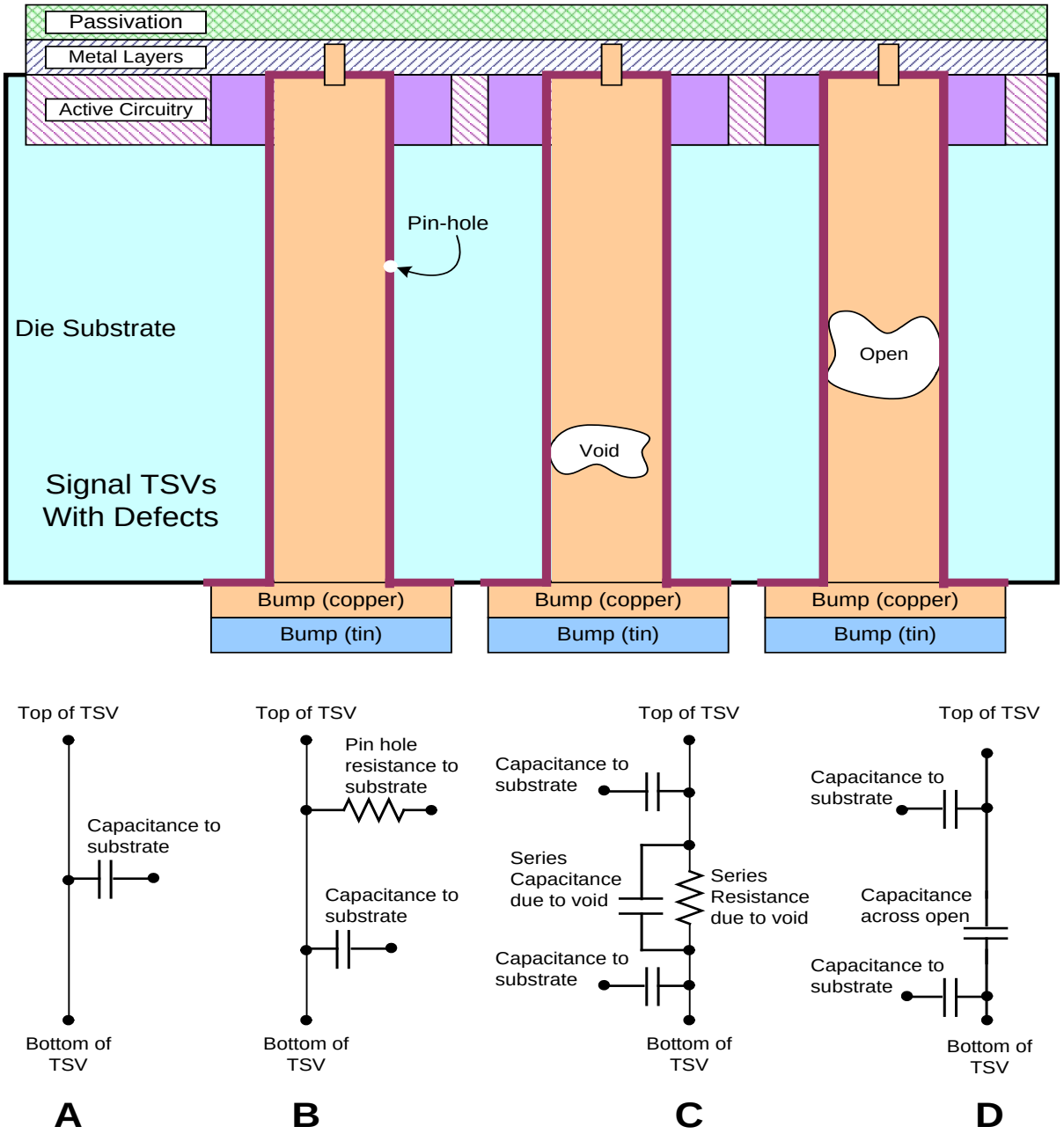


Figure 7: TSV defect-free model (A) and defects with models (B, C and D).

[1] Here it is assumed that any choice of TSV metal has a low series resistance. If this is not true, then the model of a good TSV should be modified to contain a series resistance. In some defect models, this series resistance may also have to be added.

2.1.1. TSV Dielectric Pin-hole defects.

Pin-hole defects in the thin dielectric between TSV copper and the die substrate allow leakage current to/from the TSV depending on respective TSV/substrate voltages. (See Figure 7B.) It has been observed that pin-hole leakage magnitude may be temperature or time dependent, particularly if the thermal expansion coefficients of the TSV are significantly different than the surrounding materials. If we assume the substrate is grounded, then pin-holes leak to ground, but if the substrate is floating, then multiple TSVs with pin-holes can communicate current among their respective TSVs. Also, depending on the conductivity of the substrate, there may be an effective series impedance from the pin hole through the substrate to the destination of the leakage current. Note, the TSV-to-substrate capacitance is effectively unchanged as the pin-hole is very small.

2.1.2. Voids in the TSV copper body

Voids in TSVs introduce resistivity (see Figure 7C) or a full open (see Figure 7D) and will have a voltage drop across them. For power/ground TSVs this drop may compromise power delivery to other dies after stacking. It can also introduce RC time delays in signal propagation paths. Full open voids may convert a conductive path to one that is capacitively coupled. There can also be capacitive coupling to the substrate from the two segments of the open TSV. Depending on the size of the open and its placement, the three capacitances may have different values. Note also that for a resistive void, the equivalent path may be a resistor/capacitor pair in parallel.

2.1.3. Shorts/opens between a TSV and metallization interconnect

These shorts provide connectivity to the wrong metal path, and opens refer to compromised expected connectivity. The connectivity of either short or open may be resistive. Normal connectivity should have very low resistance (< 10 milliohms). Testing for these shorts and opens could be a side effect of testing the active circuitry and metal layers.

2.1.4. For post-thinned die, improperly formed TSV micro-bump targets

Once a die has been thinned, exposing the TSV tips for application of the micro-bump targets (both copper and tin), missing or malformed micro-bumps may lead to stacking defects later. Missing micro-bumps on individual die are very difficult to sense without active probing but might be located with visual inspection. This is because electrical means of testing would require stimulus/sense capability on each side of the micro-bump, but the active electronic area exists on only one side.

2.1.5. Improperly formed topside micro-bump targets

Missing or malformed micro-bumps may lead to stacking defects later. Missing micro-bumps on individual die are very difficult to sense without active probing (but could be located with visual inspection). This is because electrical means of testing would require drive/sense capability on each side of the micro-bump, but the active electronic area exists on only one side.

2.2.Stacked die defects

When one die is bonded to another, a potentially large number of bottom TSV target micro-bumps on one die are aligned with top micro-bumps an another die, and then bonded (we've seen the word "soldered" here) such that a low-impedance intermetallic copper-tin-copper interface connects each bond site. (See Figure 5.) As before, there are a multitude of other defects possible in the circuitry and metallization that must be tested by conventional methods and are not considered here.

2.2.1. Die misalignment

Misalignment causes centering errors on some, most or all of the bonding pairs. These errors may be small or large depending on the nature of the misalignment. For example, a rotational error can cause increasing alignment error as the distance from the center of rotation increases, with small radii causing minor alignment errors, and larger radii causing pairs to completely miss each other (open connections). Also, nearby bonding sites may become shorted.

A gross cause of misalignment may occur when the die to be attached is rotated +/-90 or 180 degrees from normal. If a standard grid of micro-bumps is used, it is conceivable that TSV micro-bumps will bond with topside micro-bumps, but the rotation will effectively scramble the connectivity. It is highly likely that such connections will cause power-to-ground shorts that prevent the stack from being powered properly, preventing electrical testing. If by some chance the stack could be powered, then it is highly unlikely that the test signal infrastructure from die to new die would allow testing, as these signals would not be properly connected.

2.2.2. Improper bonding

Bonds may not occur due to processing issues, leading to opens or resistive opens. Undiscovered die defects may be a cause, for example, missing or malformed micro-bumps. Incomplete bonding may also introduce defective (resistive) connectivity. Opens may also have a significant capacitance connecting the two otherwise isolated surfaces.

2.2.3. Shorts between adjacent bonding sites

Shorts can be caused by misalignment, or by extrusion of the tin metal during bonding such that a nearby micro-bump is contacted. This may be a short or a resistive short.

2.2.4. Stacking incorrect die.

This could happen, but it is unlikely that the matchup between bonding sites would be sufficient to perform meaningful tests. For example, power delivery from the lower die to the upper (new) die might not fortuitously allow the new die to receive proper power. It is even less likely that enough pathways would be completed unless they were always situated in standardized layouts for all the potential die that could be stacked. People do worry about nefarious substitution of counterfeit die where the bonding might well be successful and the problem is in detecting the substitution of die. This is not considered here.

2.2.5. Latent stacked die defects

Defects that are activated by stimuli that occur or accumulate after stack assembly and test are called "latent" defects. Several types and their causes have been identified:

- Interdie bonds may be damaged by thermal cycling which induces warping across the die. If one die expands more than its bonded neighbor, this can stress die bonds, causing breakage (opens) or resistive connectivity. This may also lead to intermittent connections, and could affect a cluster of connections in an area, leading to multiple defects.
- Vertical expansion of copper TSVs may change their lengths. Thermal expansion may be the cause, and the amount of expansion may be variable between TSVs due to their proximity to a heat source. As heating varies, the amount of expansion may vary in time. The net effect is for an expanding TSV to "pump" against the next die, giving local stress to nearby TSVs that do not undergo expansion. This can lead to breakage or tearing of die bonds, leading to opens, or resistive connections. Multiple defects in a local area may result.

Latent defects are of concern in that they may occur after the manufacturing test step(s), perhaps even in final application environments. The possibility of multiple defects may also complicate test, where assumptions of single defects (or at least those not spatially correlated) may have played a part in the development of the test. This can confound the diagnosis process.

2.3.Finished 3D-ICs attached to boards

Finished 3D devices are attached to boards using familiar solder-paste and reflow processes. The defects that may occur are the well-known PCOLA-SOQ types. The P1838 stated philosophy (to date) is for there to be a Boundary Scan-based capability at least at the base die level to support board tests after finished 3D-ICs are attached to the board. Additional testing for advanced functionality, for example, utilizing concepts in development by the P1687 effort, are anticipated, but not yet developed.

Boundary Scan test of attached devices is not fool-proof, and care should be taken that the implementation of the 1149.1 standard is capable of detecting shorts and opens, as well as types of resistive shorts and opens.

3. Test Scenarios

In this chapter, testing of TSV and micro-bump defects is considered. These are categorized into scenarios that reflect the challenges that are seen at various manufacturing stages. For example, finding defects on single die will be accomplished differently than testing dies after stacking them together. Since yields will need to be optimized, it is unlikely that testing would be deferred until the 3D assembly is finished – testing along the way will help prevent the waste of good assemblies that are subsequently bonded to bad dies, or defectively bonded to otherwise good dies.

We assume that there is little chance for repair once a die or stack is damaged – the difficulty in "undoing" a step and removing a defect is quite high. So, it behooves industry to strive for good die, good attachment processes, and the ability to discover problems as quickly as possible rather than after several more steps are completed.

Back at the opening of Chapter 2 a number of testing situations are enumerated. Basically, they are pre-bond testing of individual die, and post-bond testing of two or more dies, as partial or finally completed assemblies. The incremental nature of testing 3D-ICs as more dies are applied is somewhat different than typical board testing. In board testing, most devices are attached to the board the first time it is tested for manufacturing defects. Those that are not may be optional devices (like extension memory) or they are socketed devices that are installed later and tested in a more functional fashion. The test plan for such a board takes missing devices into account, such that testability features such as Boundary Scan will still facilitate testing of what is there. In 3D testing, we see more incremental bonding steps, and each new bonding step adds a new die-to-die interface to be tested, although it may be important to verify that a given step has not introduced defects into previously tested interfaces. Thus, how we organize testing into logical groupings is important.

3.1. Testing with physical probe access

This section discusses the merits and challenges of physically probing devices.

3.1.1. Base die

The base die is differentiated from upper dies in that it has bonding wire pad sites, most likely around its perimeter. These sites are much larger than TSVs and are conventionally accessed with "probe cards" that have springy probing needles that are brought into contact with the bonding wire pads. These probes supply power and may touch all the other bond wire pads. If so, then a full Boundary Scan test can be executed to prove that each signal bond pad has independent observability and/or control, since the base die is envisioned to have 1149.1 support for later board testing support. The tester driving the probe card would backstop the Boundary Scan test providing complementary resources to prove the die worked with respect to bonding pads.

However, on that same surface there could be TSV topside micro-bumps. These could be very numerous and have a notably smaller pitch and may or may not be fully accessible. Perhaps only some fraction is accessible due to pitch limitations. In such case a fine-pitch array of micro-bump probes would likely be used, with some of those contacting bond wire pads sites as they look like oversized micro-bumps. (See Figure 8.) The 1149.1 EXTEST instruction could be used to prove the bond wire pads are operational. But the micro-bump DfT resources should probably be accessed independently, as this resource will be needed later to conduct post-bond testing to an upper die. Note that since the probes are connected directly to a tester with some set of test resources, which will determine what type of testing can be conducted with the micro-bumps. For example, the tester could measure the current flow of digital 0/1 states at each micro-bump. A more capable tester might be able to apply a precision load to each micro-bump to stress the connection and thus look for unwanted path resistance. Some test equipment might be able to measure substrate leakage or even capacitance. When physical access is available, there are choices directly attributable to the capabilities (and expense) of the tester hardware. So, we have postulated two test scenarios for the base die, 1149.1 EXTEST for the bond pads, and some independent instruction that works with the topside micro-bumps, perhaps much like EXTEST as well. These allow the separation of testing requirements. A question: what should micro-bump DfT pads be doing while EXTEST is in place? Should the micro-bumps be disabled? Should this be a choice exercised by design or hard-wired?

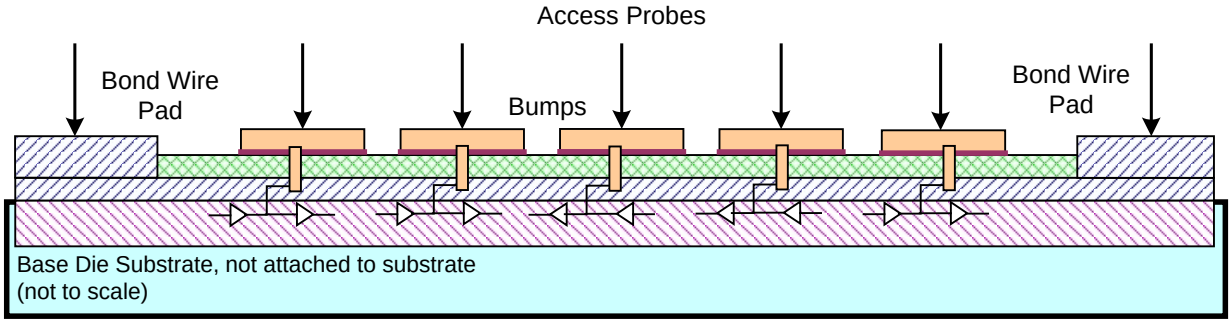


Figure 8: Base die with bond wire pads and micro-bumps.

Next, the base die can be mounted and bond-wired into its device package, in preparation for subsequent stacking (see Figure 6). This assembly could be tested on another fixture that only interfaces to the ball grid array on the package. Again, Boundary Scan tests can check out all the bond wiring for defects. This same fixture could also be used to test the assembly after each new die is attached, if all post-bond attachments are tested solely by non-physical access means.

3.1.2. Non-base die

When there are TSVs and micro-bumps on both sides of the die, then the question of access gets more complex. Here, none of the possible probe points is as large as a bond-wire pad so probing pitch is more difficult. (See Figure 9.) The next question is which side should be probed, or, is it possible to probe both at the same time, with a "clamshell" fixture.

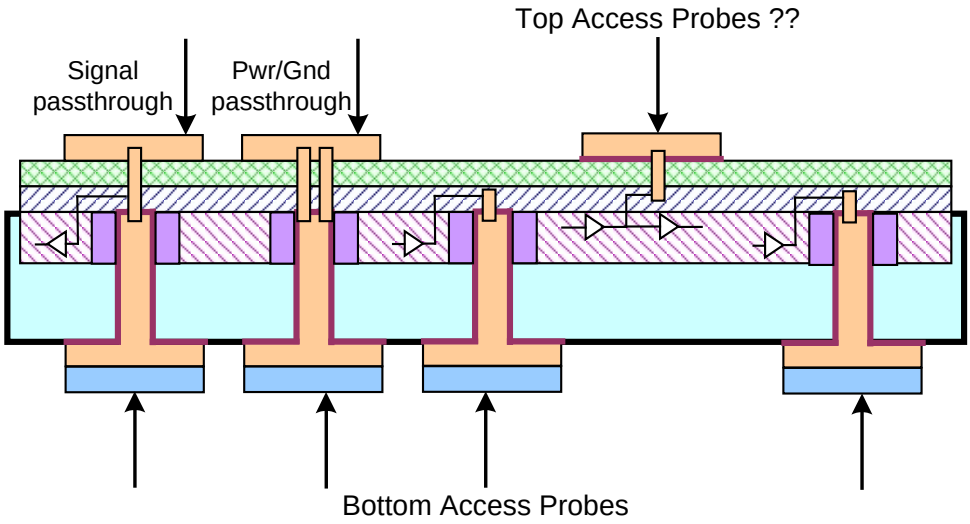


Figure 9: Non-base die with signals and pass-throughs.

Clamshell fixtures are in use for board test, but even at the far-larger pitch of board test probing, the clamshell design introduces registration complexity and cost. Such a concept may be untenable for 3D-IC probing, at least for cost-sensitive applications, for the foreseeable future. The clamshell approach would have obvious advantages; for example, it would allow direct ohmic measurements of passthrough vias.

If a clamshell is not possible, then the DfT could be set up to work either interface (top versus bottom) in succession and use two fixtures. This certainly could double the test fixturing cost, but might improve yields if more defects were discovered before die bonding. If only one test fixture can be afforded, which should it be? That might depend on the yield of the topside versus bottom side structures. If TSV formation is more challenging, then bottom side probing might be the better choice. In any case, the ability to focus on one interface at a time would help with die testing on a fixture, and later provide ½ of the interface test capability when the next die is bonded on.

The number of TSVs and micro-bumps and their pitch may put practical limits on how many can be accessed. If any of these cannot be accessed, it may still be possible to find certain defects. For example, if bottom side access is missing to certain TSVs, then opens and voids may not be testable (depending of the DfT resources available) but shorts to other TSVs can be tested given the right DfT resources.

3.2. Testing without physical probe access

This section focuses on testing without physical probe access – beyond that minimum access required to connect to the basic DfT resources (such as a TAP) and also power/ground connections. One obvious case would be you have a tested base die (but no upper die yet) mounted onto a package substrate. The substrate provides standard ball-grid connectivity to a conventional IC tester socket. But, all TSVs and micro-bumps are inaccessible to probing. Only on-die DfT is available to support testing.

3.2.1. Base Die

Perhaps no bare-die test of TSVs and micro-bumps is feasible. Then a base die may have to be packaged and bonded (but not sealed) to its package substrate. This package can be placed on a conventional IC package tester socket. All the package I/O can be tested with the combination of tester channels and 1149.1 EXTEST resources working in concert. The topside micro-bumps, using an independent test instruction (something like EXTEST focused on topside interface) could be used to look for shorts among the micro-bumps. Open or resistive micro-bumps (or missing micro-bumps) could not be tested. These must wait for the bonding of the next die.

3.2.2. Die-to-die interfaces

Given the base die is tested as completely as possible, then the next die can be bonded atop it. This connects the next die power/ground paths and also enabled access to the DfT in the next die. The bonding of this interface now allows resources in the base die to coordinate with resources in the next die to work across the interface boundary. If a topside test instruction in the base die is invoked, and a complementary bottom side instruction in the next die is coordinated with it, then a variety of test (limited by the DfT specifications) can be exercised across the interface. An obvious candidate is something like EXTEST to look for shorts and opens in the interface connectivity, on all connections in parallel. Additional DfT capability could be provided to look for ranges of resistive shorts/opens, if those are deemed important defect mechanisms. This capability might not be able to work on all the connections at once, so it might have to be a one-path-at-a-time serial process, again depending on the implemented DfT capability.

3.3. Hybrid tests

A “hybrid” test combines the resources needed for testing without probes (section 3.2) with some number of additional resources commonly associated with probed testing. Think of it as probed testing with access to the package interface (perhaps limited to power/ground and TAP port pins) and some number of additional tester resources contacting TSV micro-bumps on some upper level die that is currently the “top” die. In this model there could be two approaches; first, a classic probe fixture is positioned over the top die and pressed into contact. In a second, a micro-sized version of a flying probe tester is applied which can contact perhaps 2 or 3 additional points, but these can be selected and changed over time to achieve testing goals. Clearly there are significant mechanical engineering challenges here, but if there is a good testing benefit, maybe that pays for this engineering.

4. Test Facilities

This chapter examines some test facilities that could be used to detect and help isolate specific defects. As before, this examination is focused on the new test problems introduced by 3D stacking and assumes that we still have to test for circuitry and metallization defects in die as before.

This chapter is split into a discussion of die-level facilities that would be used during pre-bond testing. The second part looks at the facilities needed for post-bond testing. In some cases it may be obvious that some facilities apply to both testing situations, and this would be useful, resulting in potential cost savings.

4.1. Die level facilities

This section looks at what defects can be tested before die bonding happens.

4.1.1. Pin-hole defects

A pin-hole defect introduces a leakage path for current from TSV to the substrate. Here we assume the substrate is grounded, but that it may have a substrate impedance large enough that it cannot be neglected. This gives a general model shown in Figure 10. This model includes the pin-hole resistance RP and the substrate resistance RG. The capacitance of the TSV body to the substrate, CS, is also shown. In some test cases, this capacitance may be a factor. Here we think of relatively slow (almost DC) measurements where the effects of the capacitor charging or discharging are negligible. Care must be taken to re-examine this assumption from time to time to make sure it is valid.

This model also assumes that there are no other TSV defects present – meaning the series impedance from top to bottom is negligible and is not included in the model.

The active circuitry of the die can be connected by metallization to the top of the TSV. We postulate a simple test facility composed of a simple driver with a selector control that may choose one of some small number of driver strengths – that is, it can modulate the impedance of the driver between its output and a positive voltage source V (or ground). This is shown in Figure 11A.

Along with the driver is a comparator which monitors the driver output by comparing it to a threshold voltage that can be selected. At this point no detail is given about how this threshold is provided or selected. It could be a single wire with an analog voltage on it, or it could be one or more digital control wires that select a reference voltage inside the comparator. This is immaterial to the present discussion.

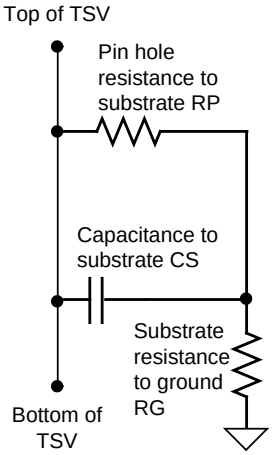


Figure 10: General equivalent circuit of TSV pinhole leakage.

The output of the comparator is a single bit "Hi/Lo" which indicates if the driver's voltage is above/below (1/0) the selected reference voltage. Then, Figure 11B gives a modified model of the test setup where a positive voltage is connected to ground via the driver resistance RS, through the pin-hole impedance RP, through the substrate resistance RG and finally to ground. An equation for the voltage VP is shown. The voltage VP is what the comparator measures against the selected threshold.

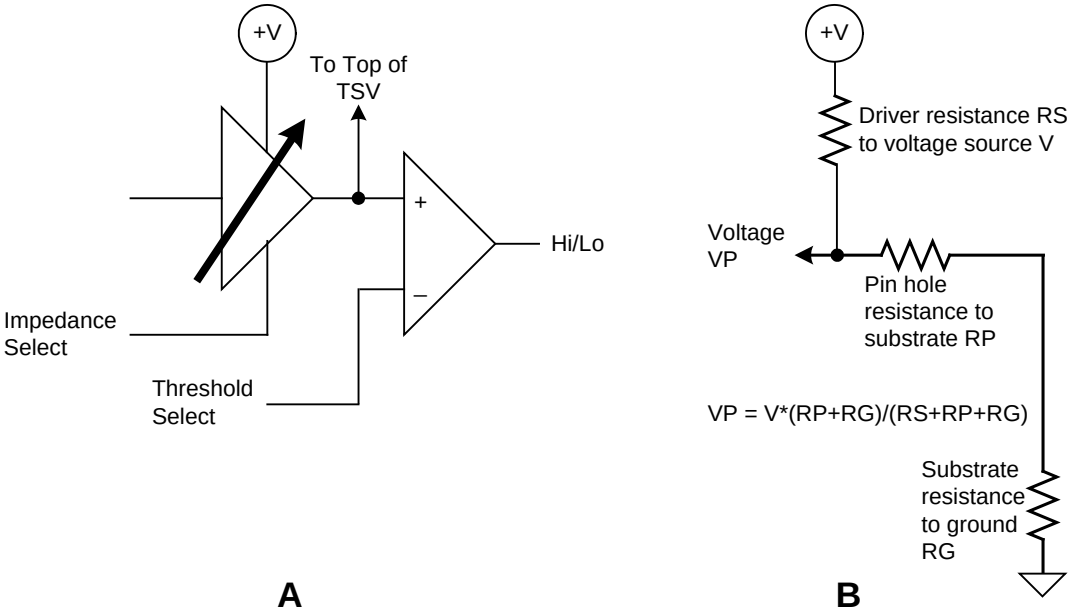


Figure 11: Test facility (A) and equivalent circuit (B) for testing a TSV pin-hole.

The goal of this facility it to allow some relatively crude but meaningful measurement of the value of RP. If there is no pin-hole defect, then RP is effectively infinity and the ratio of the two resistance sums is effectively 1.0

and thus VP will equal V. When a pin-hole defect occurs, this gives a lower value of RP and the ratio declines, reducing VP. A chart of some VP curves is given in Figure 12. (Note the binary log scale on the horizontal axis.) A second chart in Figure 13 shows the same family of curves, but with substrate resistance RG reduced from 20 to 2 ohms.

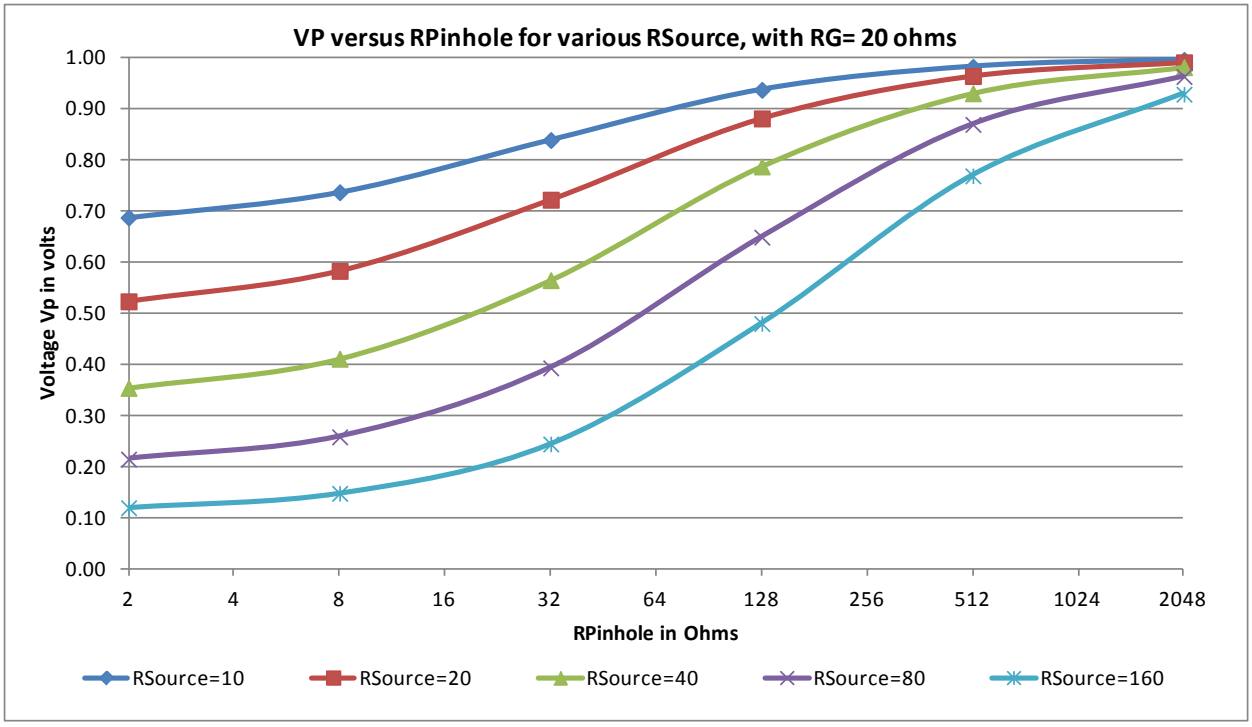


Figure 12: Chart of VP versus RP for some values of RS (with RG=20 ohms in all cases).

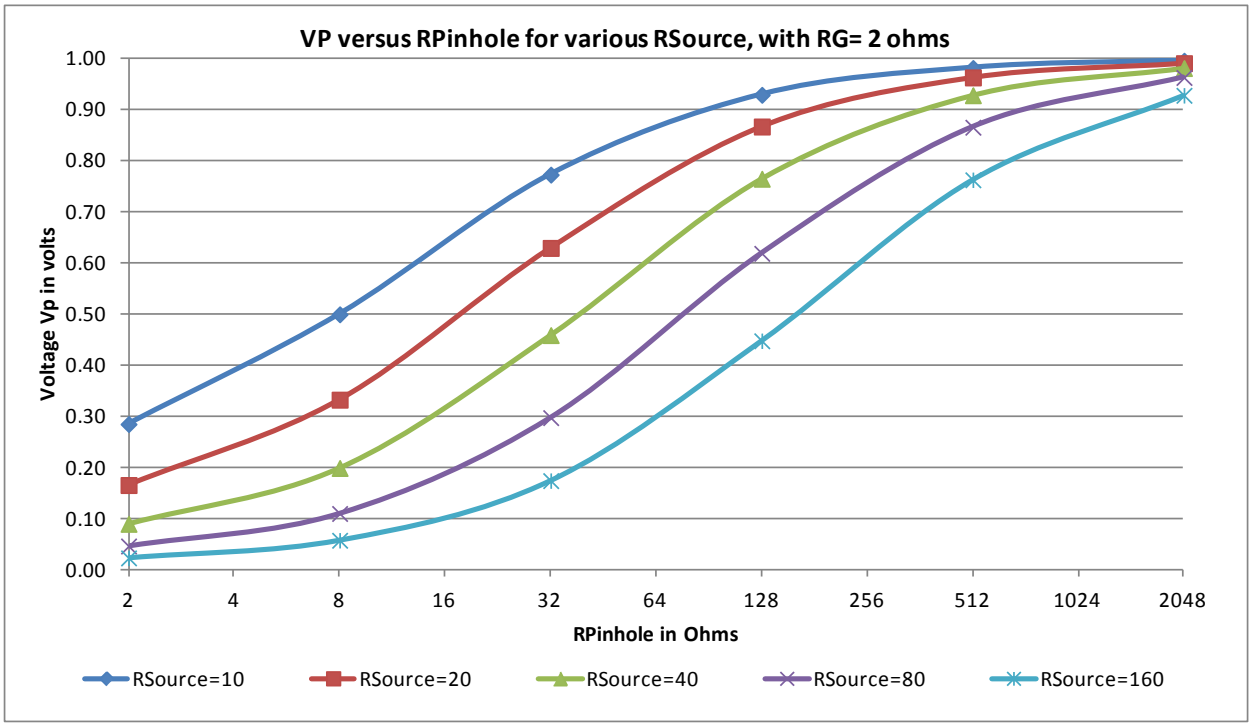


Figure 13: Chart of VP versus RP for some values of RS (with RG=2 ohms in all cases).

Examining Figure 13 if we had two threshold voltages, 0.3 and 0.7, we can run tests with various selections for RS and see the following table of possible results:

RS in ohms (note RG = 2)	For Vthreshold 0.3 volts	For Vthreshold 0.7 volts
	Hi/Lo compare fails (0) when RP is:	
10	< 2 ohms	< 24 ohms
20	< 7 ohms	< 45 ohms
40	< 15 ohms	< 100 ohms
80	< 32 ohms	< 180 ohms
160	< 64 ohms	< 400 ohms

This table show how repetitive testing with a selection of settings for RS and Vthreshold can determine a value of pin-hole impedance RP to some level of accuracy. In normal testing one might only want to run a single drive level and one Vthreshold level as a go/no-go test, since a value or pin-hole impedance below some critical value (say 100 ohms) may be considered to be too much leakage. For the purposes of characterization of pin-holes, subsequent tests using more drive levels and thresholds may be worth the time.

It is possible, given programmable drive and threshold levels, to test for TSV pin-holes in parallel, if RG is sufficiently low to keep interactions between TSVs low. Each TSV could be given independent control of the drive level and threshold, at the cost of additional circuitry. Or, all could share the same selection circuitry meaning all would execute test steps with the same selections. Then it might be necessary to run more selections and then sort out the TSV results if there was some expected variability among them – for example, some are allowed to leak more than others.

4.1.2. Opens inside TSVs

TSVs in die may have opens within them. Then the model in Figure 14 shows how the connectivity from the top of the TSV to the bottom is modified.

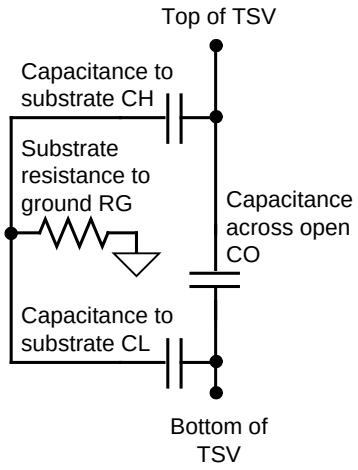


Figure 14: Model of a TSV open.

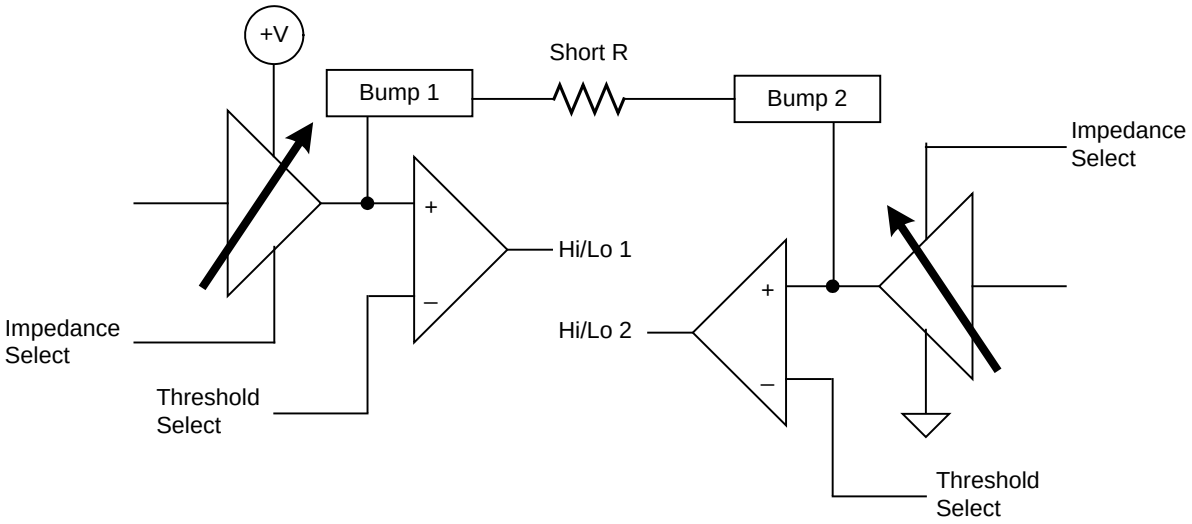
If we have probing access to the bottom of the TSV, we could use the same driver/comparator circuit in Figure 11A to stimulate the TSV. The access probe could be simply grounded. If there was a conductive path, then the driver would not be able to drive the TSV high (indicating connectivity, meaning the test passed). If there was an open, then with a small delay, the TSV could be driven high. The delay would be a function of the driver's impedance and the capacitance to the substrate via the three capacitances shown. The delay would likely be quite small. Such a test could be run on many TSVs in parallel, for those that have probe access.

If the open was not complete, that is, it was resistive, then there would be a resistive DC path to the access probe. This would form a voltage divider much like that exploited in section 4.1.1, and using combinations of driver impedance and voltage thresholds, the amount of resistance could be measured to some degree of accuracy based on the selection of driver impedance and comparison thresholds.

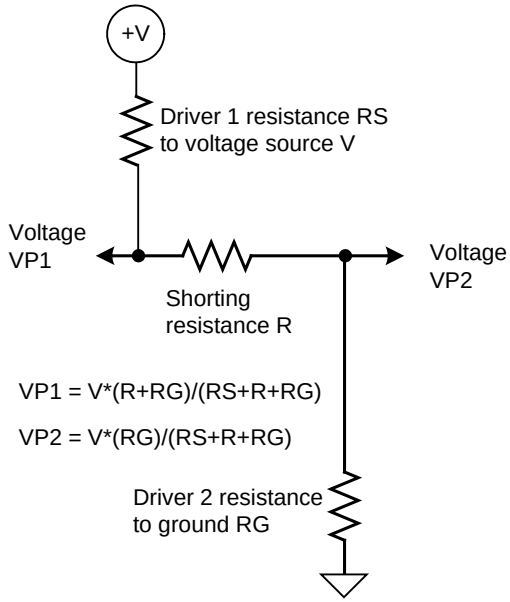
Without an access probe to the bottom of the TSV, it would be more difficult to determine if there was an open. Experiments could be run with putting transitions on the driver (with varying impedances). The comparator would see these same transitions delayed in time due to the RC constant of the driver impedance and the open capacitance to the substrate. The amount of delay could be very small. This is quite reminiscent of typical delay tests

4.1.3. Classic shorts between TSVs and/or micro-bumps

Consider two micro-bumps that are close enough to experience a shorting defect. If each micro-bump had the same driver/comparator circuit in Figure 11A, then at the pre-bond test stage the testing circuit in Figure 15 would exist, where a short is shown as a resistance that could be close to zero ohms, or it could be a resistive short. One driver would be driving a high voltage and the other a low voltage, with selectable on-resistance. Further, both comparators are available with programmable thresholds. Then Figure 15 shows how two micro-bumps can be stimulated to opposite states with an unknown shorting resistance R between them. Figure 16 gives an equivalent circuit for the test.



394 **Figure 15: Test facility for testing two shorted micro-bumps.**



395 **Figure 16: Equivalent circuit for shorted micro-bump test.**

396 Figure 17 then shows a chart for the behavior of this circuitry, which needs some explanation. Two groups of
397 5 traces each are plotted. Five are for VP1, on the drive-high side (micro-bump 1) of the short, and these are given
398 labels like "RDrvHi=10" which means the micro-bump 1 driver has 10 ohms to the +V voltage. The second group of
399 five traces are labeled like "RDrvLo=160, which means the micro-bump 2 driver has 160 ohms to ground. Note in
400 all cases, *both* drivers are using the same resistance setting – that is, we don't expect individual control of each
401 driver's impedance, so the traces should be considered in pairs, for example, RDrvLo=20 is paired with RDrvHi=20.
402 So, all the micro-bump 1 drivers start in the vicinity of 0.5 volts (for very low short impedance) and more upwards
403 to near 1.0 volts for high short impedance. The same is true for the micro-bump 2 voltage, except it trends lower
404 with rising short impedance.

405 Now, assume that both comparators are sharing the same Vthreshold selection. This means if the threshold is
406 set above 0.5 volts, then only the five traces for micro-bump 1 will be able to pass/fail depending shorting
407 resistance. The micro-bump 2 voltage will always be below that threshold and show a Hi/Lo result of for any
408 shorting resistance. The same situation will appear with micro-bump 1 and micro-bump 2 reversed in results, when
409 the threshold is set below 0.5 volts. This is to say, only one of the two micro-bump comparators can give meaningful
410 results.

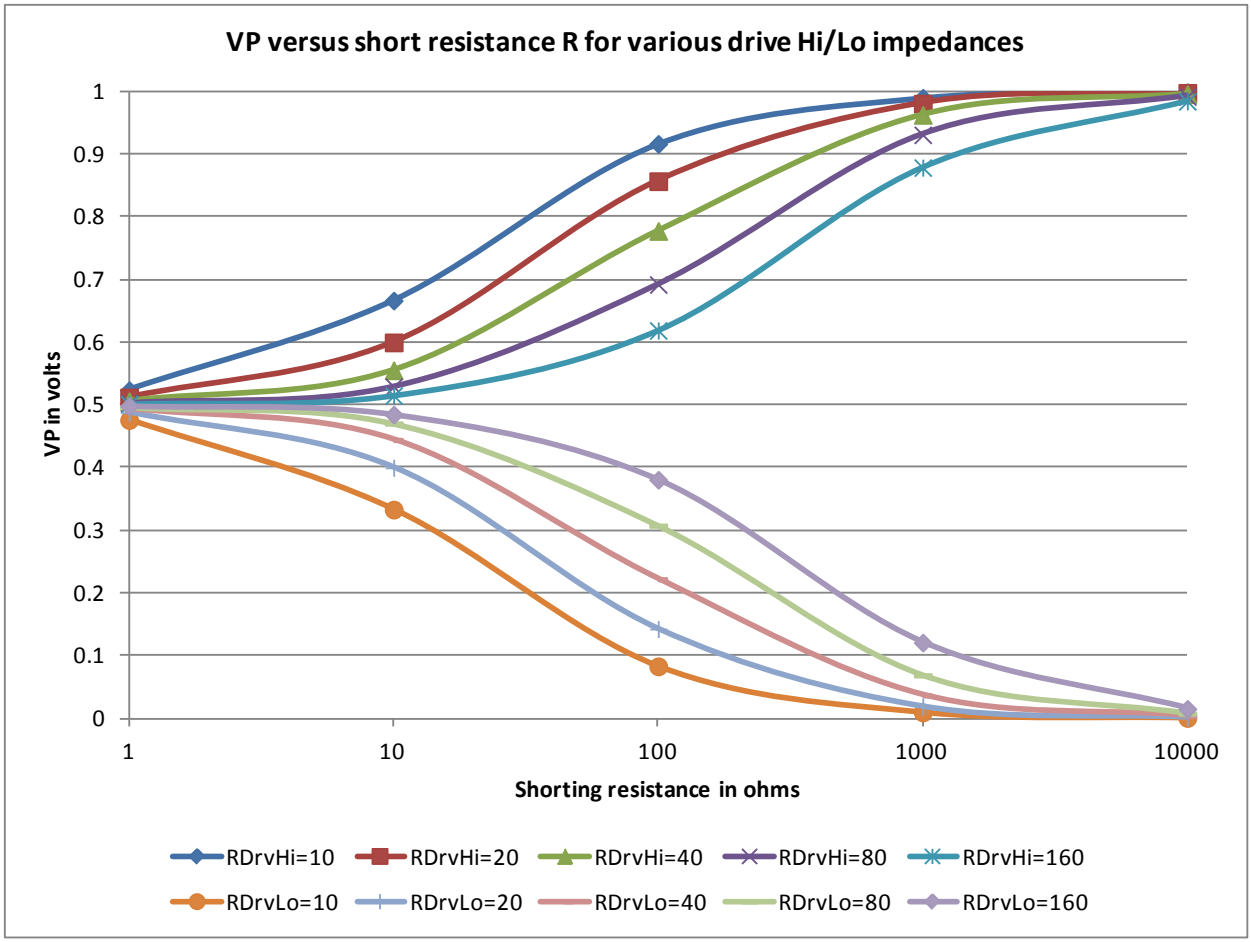


Figure 17: Chart of the voltages at VP1 and VP2.

So, picking the micro-bump 1 comparator, set the threshold to (say) 0.6 or 0.7 volts. Then the next table gives test results:

Driver (both hi/low) impedance in ohms	For Vthreshold 0.6 volts	For Vthreshold 0.7 volts
	Micro-bump 1 Hi/Lo compare fails (0) when short resistance R is:	
10	< 4 ohms	< 15 ohms
20	< 10 ohms	< 30 ohms
40	< 20 ohms	< 65 ohms
80	< 50 ohms	< 100 ohms
160	< 95 ohms	< 600 ohms

This demonstrates the ability to detect shorts that have a range of impedance which can be estimated by running several passes of the test with varying driver strength and comparison thresholds.

4.2. Post-bond facilities

After two dies are bonded together, we have resources at the topside micro-bumps of the lower die, and at the top of the TSVs in the upper die. Assuming we start with the base die and put the next mid/upper die upon it, we have the structure in Figure 6. The two dies can cooperate to perform tests. It is assumed that we have at least enough test access to the base die to provide power and to manipulate the on-die test resources, for example, a TAP.

4.2.1. Classic shorts/opens between TSVs

The bonding process may produce shorts between adjacent TSVs, for example, due to a small registration defect, or extrusion of tin metal that bridges between TSVs. The short could be very low impedance, but could have

an elevated impedance if the connection is marginal. The process used in section 4.1.3 would be sufficient to discover such shorts. It would also be possible to test many TSVs in parallel if we have the ability to control groups of TSV and micro-bump resources in concert. Basically, we could implement an EXTEST-style test capacity at an individual upper or lower interface. Again, the drive impedances and compare thresholds could be shared rather than individually controlled. This would allow for a mass test of TSVs for resistive shorts and a crude estimation of their magnitude.

4.2.2. TSV opens and resistive connections

A bond from the lower to upper die at an interface could be open, or resistive. For example, a defect that omitted a micro-bump, or, an untested open within a TSV could now reveal itself. In this case, topside micro-bumps in the lower die can be driven to a voltage, and the top of the connected TSV in the upper die can be driven to a different voltage. If there is no connectivity (an open defect) then both drivers would achieve their intended voltage which could be observed by the related comparators, indicating "fail". If good connectivity was achieved, then, just as for the test for shorts used in section 4.1.3, one of the comparators would fail (which means "pass"). Again by manipulating drive impedances and compare thresholds, marginal connectivity values could be estimated, and this type of testing could be done on many TSVs in parallel.

5. DFT resources

This study has postulated some test circuitry (such as in Figure 11A) and some simple implementations are shown next for the purpose of estimating the circuitry cost of such resources. FET-type transistors are used.

5.1.A selectable impedance driver

Part A of Figure 18 shows a very simple driver that could be used to drive a TSV or micro-bump. Part B shows two additional stages of drive that can be enabled with two select signals.

NOTE: The circuitry in Figure 18 is conceptual, for illustration purposes, and not a recommended design.

When either or both stages are enabled, the driver impedance goes down. If, for example, each FET had a 200 ohm on-resistance, then the driver could have these impedances for the Select 1/2 lines having values of 00, 10, 01, and 11: 200 ohms, 100 ohms, 66 ohms and 50 ohms respectively. Obviously, other values (or more values) can be implemented. Note that when the select lines are both 0, then the six added transistors are all off, minimizing their current drain and loading effects.

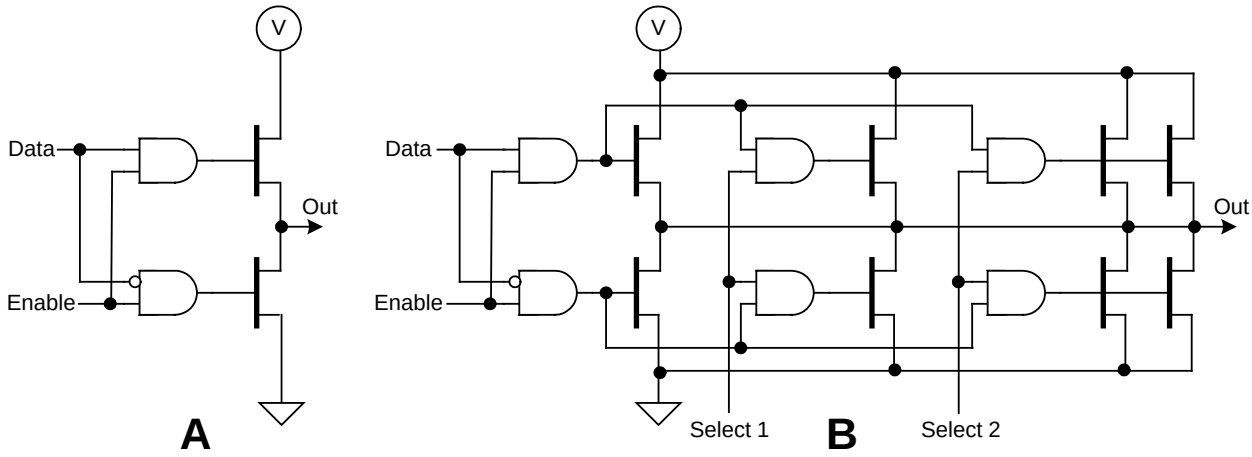


Figure 18: A conceptual driver (A) and a driver with 4 selectable drive impedances (B).

So, one could replace the TSV/micro-bump drivers in part A with the selectable impedance driver in part B, or, they could both be connected to the TSV/micro-bump, with only one being enabled depending on whether we are testing or operating normally. This might be necessary if the mission mode driver needs special characteristics incompatible with being part of a merged design. Note that the variable impedance driver does not need to have

special properties such as the ability to transition very quickly, as testing operations are likely to be lower-speed. Small transistors may be used to save space, reduce loading, etc.

5.2.A selectable threshold comparator

Figure 11A also shows a threshold comparator with a selectable threshold. Two choices for implementing this capability are considered as depicted in Figure 19.

NOTE: The comparator circuitry in Figure 19 is conceptual, for illustration purposes. The actual design is beyond the scope of this discussion.

First, an analog signal generated on-die could be routed to each comparator's negative input at a die interface (lower TSV or upper micro-bump). This would be a centralized resource shared by all the interface comparators so it could be fairly capable, generating a range of voltages. Second, at each comparator, a local threshold level could be generated, with individual control provided by a small local register. An alternative might be a hybrid of these choices, where there are several on-die threshold generators that are then distributed to groups of comparators, which might be useful if there are several "families" of logic levels in use on the die.

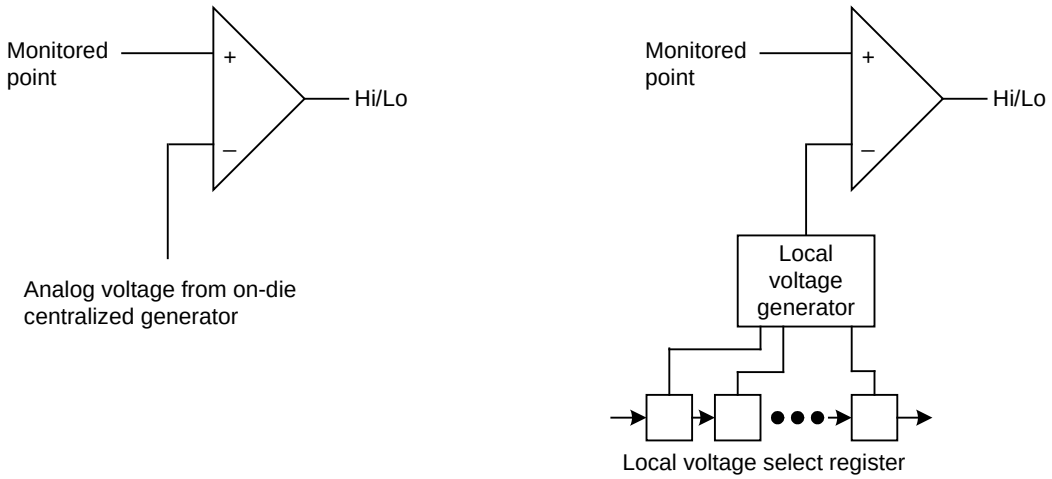


Figure 19: Two choices of threshold generation used by voltage comparators.

Note that the comparator and voltage generator might have an on/off control that removes them as power consumers when not needed for testing (not shown).

5.3.A way of controlling/monitoring the DFT resources

Figure 20 shows a portion of a TSV on a die (part A) and how DFT resources with control and observation capability might be added in part B. (The control and observation are patterned after that given by 1149.1.)

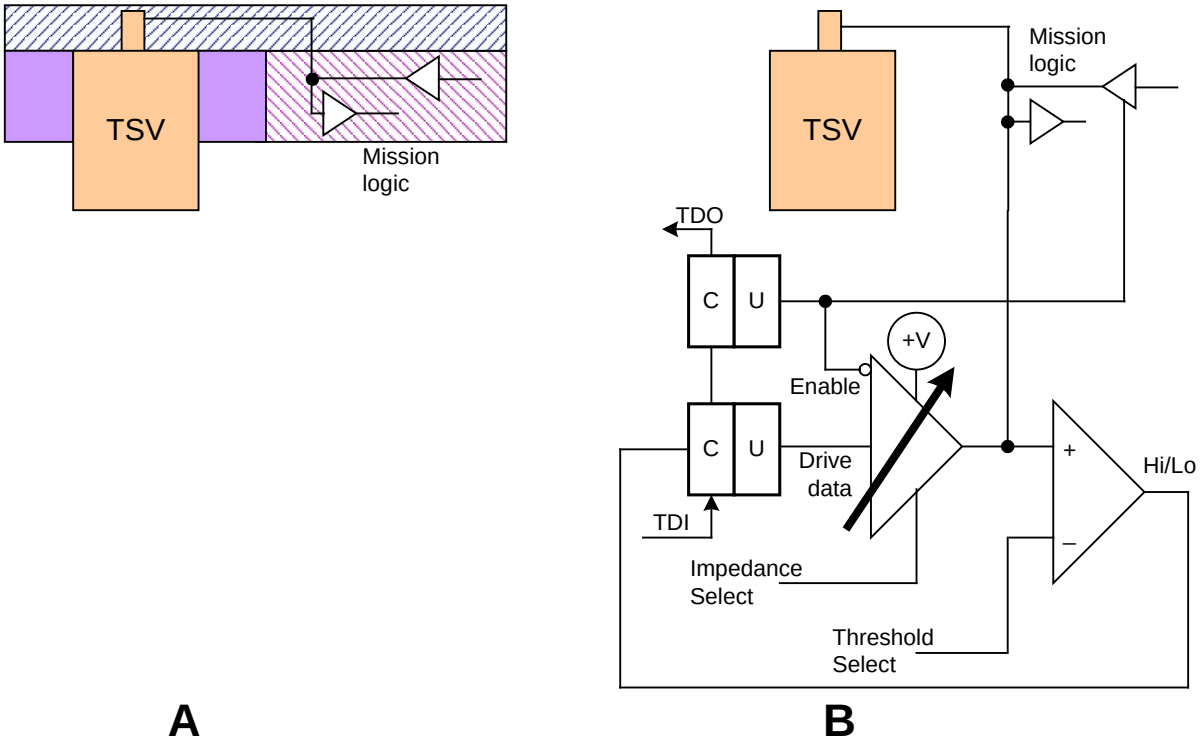


Figure 20: TSV (A), and modified with added variable driver, variable compare and control/observe capability (B).

Note that the original mission driver has been changed to have an enable input, so it can be shut off during testing. That control is shared (in this figure) with an enable for the test driver such that both are mutually exclusive. At the cost of another boundary register cell, they could be made independent.

5.4.A quick look at DFT area cost

The defect tiger team examined the cost of DFT in terms of circuit area needed in the vicinity of TSVs and micro-bumps. As is typically true in modern ICs, the total area cost of DFT across an entire IC is usually minimal. Using Boundary Scan (1149.1) as an example, the area consumed by the TAP, instruction register and decode, bypass register, idcode register and several boundary register cells per I/O pin is small for typical ICs.

By polling several IC companies, we found that a typical 1149.1 "BC_1" cell design takes about 14 um^2 area (for a 40 nanometer IC process). A given I/O pin in an IC might need between 1 and 3 such cells, but compared to the size of the I/O pad design, this can be a small percentage of the area. TSVs are much smaller than normal I/O pins. There is some question whether they still need electrical static discharge protection circuitry (which we have assumed is not needed). TSVs and micro-bumps may be limited (for now) to a 40 um pitch (or 1600 um^2) as shown in Figure 2. A dense array of TSVs could look like what is shown in Figure 21, where each TSV/micro-bump pair has a pink-shaded DFT addition (a BC_1-equivalent). The TSV copper area for 2.5 um radii is 19.6 um^2. What is quite variable is the area of the Keep Out Zone (KOZ) and we don't have numbers for it. Neglecting KOZ area, we see that at 40 um pitch, the 40x40 area which contains both the TSV copper and a single BC_1 cell, we have "lost" 43.6 um^2 or about 2.7% of the circuitry area. The TSV/DFT area of Figure 20B would be 19.6 + 2*14 = 47.6 um^2, plus the added area of the variable driver and variable comparator.

We have no feeling today about what the size of this DFT circuitry might be needed. If, as we have shown, a variable strength driver and some form of variable threshold receiver is needed at most TSVs and micro-bumps, then this will consume available silicon area in the vicinity of same. Some number of controlling cells (a'la BC_1) would also be needed to enable and drive/observe these resources. The parameters needed for selecting drive strength or compare thresholds could be shared across many TSVs and micro-bumps. The number of strength or threshold levels would be a design criteria (consuming more area for more flexibility). It should be emphasized that both the variable driver and variable comparison should be kept as simple as possible for the needs they should fulfill. They only support low-speed test functions and need not have complex features, unless they are actually functionally

merged with the system circuitry, which could be yet another strategy. Note too that an upcoming revision of the 1149.1 standard makes provisions for selecting analog parameters found in some of today's device drivers and receivers. That is, the device's function may have some programmable pin features; these could be re-used during testing to provide programmable test drive and receive thresholds.

Clearly, if the pitch of TSVs were tighter, the fraction of area consumed by TSV/DFT would rise commensurately, and of course, for smaller processing technology (below 40 nm) less area would be consumed by DFT. But if the total area consumed with dense TSV arrays is a smaller part of the total die area, then the main concern is for the DFT part of the area per TSV be able to fit and not displace too much area desired for mission circuitry. This will have to be analyzed each time, taking into account TSV pitch, size of DFT circuitry (taking into account options like those seen in Figure 19) and the KOZ area for that process technology.

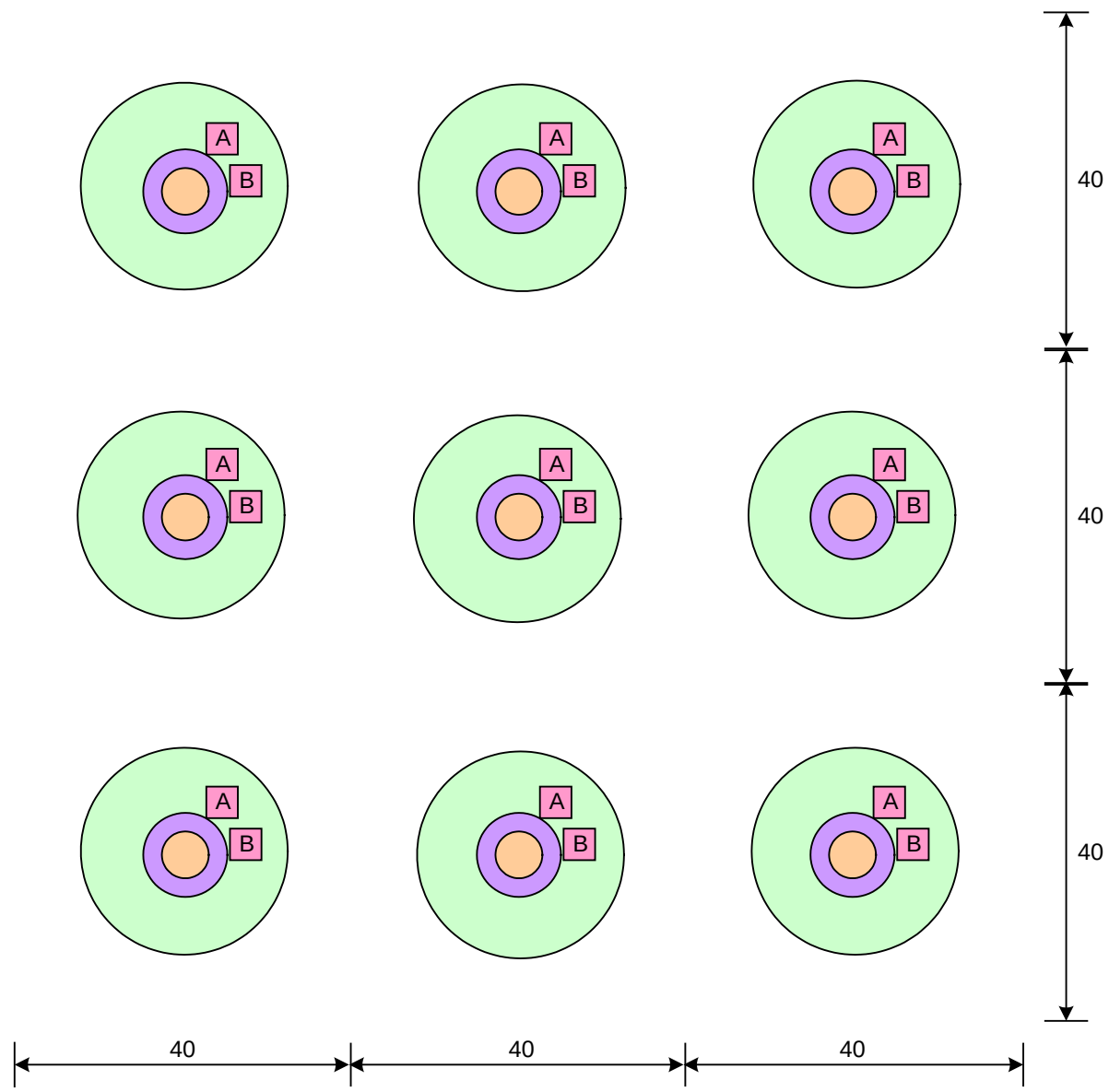


Figure 21: Dense array of TSVs or micro-bumps.

6. Defect detectability summary

The following table (with notes) summarizes what defects can be tested, pre- and post-bond. Tests can be run in parallel in most cases, although testing can focus on parallel go/no-go or serialized multi-threshold and multi-strength strategies for more accuracy.

If postbond testing is performed after each die is attached, then it will probably be a good idea to focus test capability on each interface layer, such that the bottom micro-bump layer of the topmost die is cooperating with the

top micro-bump layer of the next die down. Using 1149.1-like nomenclature, we might want to have a "EXTEST_TOP" and "EXTEST_BOTTOM" instruction that allow this test coordination across a bonding interface. Conceivably you might also want to test multiple interfaces at one time in a stack (for throughput) and that would use an "EXTEST_BOTH" instruction.

Pre or Post Bond	Defect	Testable?	Notes
Prebond	Pin Hole	Yes	1, 2, 3
	Opens in TSV	No (see postbond)	4, 5
	TSV-TSV or Micro-bump-Micro-bump Short	Yes	1, 2
Postbond	Pin Hole	Yes	6
	Opens in TSV	Yes	1, 2
	TSV-TSV or Micro-bump-Micro-bump Short	Yes	1, 2
	TSV-Micro-bump opens	Yes	1, 2

Notes:

1. May test multiple cases in parallel.
2. Using multiple drive strengths and thresholds, can home in on a resistance value measurement.
3. Adjacent pin holes may interact via common substrate resistance.
4. No practical DC test available (without external contact).
5. If an external fixture can contact the bottom micro-bump of a TSV, then an open can be sensed, even if the external fixture can only provide is a ground point. The "NO" answer holds when such contact is not possible.
6. Only use TSV driver, turn off micro-bump driver in other dies. Assumes no micro-bump leakage to ground.