Submission to
IEEE P802.11
Wireless LANs

Harris/Lucent TGb
Compromise CCK (11Mbps) Proposal

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Harris Semiconductor

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Lucent Technologies

KEY FEATURES

• 11 and 5.5 Mbps data rates
• Outstanding high-multipath performance
• Outstanding low-SNR performance
• Seamless interoperability with existing DS and FH
• Clean, extensible receiver architectures enabled
• Maintains QPSK chips at 11 MHz chip rate
• Maintains 3 frequency channels
• FCC and MKK regulations satisfied
MERGER EASE

- **HARRIS**
  - Codeword change only
  - Modified QMBOK

- **LUCENT**
  - Codeword change
  - Do not position modulate

COMPROMISE ADVANTAGES RELATIVE TO LUCENT’S MAY PROPOSAL

- 4 dB less PA Backoff.
- RAKE receiver foundation maintained.
- RAKE married to HARRIS’s Equalizer simplifies design over BCPM TSE/MS.
- 11 Mbps 1K byte packet performance.
  - May: 130 nsec
  - July: 226 nsec at lower complexity
COMPROMISE ADVANTAGES RELATIVE TO HARRIS’S MAY PROPOSAL

MULTIPATH ROBUSTNESS
- RMS delay spread
- Bigger is better
- 64 byte packet
- 5.5 Mbps: MAY 226 nsec, JULY 450 nsec
- 11 Mbps: MAY 186 nsec, JULY 330 nsec

NOISE ROBUSTNESS
- Eb/No dB
- Smaller is better
- With Equalizer
- 5.5 Mbps: MAY 25.2 dB, JULY 17.7 dB
- 11 Mbps: MAY 24.7 dB, JULY 17.7 dB

ARCHITECTURE
- Design ease
- Gate count
- Power draw
- 1, 2 Mbps: MAY RAKE, JULY RAKE and Equalizer
- 5.5, 11 Mbps: MAY FF/FB Equal, JULY RAKE and Equalizer

COMPROMISE OR NEW PROPOSAL?
CLEARLY A COMPROMISE BECAUSE
- BPSK or QPSK chips are used (Harris)
- 1-and-2 MBps DSSS-like signal (Lucent & Harris)
  - Phase-modulated codewords
- 11 Mcps rate maintained (Harris & Lucent)
  - Spectrum (bandwidth) unchanged
- Next Generation-QMBOK (Harris) codeword called CCK used
- Seamless interoperability maintained with DS and FH
- Merged architecture: RAKE (Lucent) with Equalizer (Harris)
PERFORMANCE:
WAVEFORM Versus RECEIVER

PERFORMANCE ENABLERS

TRANSMIT SIGNAL DESIGN

- Distance properties

RECEIVER DESIGN

- Wide choice range
- Does it fully exploit Tx signal features?

SIGNAL DESIGN

TESTPOINT
5.5 MBPS
8 CHIP CODEWORDS

SIMULATION ASSUMPTIONS
6 Finger RAKE RCVR
8 Samples/chip CIR Decimated To 1

<table>
<thead>
<tr>
<th>DELAY SPREAD nsec</th>
<th>MBOK CoverCode 03 h</th>
<th>MBOK CoverCode 12 h</th>
<th>CCK 4-ARY</th>
</tr>
</thead>
<tbody>
<tr>
<td>50</td>
<td>225</td>
<td>320</td>
<td></td>
</tr>
</tbody>
</table>
CODEWORD STUDY

- Jointly performed comprehensive codeword study
- Examined 8, 11 and 16 chip codes
- Examined WALSH and cover codes
- Examined real-chip (MBOK) versus complex-chip (CCK) codes
- Computed matched-filter-bound to examine fundamental distance properties in multipath
- Jointly-examined against receiver architectures
- CCK gave best overall performance and architecture

I/Q MULTIPATH CORRUPTION

- HARRIS'S Quadrature-MBOK
- LUCENT'S Quadrature-BCPM
- CORRUPTED BY MULTIPATH PHASE ROTATIONS

SOLUTION:
Serially-Encode QPSK chips
CODE DIMENSIONALITY

8 BPSK CHIPS: \(2^8 = 256\) Codewords

\[\begin{array}{c}
\text{8 QPSK CHIPS: } 4^8 = 65536 \text{ Codewords}
\end{array}\]

COMPLEMENTARY CODES

8 Chip/4 Phase \(\phi: 0, \pi/2, \pi, 3\pi/2\)

\[c = \{e^{j(\phi_1+\phi_2+\phi_3+\phi_4)}, e^{j(\phi_1+\phi_3)}, e^{j(\phi_1+\phi_2+\phi_4)}, e^{j(\phi_1+\phi_4)}, e^{j(\phi_1+\phi_3+\phi_4)}
\]

- Directly encodes complex (QPSK) chips
- \(\phi_1\) quadriphase rotates whole codeword
- 64 codewords before quadriphase
- 256 codewords after quadriphase (8 bits)
- 2 bit sign, 6 bits codeword select
- Fast-Walsh-transform like decoder
NAME CHANGE UNAVOIDABLE

- **QMBOK**: Quadrature M-ary Bi-Orthogonal Keying
- QMBOK does not make sense for new modulation
- Not quadrature, not orthogonal (only nearly orthogonal), not bi-orthogonal
- Still 8 chip
- CCK -- Complementary Code Keying

DIFFERENTIAL-PHASE MODULATE CODEWORDS

- Like 1 and 2 Mbps
- Noncoherent Rcvr Enabled
RAKE DESIGN RULES

<table>
<thead>
<tr>
<th>RULE</th>
<th>HIGH-RATE INDOOR WLAN</th>
<th>VIOLATION PENALTY</th>
</tr>
</thead>
<tbody>
<tr>
<td>Symbol Duration Must Be Much Greater Than Multipath Spread</td>
<td>200 nsec gives 0.25 - 0.5 Symbol Overlap</td>
<td>RAKE ISI Breakdown</td>
</tr>
<tr>
<td>Autocorrelation Must Be Impulsive And Cross Correlation Zero</td>
<td>8-16 chips is too small to be effective</td>
<td>Freq. Selective RAKE ICI Breakdown</td>
</tr>
</tbody>
</table>

RECOMMENDED RAKE RCVR EXTENSIONS

- RAKE rcvr alone works great for 1 and 2 Mbps
- At high data rates, multipath impairments limit the performance of a RAKE
- HARRIS/LUCENT recommend extensions which enable high-performance at 11 Mbps
INDOOR MULTIPATH EXAMPLE

**IMPULSE RESPONSE PROFILE**

100 nsec RMS Delay Spread

ENVIRONMENT: COMMERCIAL/ FACTORY

300 nsec RMS Delay Spread
**MULTIPATH: ISI LOSS**

- InterSymbol Interference (ISI)
- Symbols Smeared Together
- Previous Symbol: Post-Cursor ISI
- Preceding Symbol: Pre-Cursor ISI
- Primary RAKE Failure Mechanism for 802.11

![Channel Impulse Response](image)

**MULTIPATH: ICI LOSS**

- InterChip (sub-symbol) Interference (ICI)
- Chips Smeared Together
- Previous Chip: Post-Cursor ICI
- Preceding Chip: Pre-Cursor ICI
- Codeword Orthogonality Lost
- Codeword Equal-Energy Lost
- Secondary RAKE Failure Mechanism for 802.11

![Symbol’s Chips Smeared](image)
ISI/ICI MITIGATION IN PRE-JULY PROPOSALS

<table>
<thead>
<tr>
<th>LUCENT</th>
<th>HARRIS</th>
<th>ALANTRO</th>
<th>MICRILOR</th>
</tr>
</thead>
<tbody>
<tr>
<td>• Codeword Design</td>
<td>• Codeword Design</td>
<td>• Rate 1/2 CODE</td>
<td>• Codeword Design</td>
</tr>
<tr>
<td>• TSE/MS MLSE</td>
<td>• CHIP DFE</td>
<td>• MLSE/DFE</td>
<td></td>
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</tbody>
</table>

HARRIS/LUCENT
• Codeword Design
• RAKE with ISI/ICI Equalizer

JULY’S PROPOSAL

CANONICAL ARCHITECTURES

<table>
<thead>
<tr>
<th>1 CHIP EQ.</th>
<th>2 RAKE RCVR</th>
<th>3 RAKE With ISI EQ.</th>
<th>4 RAKE With ISI/ICI EQ.</th>
</tr>
</thead>
<tbody>
<tr>
<td>low MULTI-PATH ROBUST</td>
<td>high</td>
<td>low</td>
<td>high</td>
</tr>
<tr>
<td>low NOISE ROBUST</td>
<td>high</td>
<td>low</td>
<td></td>
</tr>
</tbody>
</table>

Submission  Slide 21  Webster/Harris; Boer/Lucent
CHIP EQUALIZER

- 2 FF Taps (multiplies) and 10 FB Taps (adds)
- Sliding DFE algorithm minimizes FF Taps
- Lowest-complexity architecture
- 226 nsec multipath-spread testpoint at 11 Mbps
- 20.5 dB SNR testpoint at 11 Mbps (64 byte)

RAKE RECEIVER

- 6 tap Channel Matched Filter
- Second-lowest-complexity architecture
- 90 nsec multipath spread testpoint at 11 Mbps
- 15.5 dB SNR testpoint at 11 Mbps (64 byte)
RAKE WITH ISI EQUAL.

- 6 tap Channel Matched Filter
- Third-lowest-complexity architecture
- 144 nsec multipath spread testpoint at 11 Mbps
- 15 dB SNR testpoint at 11 Mbps (64 byte)

RAKE WITH ISI/ICI EQUAL.

- 6 tap Channel Matched Filter
- Highest-complexity architecture
- 333 nsec multipath spread testpoint at 11 Mbps
- 15.5 dB SNR testpoint at 11 Mbps (64 byte)
RAKE WITH ISI/ICI EQUAL.
CORRELATOR DETAIL

Codeword # 3
Chips

\[ z^{-1} \]

\[ z^{-1} \]

\[ z^{-1} \]

\[ h_1 \]

\[ h_2 \]

\[ h_3 \]

Detection
Statistic for
Codeword # 3

Received
Signal

Correlator for
Codeword # 3

MAKE HARD-DECISION
FOR CODEWORD WITH
BEST STATISTIC

SIMILAR STRUCTURE FOR
ALL OTHER CODEWORDS

PER FOR MULTIPATH AND NOISE

<table>
<thead>
<tr>
<th></th>
<th>5.5 Mbit/s - CCK</th>
<th>11 Mbit/s - CCK</th>
</tr>
</thead>
<tbody>
<tr>
<td>Trms at PER=10%, noise free, 64b</td>
<td>226 nsec</td>
<td>186 nsec</td>
</tr>
<tr>
<td>Eb/No at PER=20%, with Trms at 10%, 64b</td>
<td>20.7 dB</td>
<td>21.2 dB</td>
</tr>
<tr>
<td>Trms at PER=10%, noise free, 1000b</td>
<td>221 nsec</td>
<td>183 nsec</td>
</tr>
<tr>
<td>Eb/No at PER=20%, with Trms at 10%, 1000b</td>
<td>25.2 dB</td>
<td>24.7 dB</td>
</tr>
<tr>
<td>RAKE with 6 tap CMF</td>
<td>Trms at PER=10%, noise free, 64b</td>
<td>273 nsec</td>
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<tr>
<td></td>
<td>Eb/No at PER=20%, with Trms at 10%, 64b</td>
<td>14.8</td>
</tr>
<tr>
<td></td>
<td>Trms at PER=10%, noise free, 1000b</td>
<td>226 nsec</td>
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<tr>
<td></td>
<td>Eb/No at PER=20%, with Trms at 10%, 1000b</td>
<td>18.5</td>
</tr>
<tr>
<td>RAKE ISI Equalizer w/ 6 tap CMF</td>
<td>Trms at PER=10%, noise free, 64b</td>
<td>509 nsec</td>
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<td></td>
<td>Eb/No at PER=20%, with Trms at 10%, 64b</td>
<td>16</td>
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<tr>
<td></td>
<td>Trms at PER=10%, noise free, 1000b</td>
<td>430 nsec</td>
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<td>Eb/No at PER=20%, with Trms at 10%, 1000b</td>
<td>19</td>
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<tr>
<td>RAKE ISI/ICI Equalizer w/ 6 tap CMF</td>
<td>Trms at PER=10%, noise free, 64b</td>
<td>Not Needed</td>
</tr>
<tr>
<td></td>
<td>Eb/No at PER=20%, with Trms at 10%, 64b</td>
<td>Not Needed</td>
</tr>
<tr>
<td></td>
<td>Trms at PER=10%, noise free, 1000b</td>
<td>Not Needed</td>
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