In page 529, line 47, correct section 8.4.9.2.3.1 as shown below:

8.4.9.2.3.1 CTC encoder

The Convolutional Turbo Code defined in this section is designed to enable support of hybrid ARQ (H-ARQ). H-ARQ implementation is optional. The Convolutional Turbo Code encoder, including its constituent encoder, is depicted in Figure 240. It uses a double binary Circular Recursive Systematic Convolutional code. The bits of the data to be encoded are alternately fed to *A* and B, starting with the MSB of the first byte being fed to A. The encoder is fed by blocks of k bits or N couples *(k* = 2*N bits). For all the frame sizes *k* is a multiple of 8 and *N* is a multiple of 4. Further *N* shall be limited to: $8 \le N/4 \le 1024$.

The polynomials defining the connections are described in octal and symbol notations as follows:
— For the feedback branch: 0xB, equivalently $1+D+D^3$ (in symbolic notation)
— For the *Y* parity bit: 0xD, equivalently $1+D^2+D^3$
— For the *W* parity bit: 0x9, equivalently $1+D^3$

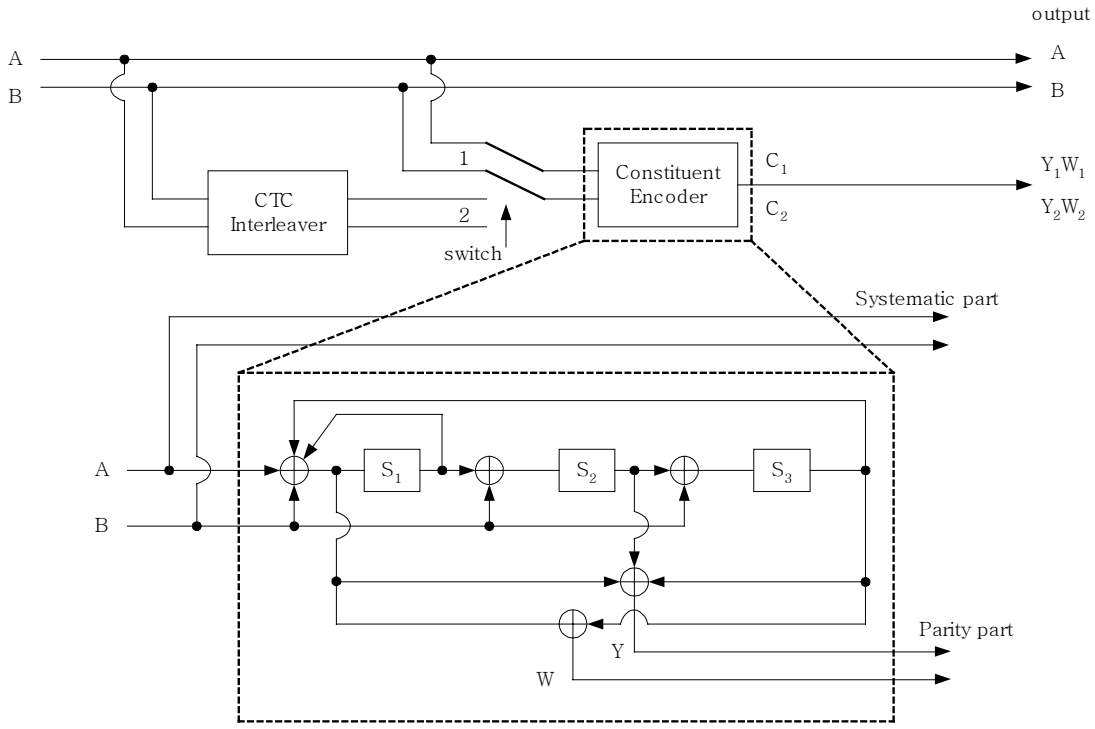

Figure 240—CTC encoder

First, the encoder (after initialization by the circulation state Sc_1, see 8.4.9.2.3.3) is fed the sequence in the natural order (position 1) with the incremental address $i = 0$ .. N–1. This first encoding is called S_{C1} encoding. Then the encoder (after initialization by the circulation state Sc_2, see 8.4.9.2.3.3) is fed by the interleaved sequence (switch in position 2) with incremental address $j = 0, \ldots$ N–1. This second encoding is called C_2 encoding.
The order in which the encoded bit shall be fed into the ~~interleaver (8.4.9.3)~~ subpacket generation block (8.4.9.2.3.4) is:

$$A, B, Y_1, W_1, Y_2, W_2 =$$
$$A_1, A_2, \ldots, A_N, B_1, B_2, \ldots, B_N, Y_{11}, Y_{12}, \ldots, Y_{1N}, W_{11}, W_{12}, \ldots, W_{1N}, Y_{21}, Y_{22}, \ldots, Y_{2N}, W_{21}, W_{22}, \ldots, W_{2N}$$

$$A, B, Y_1, Y_2, W_1, W_2 = A_0, B_0, \ldots, A_{N-1}, B_{N-1}, Y_{1,0}, Y_{1,1}, \ldots, Y_{1,N-1}, Y_{2,0}, Y_{2,1}, \ldots, Y_{2,N-1}, W_{1,0}, W_{1,1}, \ldots, W_{1,N-1}, W_{2,0}, W_{2,1}, \ldots, W_{2,N-1}$$

~~where *M* is the number of parity bits.~~
Note that the interleaver (8.4.9.3) shall not be used when using CTC

Table 284 gives the block sizes, code rates, channel efficiency, and code parameters for the different modulation and coding schemes. As 64-QAM is optional, the codes for this modulation shall only be implemented if the modulation is implemented.

The encoding block size shall depend on the number of subchannels allocated and the modulation specified for the current transmission. Concatenation of a number of subchannels shall be performed in order to make larger blocks of coding where it is possible, with the limitation of not passing the largest block under the same coding rate (the block defined by 64-QAM modulation). Table ccc specifies the concatenation of subchannels for different allocations and modulations. The concatenation rule shall not be used when using H-ARQ.

For any modulation and FEC rate, given an allocation of n subchannels, we define the following parameters:

j = parameter dependent on the modulation and FEC rate
n = number of allocated subchannels
k = floor(n / j)
m = n modulo j

(aaa)

Table bbb shows the rules used for subchannel concatenation,

Table bbb—Subchannel concatenation rule for CTC

Number of subchannels	Subchannels concatenated
n <= j n≠7	1 block of n subchannels
n=7	1 block of 4 subchannels 1 block of 3 subchannels
n > j	(k-1) blocks of j subcahnnels 1 block of L_{b1} subchannels 1 block of L_{b2} subchannels Where: L_{b1} = ceil((m+j)/2) L_{b2} = floor((m+j)/2) If (L_{b1} == 7) or (L_{b2} == 7) $L_{b1} = L_{b1} + 1$; $L_{b2} = L_{b2} - 1$;

Table ccc—Encoding Subchannel concatenation for different allocations and modulations in CTC

Modulation and rate	j
QPSK 1/2	j = 10
QPSK 3/4	j = 6
QAM16 1/2	j = 5
QAM16 3/4	j = 3
QAM64 1/2	j = 3
QAM64 2/3	j = 2
QAM64 3/4	j = 2
QAM64 5/6	j = 2

Table 284 gives the block sizes, code rates, channel efficiency, and code parameters for the different modulation and coding schemes. As 64-QAM is optional, the codes for this modulation shall only be implemented if the modulation is implemented. Table hhh shows code parameters for HARQ.

Table 256—Optimal CTC channel coding per modulation

Modulation	Data block size (bytes)	Encoded data block size (bytes)	Code rate	N	P0	P1	P2	P3
QPSK	6	12	1/2	24	5	0	0	0
QPSK	12	24	1/2	48	13	24	0	24
QPSK	18	36	1/2	72	11	6	0	6
QPSK	24	48	1/2	96	7	48	24	72
QPSK	30	60	1/2	120	13	60	0	60
QPSK	36	72	1/2	144	17	74	72	2
QPSK	48	96	1/2	192	11	96	48	144
QPSK	54	108	1/2	216	13	108	0	108
QPSK	60	120	1/2	240	13	120	60	180
QPSK	9	12	3/4	36	11	18	0	18
QPSK	18	24	3/4	72	11	6	0	6
QPSK	27	36	3/4	108	11	54	56	2
QPSK	36	48	3/4	144	17	74	72	2
QPSK	45	60	3/4	180	11	90	0	90
QPSK	54	72	3/4	216	13	108	0	108
QAM16	12	24	1/2	48	13	24	0	24
QAM16	24	48	1/2	96	7	48	24	72
QAM16	36	72	1/2	144	17	74	72	2
QAM16	48	96	1/2	192	11	96	48	144
QAM16	60	120	1/2	240	13	120	60	180
QAM16	18	24	3/4	72	11	6	0	6
QAM16	36	48	3/4	144	17	74	72	2
QAM16	54	108	3/4	216	13	108	0	108
QAM64	18	36	1/2	72	11	6	0	6
QAM64	36	72	1/2	144	17	74	72	2
QAM64	54	108	1/2	216	13	108	0	108
QAM64	24	36	2/3	96	7	48	24	72
QAM64	48	72	2/3	192	11	96	48	144
QAM64	27	36	3/4	108	11	54	56	2
QAM64	54	72	3/4	216	13	108	0	108
QAM64	30	36	5/6	120	13	60	0	60
QAM64	60	72	5/6	240	13	120	60	180

Table hhh—Optimal CTC channel coding per modulation when supporting H-ARQ

Data block size (bytes)	N	P0	P1	P2	P3
6	24	5	0	0	0
12	48	13	24	0	24
18	72	11	6	0	6
24	96	7	48	24	72
36	144	17	74	72	2
48	192	11	96	48	144
60	240	13	120	60	180
120	480	13	240	120	360
240	960	13	480	240	720
360	1440	17	720	360	540
480	1920	17	960	480	1440
600	2400	17	1200	600	1800

In page 532, line 40, correct the text as shown below:

8.4.9.2.3.4 Subpacket generation

Proposed FEC structure punctures the mother codeword to generate subpacket with various coding rates. The subpacket is also used as H-ARQ packet transmission. Figure ~~bbb~~244 shows block diagram of subpacket generation. 1/3 CTC encoded codeword goes through interleaving block and the puncturing is performed. Figure 245 shows block diagram of the interleaving block. The puncturing is performed to select the consecutive interleaved bit sequence that starts at any point of whole codeword. For the first transmission, the subpacket is generated to select the consecutive interleaved bit sequence that starts from the first bit of the systematic part of the mother codeword. The length of the subpacket is chosen according to the needed coding rate reflecting the channel condition. The first subpacket can also be used as a codeword with the needed coding rate for a burst where H-ARQ is not applied.

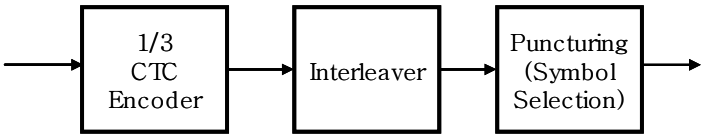

Figure 244— Block diagram of subpacket generation

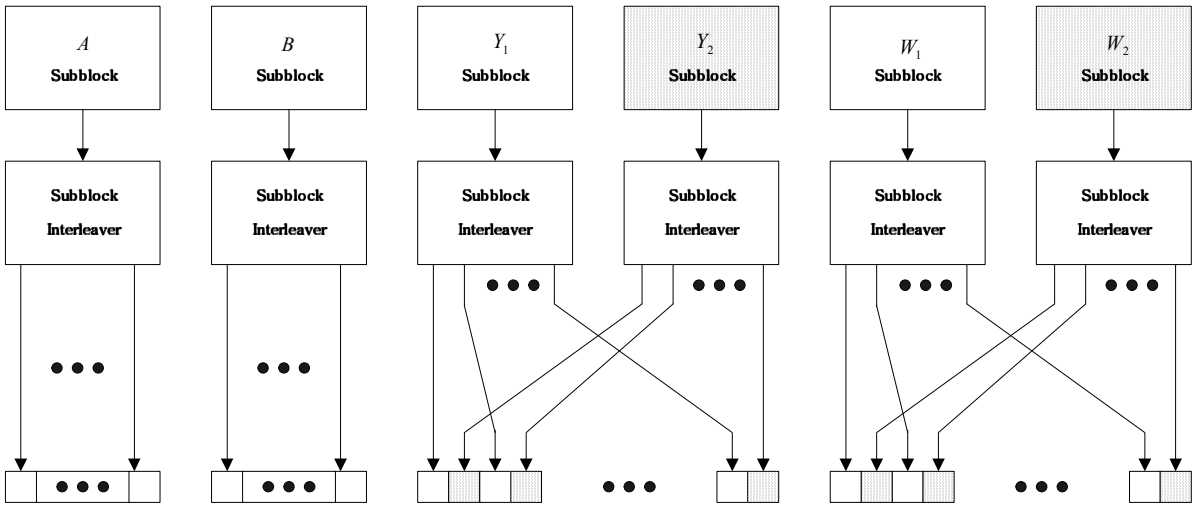

Figure 245— Block diagram of the interleaving scheme

8.4.9.2.3.4.1 Symbol Separation

All of the encoded symbols shall be demultiplexed into 6 subblocks denoted A, B, Y_1, Y_2, W_1 and W_2. The encoder output symbols shall be sequentially distributed into 6 subblocks with the first encoder output symbols going to the A subblock, the second encoder output going to the B subblock, the third to the Y_1 subblock, the fourth to the Y_2 subblock, the fifth to the W_1 subblock, the sixth to the W_2 subblock, etc.

8.4.9.2.3.4.2 Subblock Interleaving

The six subblocks shall be interleaved separately. The interleaving is performed by the unit of symbol. The sequence of interleaver output symbols for each subblock shall be generated by the procedure described below. The entire subblock of symbols to be interleaved is written into an array at addresses from 0 to the number of the symbols minus one (N-1), and the interleaved symbols are read out in a permuted order with the i-th symbol being read from an address, AD_i ($i = 0$ to $N-1$), as follows:

1. Determine the subblock interleaver parameters, m and J. Table ddd gives these parameters.

2. Initialize i and k to 0.

3. Form a tentative output address T_k according to the formula

$$T_k = 2^m (k \bmod J) + BRO_m(\lfloor k / J \rfloor)$$

where $BRO_m(y)$ indicates the bit-reversed m-bit value of y (i.e., BRO3(6) = 3).

4. If T_k is less than N, $AD_i = T_k$ and increment i and k by 1. Otherwise, discard T_k and increment k only.

5. Repeat steps 3 and 4 until all N interleaver output addresses are obtained.

The parameters for the subblock interleavers are specified in Table ddd.

Table ddd – The parameters for the subblock interleavers

Data block size (bits) N_{EP}	N	Subblock Interleaver Parameters	
		m	J
48	24	3	3
72	36	4	3
96	48	4	3
144	72	5	3
192	96	5	3
216	108	6	3
240	120	6	2
288	144	6	3
384	192	6	3
432	216	6	4
480	240	7	2

Table eee – The parameters for the subblock interleavers when supporting H-ARQ

Data block size (bits) N_{EP}	N	Subblock Interleaver Parameters	
		m	J
48	24	3	3
96	48	4	3