RPR MAC Delay Metric and SRP Phase One Simulation

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Agenda

- Delay performance criteria – quote from Harmen

- Delay apple to apple measurement

- RPR MAC performance reference model

- SRP simulation

- Summary

- Appendix

Delay Performance Criteria

- **"Queueing delay:** Time between the arrival of an end of packet at the MAC transmit buffer and the instant that this packet becomes the head-of-the-line packet in the transmit buffer. This delay is mainly caused by the node's own traffic."

- **"Medium access delay:** Time required for a head-of-the-line packet in the MAC transmit buffer to gain access to the medium. This delay is only caused by the medium competition and the fairness mechanism, not by the node's own traffic. This delay does not include the packet transmission time."

Delay Performance Criteria

- **"Receive buffer delay:** Time between the arrival of a begin-of-packet at the MAC receive buffer and the instant that this packet is completely delivered to the next protocol layer."

- **"Ring end-to-end delay:** Time required for a packet to travel from a source to a destination node on the same ring.
It consists of the packet transmission delay, all transit node delays, and the propagation delay from source to destination."

- **"MAC end-to-end delay:** Time between the arrival of an end of packet at the MAC transmit buffer of the source node and the time that this packet is completely delivered to the next protocol layer of the destination node on the same ring."
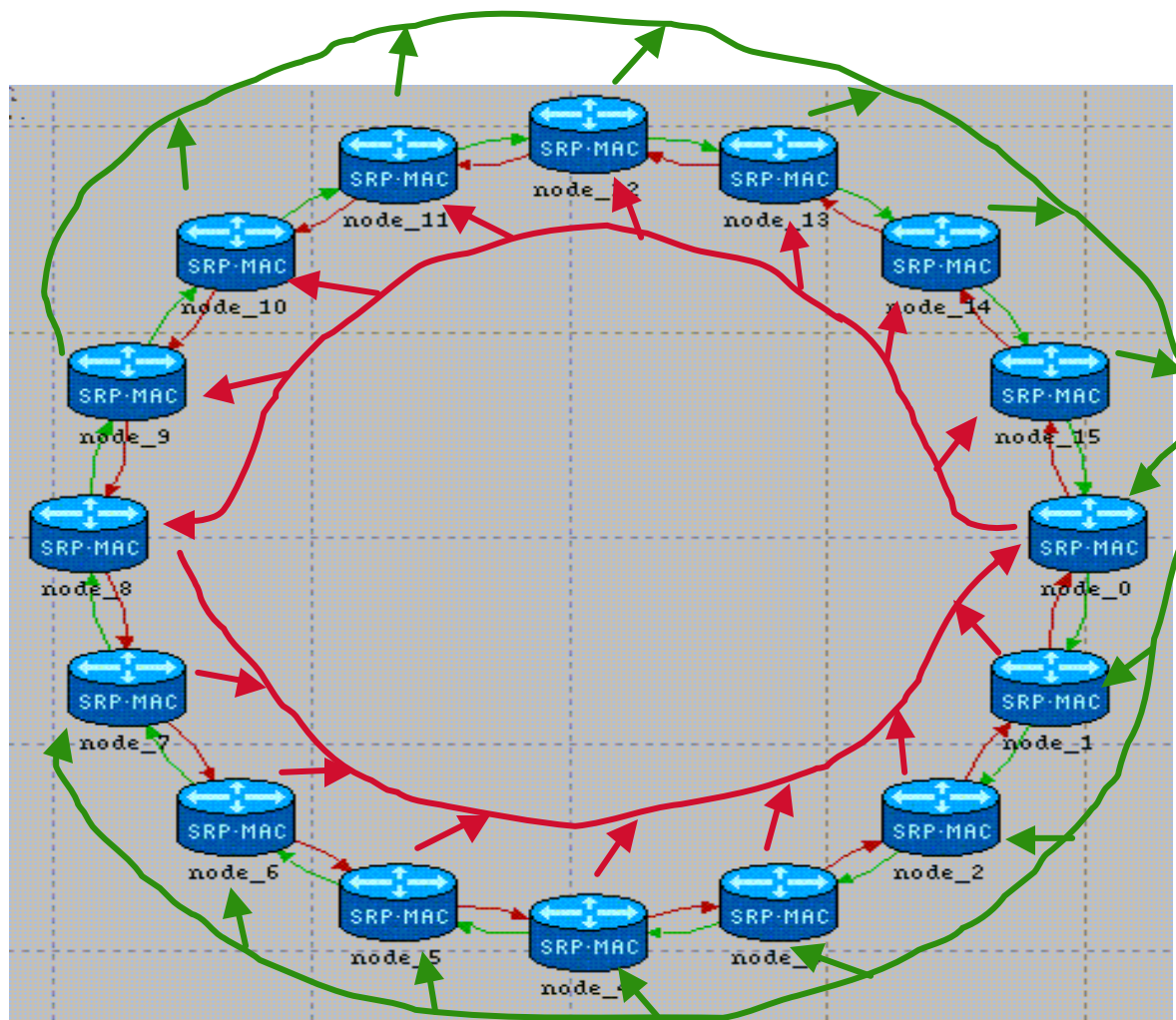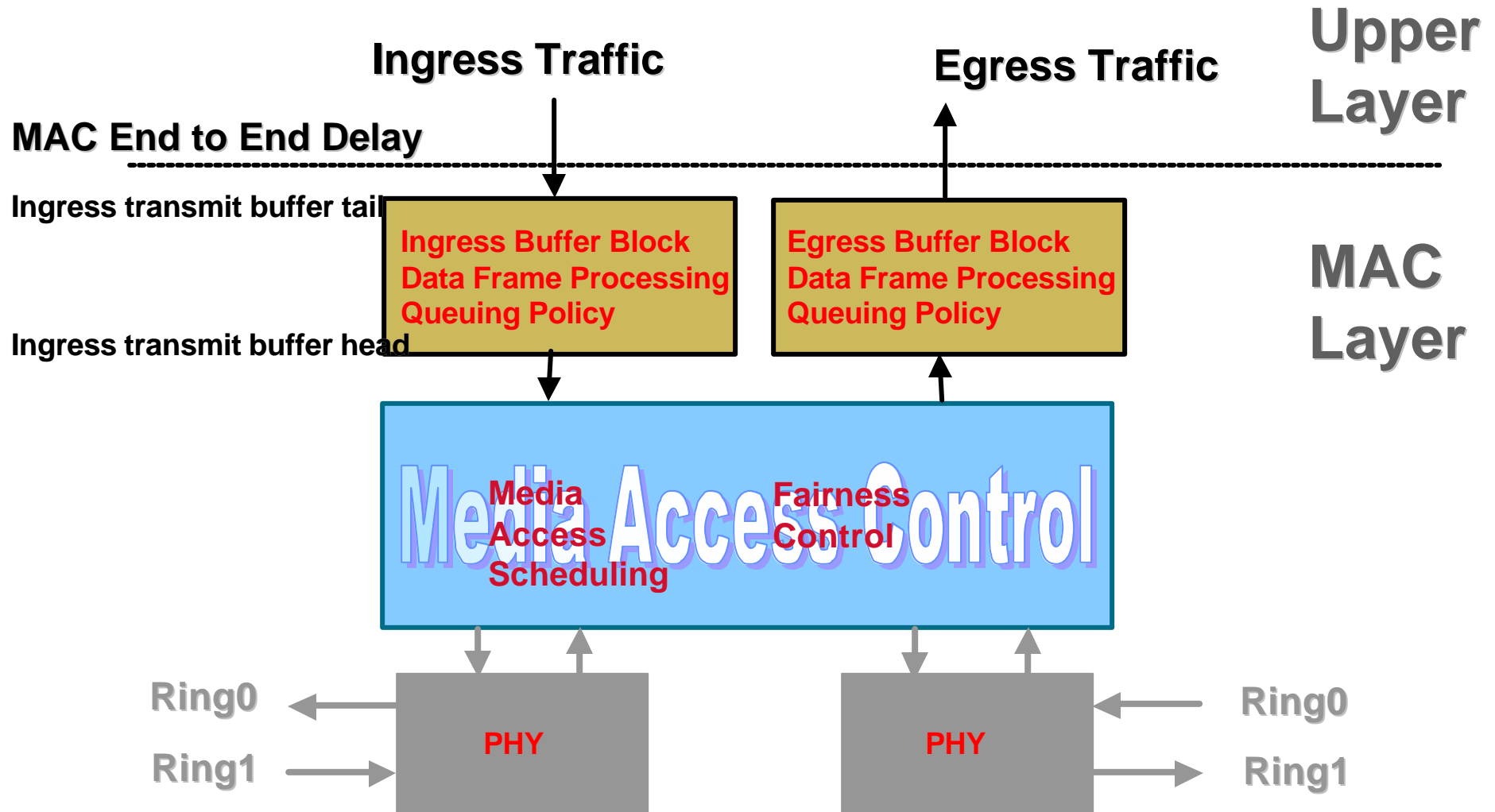
Apple to Apple for Delay Measurement

- All delays matter in MAC performance

- Eliminate ambiguous measuring points

- MAC end-to-end delay has it all

  - Ingress queuing delay and egress receive buffer delay:

    Same ingress and egress buffer size

    Same ingress queuing policy

    Same egress queuing policy

    Same RPR packet header size

  - Media access delay

    Same delay measurement point for HOL packet in ingress buffer

  - Ring end-to-end delay

    Same propagation delay

- Factor out upper layer processor or switching fabric delay impact

  - Assume sufficient higher upper layer processing rate than ring bandwidth
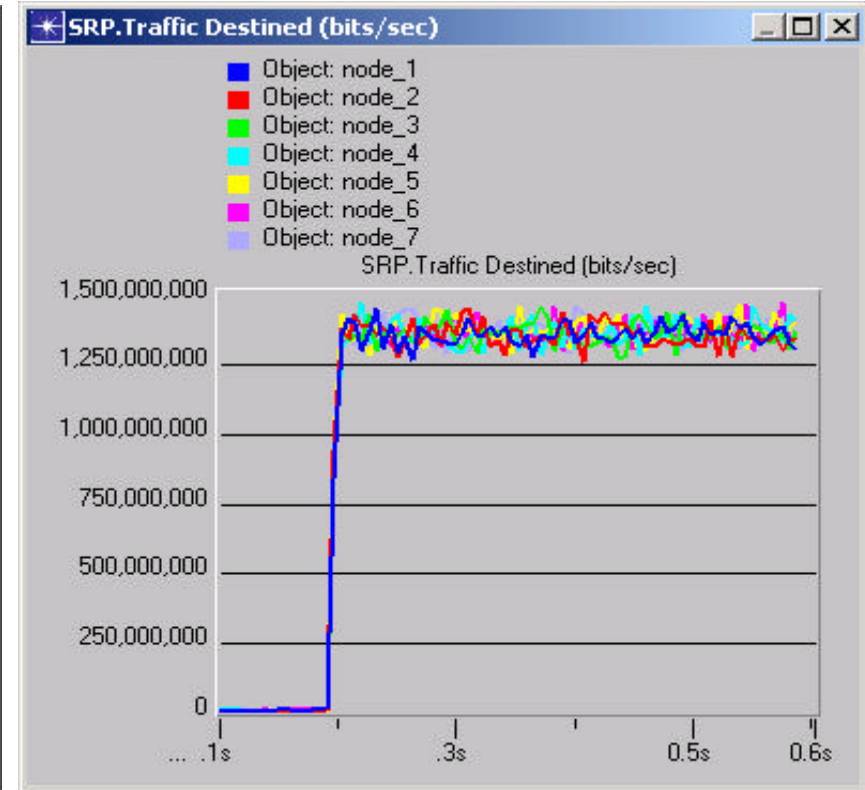
RPR MAC Performance Reference Model

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Upper Layer

Ingress Traffic

Egress Traffic

MAC End to End Delay

Ingress transmit buffer tail

Ingress Buffer Block Data Frame Processing Queuing Policy	Egress Buffer Block Data Frame Processing Queuing Policy

Ingress transmit buffer head

MAC Layer

Media Access Control

Media Access Scheduling

Fairness Control

Ring0

Ring1

PHY

PHY

Ring0

Ring1

SRP Simulation
Hub Aggregation

Simulation Configuration

- Traffic Profile
    - Access traffic goes to Hub node in the shortest path
    - Access traffic rate: 150% ~ 200% x 10Gbps / 7, exponential
    - Hub node distributes traffic randomly to access nodes
    - Hub distribution traffic rate: 110% x 20Gbps, exponential
    - Packet size: 60% 64 bytes, 20% 512 bytes and 20% 1518 bytes

- SRP Configuration
    - Low priority transmit buffer: 256KB
    - Low priority transit buffer: 1MB
    - Low threshold: 8K ~ 32K
    - Decay interval: 128KB time

100Km Ring
Access and Distribution Traffic Throughput
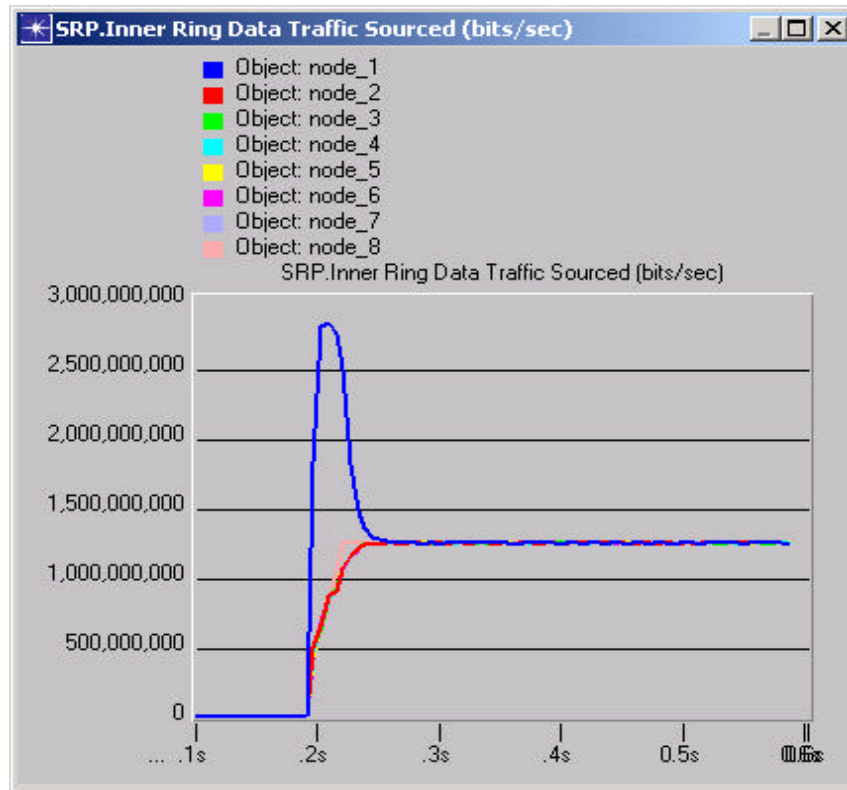
• Fair access rate for all nodes
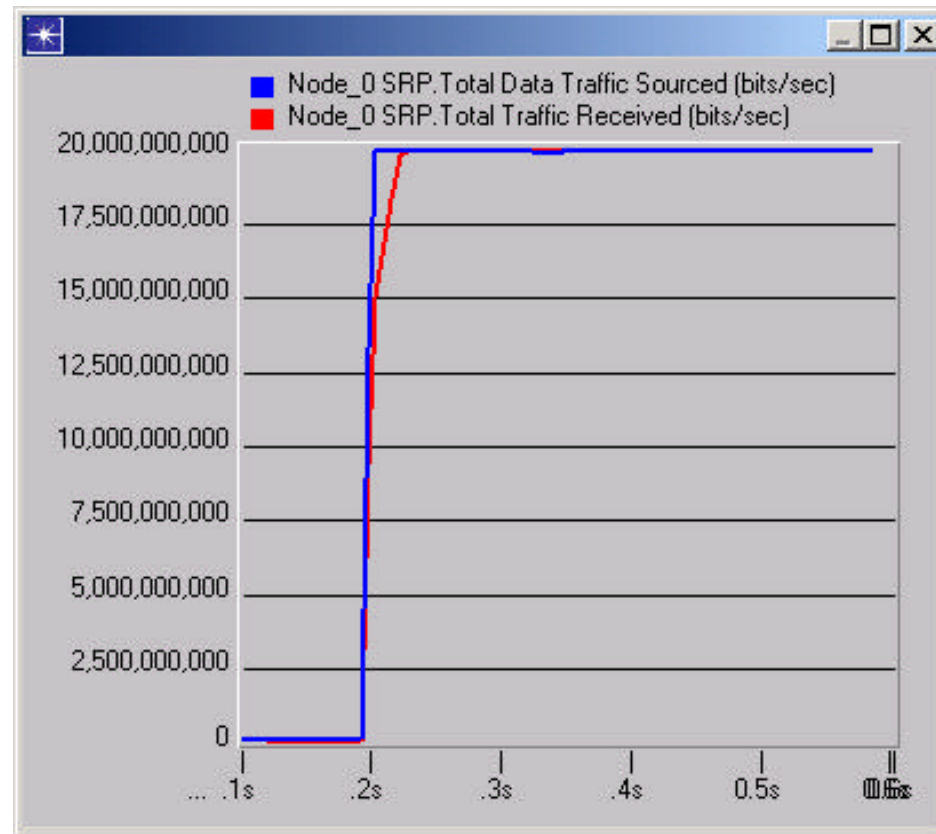
100Km Ring
MAC End-to-End Delay and Jitter

- MAC end2end delay =
  transmit queue delay + media access delay + ring end2end delay + receiver queue delay
- Consistent and fair delay and jitter performance for all nodes
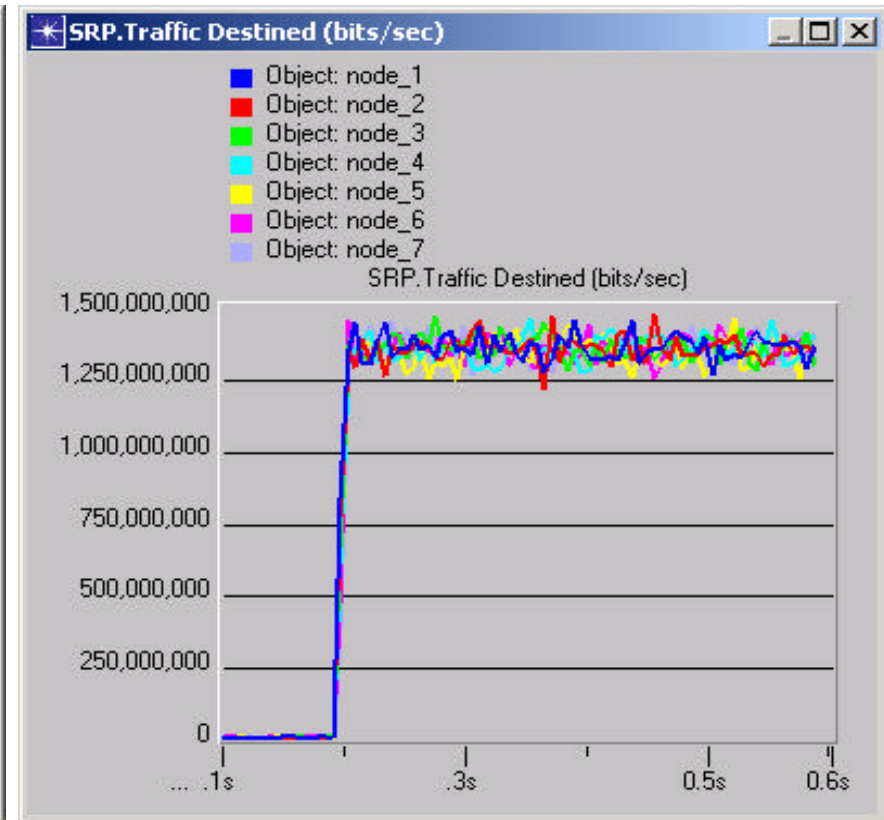
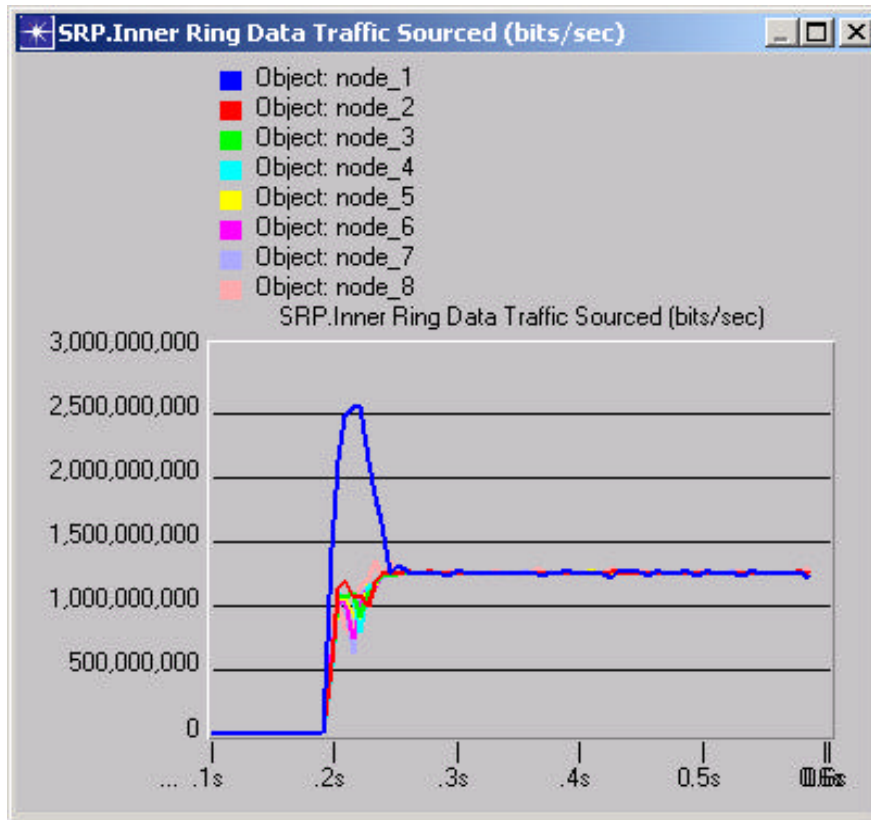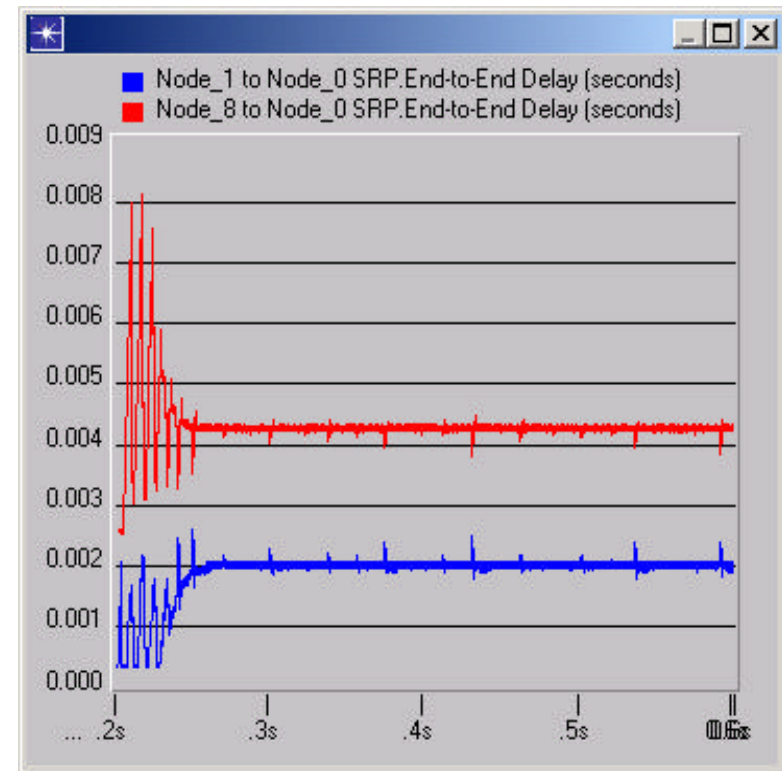# 100Km Ring
Full BW Utilization

• Full linerate transmission on both inner ring and outer ring

1000Km Ring
Access and Distribution Traffic Throughput
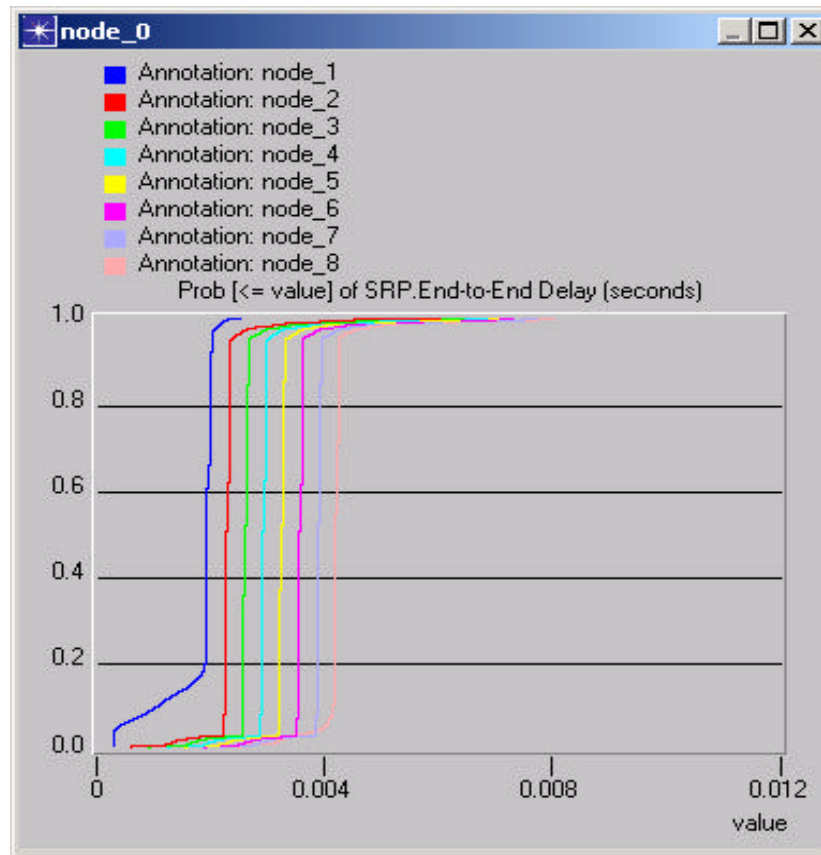
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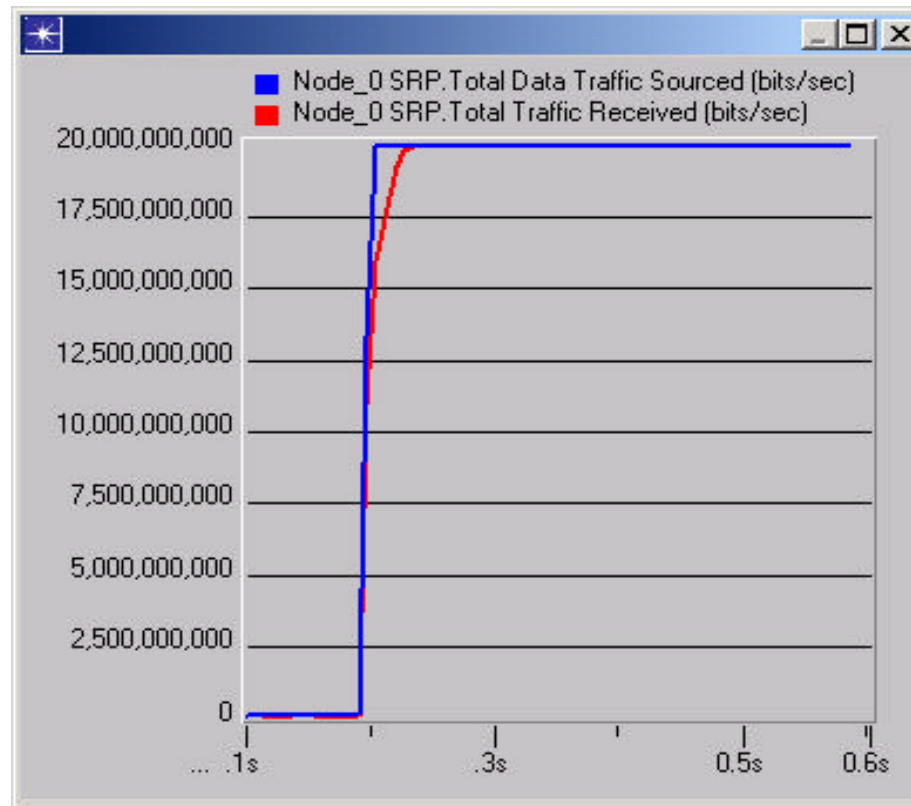
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1000Km Ring
Full BW Utilization

• Full linerate transmission on both inner ring and outer ring

Summary

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- Use MAC end-to-end delay as RPR delay performance metric
- Identify where and how the delay is measured in your RPR MAC architecture

- SRP provides

  - excellent fairness for all access notes
  - full bandwidth utilization
  - fair and bounded end-to-end delay and jitter for all
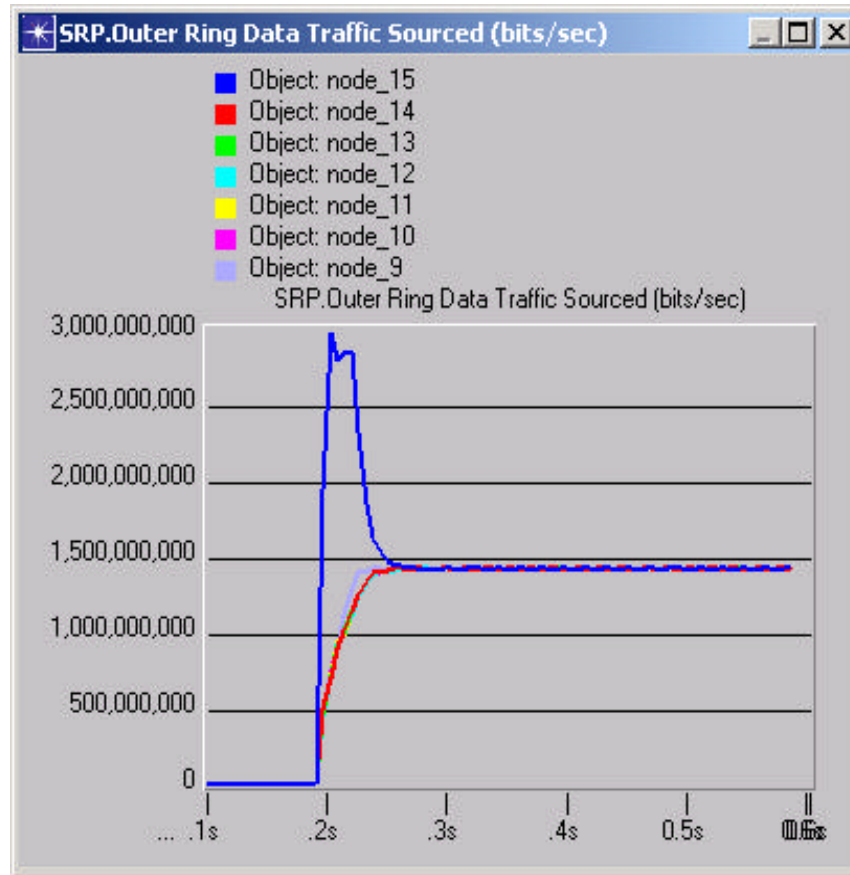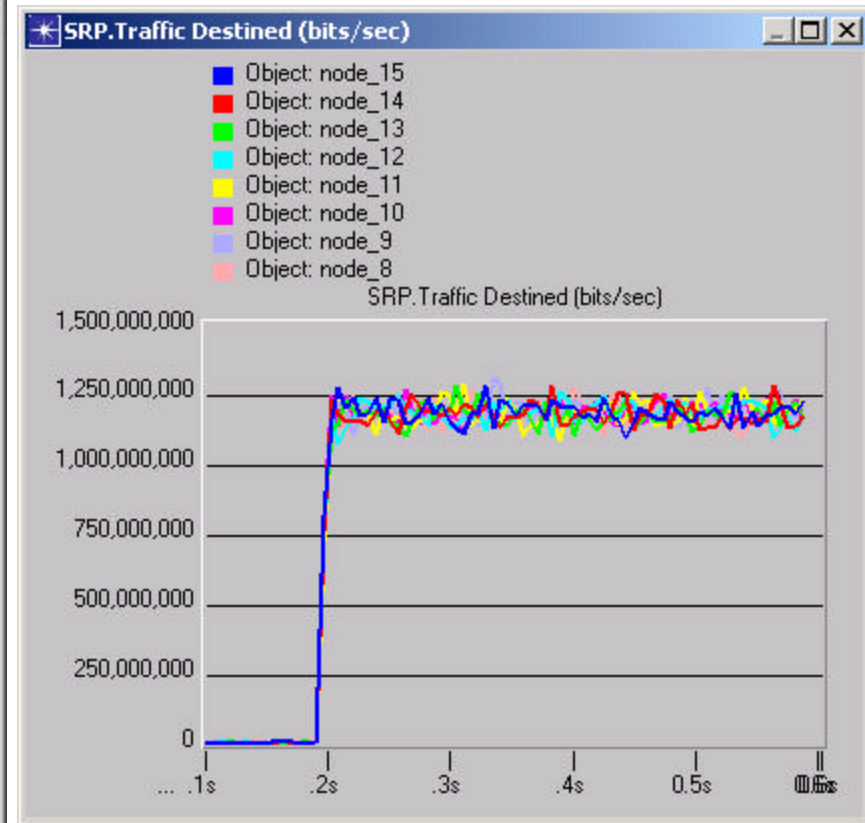 - excellent scalability for different ring sizes

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Appendix

- 100Km Ring
    - Fair access and distribution rate

- 1000Km Ring
    - Fair access and distribution rate

100Km Ring
Fair Access and Distribution Rate

1000Km Ring
Fair Access and Distribution Rate