



PROPOSED OBJECTIVE LANGUAGE/FORMS

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CISCO SYSTEMS



FOUNDATIONAL OBJECTIVES

- Support a MAC data rates of 100, 200, and 400 Gb/s
- Support full-duplex operation only
- Preserve the Ethernet frame format utilizing the Ethernet MAC
- Preserve minimum and maximum Frame Size of current IEEE 802.3 standard
- Support a BER of better than or equal to 10^{-12} at the MAC/PLS service interface (or the frame loss ratio equivalent) for single-lane 100Gb/s operation
- Support a BER of better than or equal to 10^{-13} at the MAC/PLS service interface (or the frame loss ratio equivalent) for two-lane 200Gb/s or four-lane 400Gb/s operation
- Support optional Energy-Efficient Ethernet operation

PROPOSED PHY AND INTERFACE OBJECTIVES

- Define a single-lane 100 Gb/s Attachment User interface (AUI) for chip-to module applications, compatible with existing PMDs based on 100 Gb/s per lane optical signaling
- Define a single-lane 100 Gb/s Attachment User interface (AUI) for chip-to-chip Applications
- Define a single-lane 100Gb/s PHY for operation over electrical backplanes supporting a ball-to-ball insertion loss \leq "z" dB at "y"GHz.
- Define a single-lane 100Gb/s PHY for operation over twin-axial copper cable with lengths up to at least "w"m.

PROPOSED PHY AND INTERFACE OBJECTIVES

- Define a two-lane 200 Gb/s Attachment User interface (AUI) for chip-to module applications, compatible with existing PMDs based on 100 Gb/s per lane optical signaling
- Define a two-lane 200 Gb/s Attachment User interface (AUI) for chip-to-chip Applications
- Define a two-lane 200Gb/s PHY for operation over electrical backplanes supporting a ball-to-ball insertion loss \leq "z" dB at "y"GHz.
- Define a two-lane 200Gb/s PHY for operation over twin-axial copper cable with lengths up to at least "w"m.

PROPOSED PHY AND INTERFACE OBJECTIVES

- Define a four-lane 400 Gb/s Attachment User interface (AUI) for chip-to module applications, compatible with existing PMDs based on 100 Gb/s per lane optical signaling
- Define a four-lane 400 Gb/s Attachment User interface (AUI) for chip-to-chip Applications
- Define a four-lane 400Gb/s PHY for operation over electrical backplanes supporting a ball-to-ball insertion loss \leq "z" dB at "y"GHz.
- Define a four-lane 400Gb/s PHY for operation over twin-axial copper cable with lengths up to at least "w"m.