100Gbps/Lane Electrical Signaling

A New Approach

Ramin Farjadrad, SVP of R&D

Industry Target Channels

Application	Standard	Modulation	Reach	Loss Ball-ball
Chip-to-OE (MCM)	OIF-56G-USR	NRZ	< 1cm	2 dB@28 GHz
Chip-to-nearby OE (no connector)	OIF-56G-XSR	NRZ/ PAM4	<7.5 cm[1]	8 dB@28 GHz 4.2 dB@14 GHz
Chip-to-module (one connector)	OIF-56G-VSR IEEE CDAUI-8	NRZ/PAM4 PAM4	< 10 cm[2] <20 cm	18 dB@28 GHz 10 dB@13.3 GHz
Chip-to-chip (one connector)	OIF-56G-MR IEEE CDAUI-8	NRZ/PAM4 PAM4	< 50 cm < 50 cm	35.8 dB@28 GHz 20 dB@13.3 GHz
Backplane (two connectors)	OIF-56-LR IEEE 200G-KR4	PAM4 PAM4	<100 cm <100 cm	30dB@14.5 GHz 30dB@13.3 GHz

- PAM4 enabled 50Gbps transmission over LR channels with IL=30dB@14GHz
- Will higher level PAMs enable 100Gbps transmission over similar channels?
- Should industry limit 100Gbps/lane to channels with IL<30dB@28GHz?

Modulation Considerations for 100Gbps/Lane

- Higher PAM levels use less transmission bandwidth, thus operating in the better portion of the channel
  - →Lower Insertion Loss (IL)
  - →Higher Return Loss (RL)
  - →Less Channel Xtalk, Noise, etc
- Higher PAM levels also lead to less distance between levels (less SNR) and also more PHY complexity
- This presentation evaluates the tradeoffs among PAM options and introduces a new approach to the 100Gbps/Lane challenge

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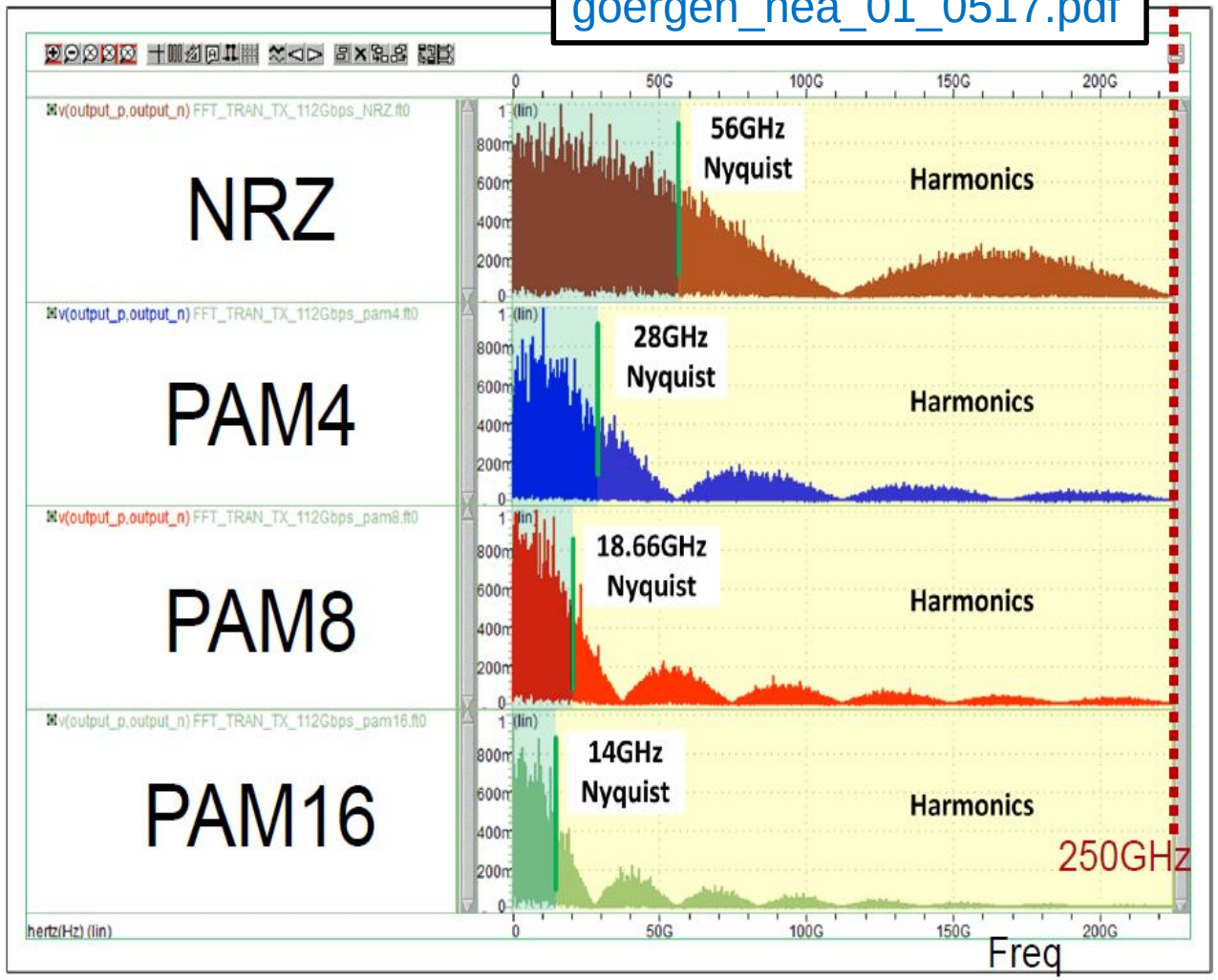
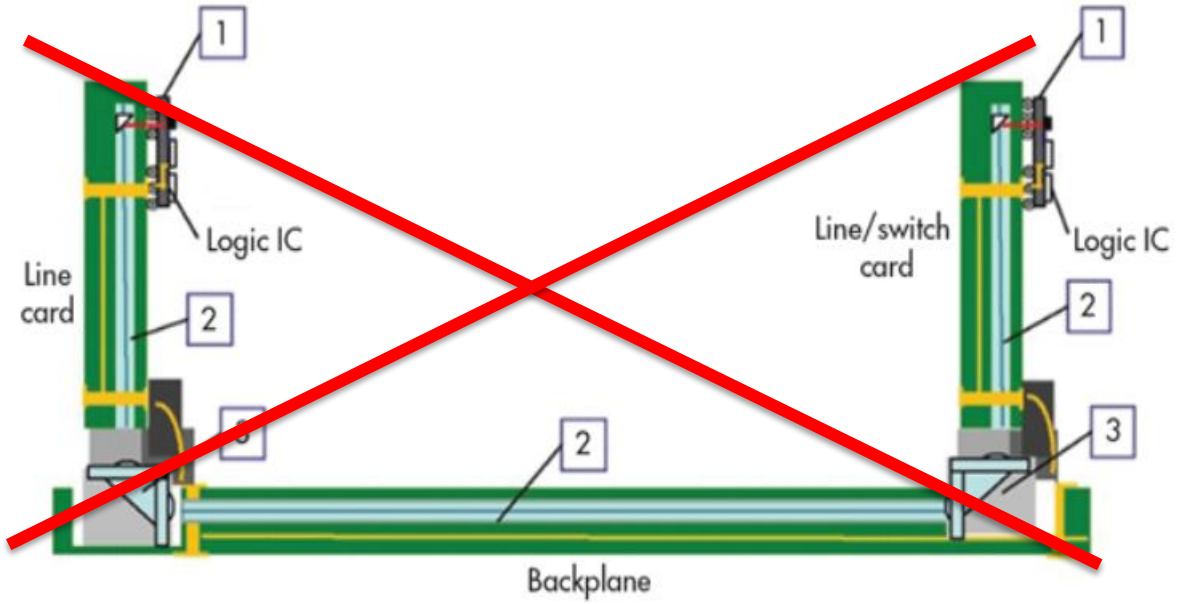


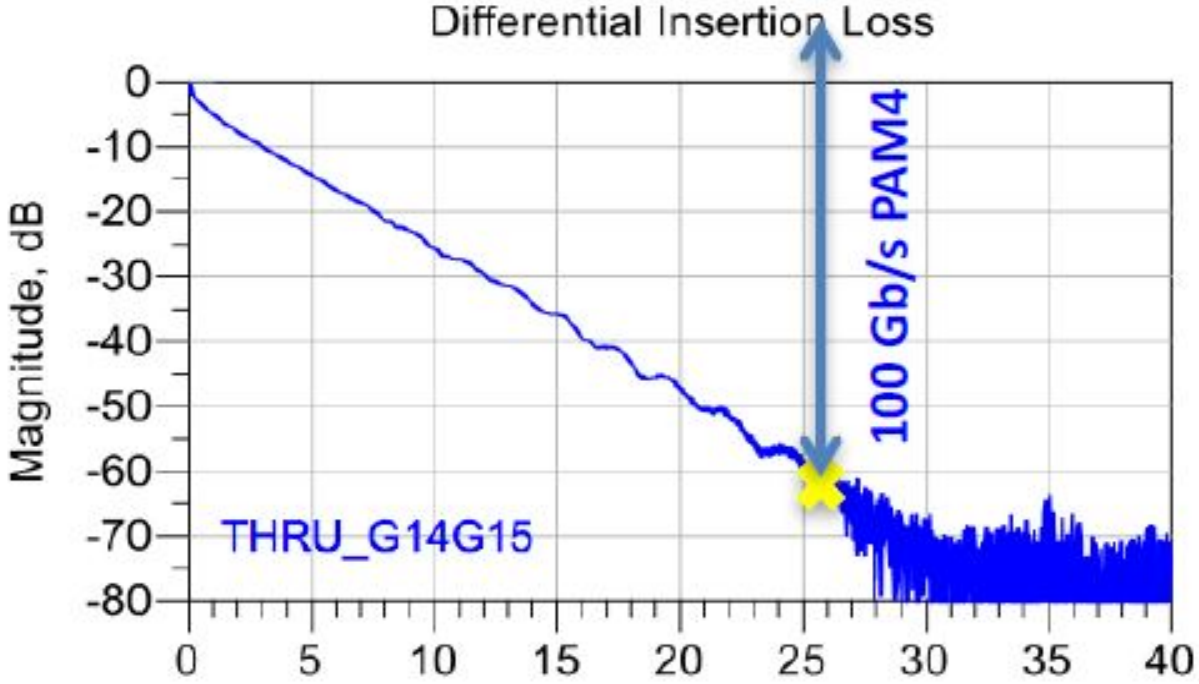
100Gbps/Lane PAM4

- Double the 53Gbps PAM4 baud rate → 53Gbaud
  - Signaling BW (Nyquist) = 26.5GHz

- Challenges of transmission over 100cm Backplane or 3-5m Cable
  → New super high quality PCB materials/thicker cables
    - PCB: FR408HR/Nelco4K → Megtron7/Rogers/Tachyon100 (3x-4x Cost)
    - Cables: Passive → Active or 30AWG → 24AWG (2x Thicker)
  → Connectors with BW > 28GHz → Super High Cost & Sensitive
  → Signaling integrity challenges
    - Limits the PCB routing options
    - Alternative backplane configs such flyover cables

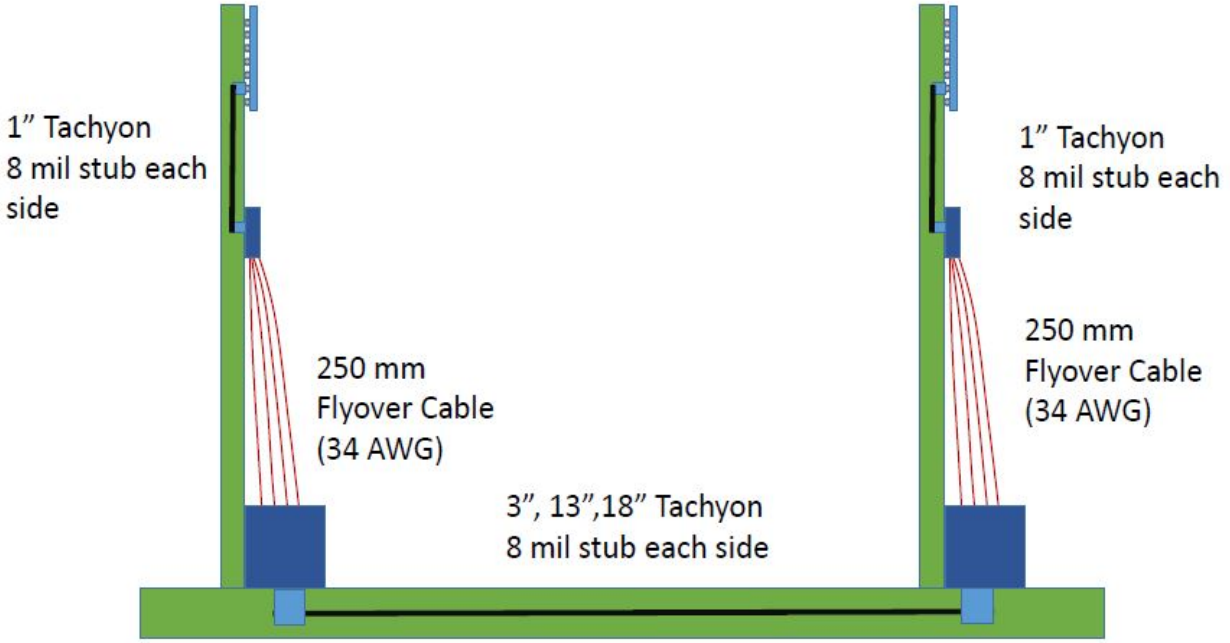
100Gbps/Lane PAM4: Standard 2-Connector Backplane

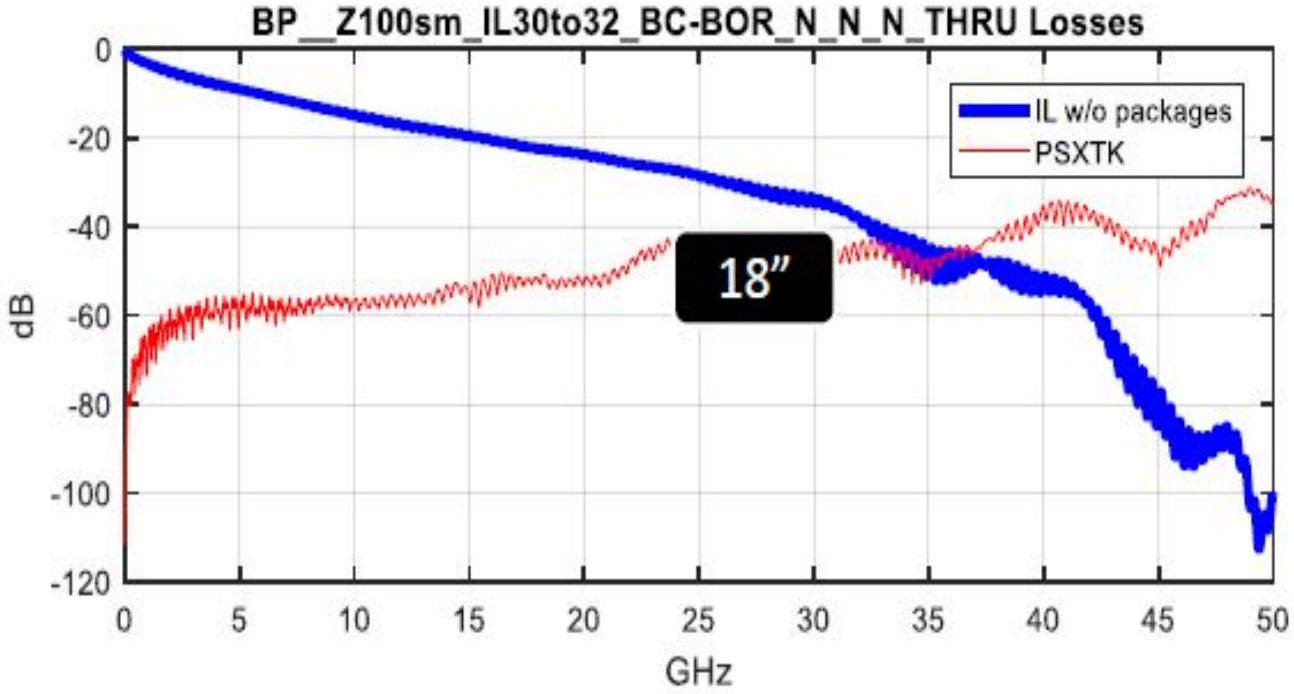




- Conventional two connector PCB backplanes demonstrate significant loss even with high quality dielectric materials (ghiasi_nea_01a_0517)
  - 40” Backplane with Megtron6 → IL>60dB@26.5GHz
  - Expensive Connectors with BW >28GHz
  - No practical PHY can equalize IL=60dB for BER<1E-12

100Gbps/Lane PAM4: Flyover Backplane

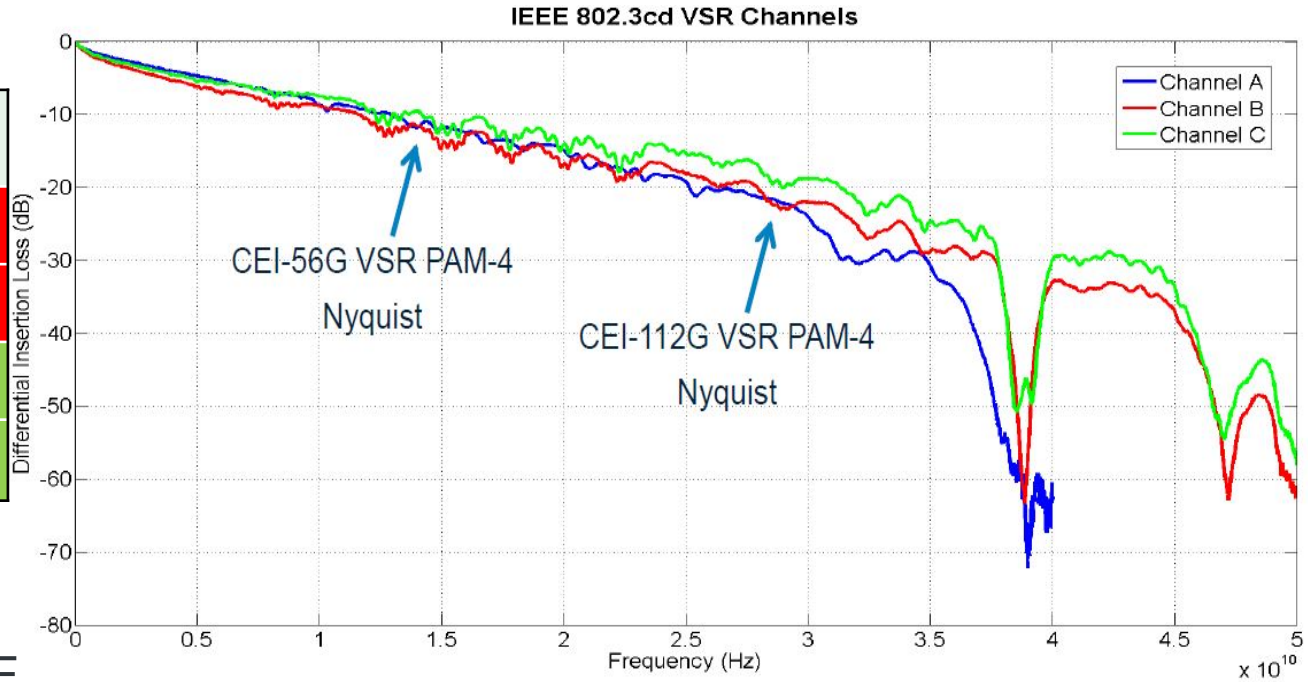




- Flyover backplane provides less lossy backplane solution by replacing part of the route with cables (mellitz_100GEL_adhoc_01_010318)
  - Less loss in exchange for extra cost/complexity
  - 20” Cables + 18” Tachyon Backplane → IL=~30dB@26.5GHz
  - Expensive Connectors with BW >28GHz

100Gbps/Lane PAM4: PHY Complexity & Power

SNR Margin (BER<1E-5)	Channel A	Channel B	Channel C
Taps: 8 FFE + 1 DFE	1.2	-1.3	-0.7
Taps: 16 FFE + 1 DFE	2.3	-0.4	-0.1
Taps: 32 FFE + 1 DFE	3.6	2.2	2.7
Taps: 64 FFE + 1 DFE	4.8	2.9	3.3



- PHY Equalizer for 50G PAM4
  - IL=30dB@14GHz → 16-Tap FFE + 1-Tap DFE
- Complex Equalization for 100G PAM4:
  - VSR Channel IL=~22dB@28GHz → Minimum 32-Tap FFE (palkert_nea_02_0517)
    - More power/complex than 64-Tap FFE @14GBaud ← Higher parallelism leads to inefficiency
  - 1-Tap DFE using loop-unrolled parallel design >2x higher power
    - 2-Tap (or more) DFE get exponentially high in complexity & power

PAM8 or PAM16 for 100Gbps/Lane?

- PAM8: 1.5x the 53Gbps PAM4 baud rate → 35.3Gbaud
  - Advantage:
    - Signaling BW (Nyquist) = 17.8GHz (33% less than 106Gbps PAM4)
  - Disadvantages:
    - Require 9.1dB higher input SNR than PAM4 for same BER with 3x FEC interleaving (sun_nea_01a_0517)
  - PAM8: BER=1E-15 (Post FEC)→ Input SNR=27.9dB & 3x-Interleaved KP4 FEC

- PAM16: Same baud rate as 53Gbps PAM4 → 26.5Gbaud
  - Advantage:
    - Signaling BW (Nyquist) = 13.25GHz (50% less than 106Gbps PAM4)
  - Disadvantages:
    - Requires 16dB higher input SNR than PAM4 for same BER h 8x FEC interleaving
  - PAM16: BER=1E-15 (Post FEC)→ Input SNR=34.8dB & 8x-Interleaved KP4 FEC

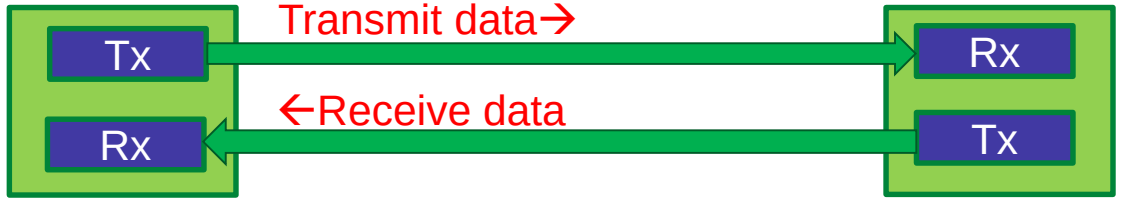
100Gbps PAM-N Modulations Performance Comparison

- Sample 40” Backplane with 2 Line Card Connections
- Analysis assumes same PHY SNR performance across any baud rate
  - In reality to achieve same SNR performance, PHY power increases by 2x-4x depending on the process technology PHY is implemented in

Modulation	53Gbps PAM4	106Gbps PAM4	106Gbps PAM8	106Gbps PAM16
Baud rate (6% FEC Overhead) [GBaud]	26.5	53	35.3	26.6
Nyquist BW [GHz]	13.25	26.5	17.67	13.25
IL @Nyquist [dB]	-32	-61.1	-42.3	-32
Tx Output Power for 1Vpkpk [dBm]	1.43	1.43	0.34	-0.15
Salz SNR (Ideal PHY AFE)	34.25	21.35	28.48	32.67
Salz SNR (6.5ENOB AFE)	28.25	19.1	24.68	27.6
SNR DFE Taps [32 FF , 1 FB] High Tap Resolution	25.11	6.63	14.42	24.53
SNR DFE Taps [32 FF , 1FB] 10bit Tap Resolution	24.18	6.38	13.73	23.6
Required Input SNR for BER=1E-15 (Post FEC)	18.8 (1x FEC)	18.8 (1x FEC)	27.9 (3x FEC)	34.8 (8x FEC)
SNR margin (Slatz)	15.45	2.55	0.58	-2.13
SNR margin with Practical PHY (PHY Performance same at any baud)	5.38	-12.42	-14.17	-11.2

Dual Duplex Definition

Single Duplex (SD):



Dual Duplex (DD):

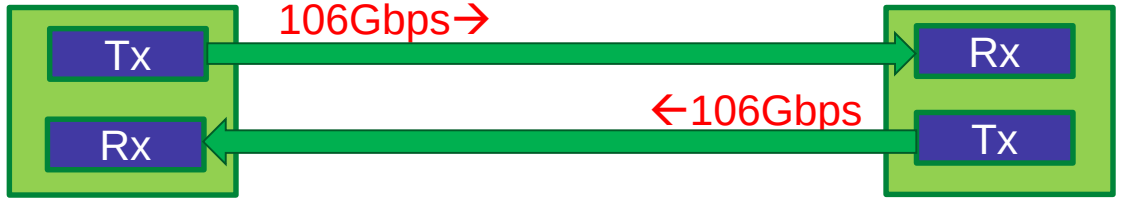
- Transmit and receive data on each pair
- In Dual Duplex data rate on each pair is half of the data rate of Single Duplex

→ Insertion Loss in Dual Duplex mode is much lower

SD – Single Duplex (Tx on one pair, Rx on one pair)
DD – Dual Duplex (Tx and Rx on both pairs)

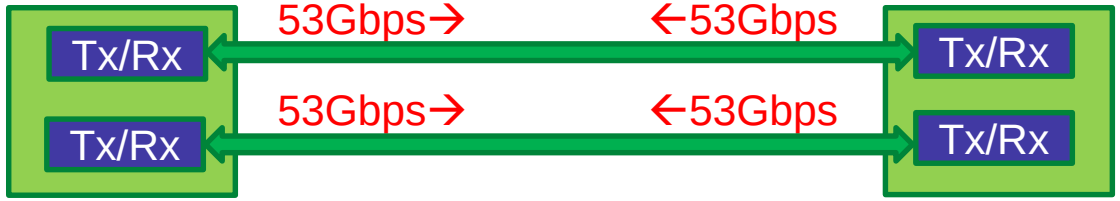
100G Dual Duplex Technology

Standard 100G Electrical:



Baud rate: 53Gbaud (f_N=26.5GHz)

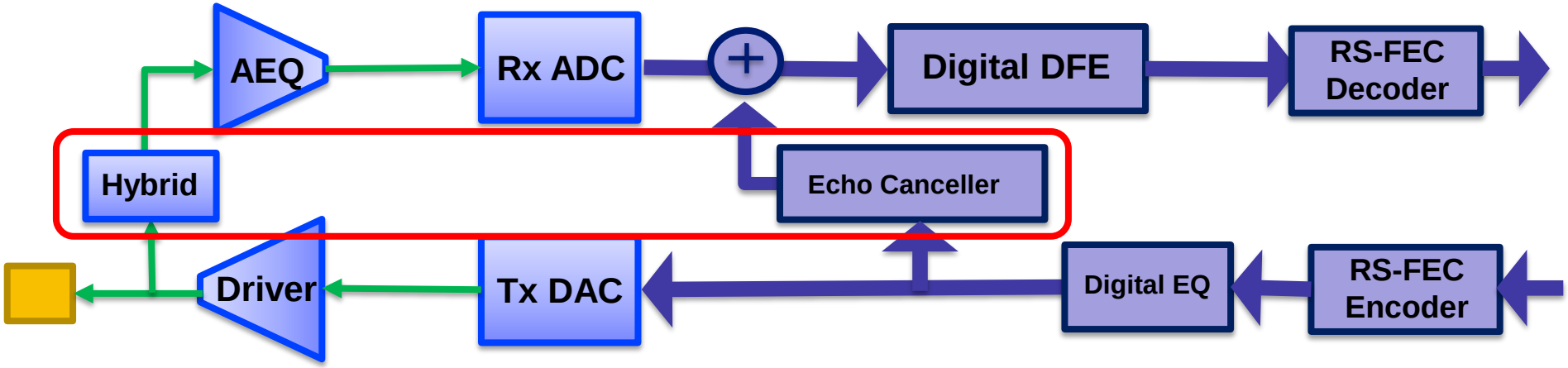
Aquantia 100G Electrical:
Dual Duplex PAM4 Signaling



Baud rate: 26.5Gbaud (f_N=13.25GHz)

- Using the standard Tx and Rx channels to transmit and receive on each one.
  - Signal rate is half of standard rate, results in a much lower Insertion Loss
  - Echo cancelation technology is required to remove ~40dB echo power
  - Echo cancellation at Multi-Gbaud is a known art (implemented in 10GBASE-T etc)

Dual Duplex Architecture



- A dual duplex architecture is realized by including Echo cancellation to a conventional Transceiver
  - Echo cancellation of ~40dB at 13.25GBaud is required for 100Gbps/PAM4
  - Echo canceller complexity may be significantly reduced if ~3dB SNR degradation is tolerable
- Everything else stays same as in 802.3cd 100GBASE-KR2
  - Same Equalizer (FFE/DFE), PCS and FEC RS(544,514,10)

100Gbps Dual Duplex & Single Duplex Performance Comparison

- Sample 40” Backplane with 2 Line Card Connections
- Dual Duplex PAM4 can double the data rate of a standard PAM4 over a similar channel with up to 5dB@13.25GHz reach (~3dB SNR) penalty
  - This penalty can be reduced by higher complexity Echo Canceller
- A 2-bit 64-Tap 13.25Gbaud Echo Canceller burns ~1/8 power of an 8-bit 64-Tap 26.5Gbaud FFE (used in 106Gbps SD-PAM4)

Modulation	53Gbps SD-PAM4	106Gbps SD-PAM4	106Gbps SD-PAM8	106Gbps SD-PAM16	106Gbps DD-PAM4
Baud rate (6% FEC Overhead) [GBaud]	26.5	53	35.3	26.6	26.5
Nyquist BW [GHz]	13.25	26.5	17.67	13.25	13.25
IL @Nyquist [dB]	-32	-61.1	-42.3	-32	-32
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SNR margin (Slatz)	15.45	2.55	0.58	-2.13	15.45
SNR margin with Practical PHY (PHY Performance same at any baud)	5.38	-12.42	-14.17	-11.2	2.25

100Gbps/Lane PAM4: Dual Duplex vs. Single Duplex Channels

Interface	Architecture	IL @26.5GHz Ball to Ball	IL @26.5GHz Bump to Bump	100Gbps PAM4 SD	100Gbps PAM4 DD
Chip to Module	Conventional 10” PCB + Module	**20dB**[1] (10@13.3GHz)	**28dB** (14@13.3GHz)	Practical	Practical
	Internally Cabled Host + Module	**15dB**[1] (10@13.3GHz)	**23dB** (14@13.3GHz)	Practical	Practical
Chip to Chip	Conventional PCB + Mezz Connector	**40dB**[1] (20@13.5GHz)	**48dB** (28@13.5GHz)	Impractical	Practical
	Internally Cabled Host + Mezz Connector	**20-30dB**[1] (15-20@13GHz)	**28-38dB** (19-24@13GHz)	Limited	Practical
Backplane	1m Conventional PCB	**60dB**[1] (30@13.3GHz)	**68dB** (34@13.3GHz)	Impractical	Practical
	Cabled Backplane	**20-35dB**[2] (10-18@13GHz)	**28-43dB** (14-22@13GHz)	Very Limited	Practical
Copper Cable	Conventional 3m 30AWG DAC + Host PCB	**46dB** (30@13.3GHz)	**54dB** (34@13.3GHz)	Impractical	Practical
	Internally Cabled Host + DAC	**20-30dB**[1] (15-20@13GHz)	**28-38dB** (19-24@13GHz)	Limited	Practical

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Conclusion

- Despite 9.5dB SNR penalty, PAM4 replacement of NRZ delivered twice the throughput of 25Gbps/lane NRZ over similar legacy electrical channels to achieve 50Gbps/lane

- At 100Gbps/lane, Single-Duplex signaling schemes are limited to short reach electrical links (SR)
  - This is also true for higher level PAMs (PAM8 & PAM16) with lower baud rates

- Dual Duplex PAM4 signaling by exploiting the electrical channel capacity in both directions, delivers
  - 100Gbps transmission over almost similar electrical channels as in 802.3cd (50Gbps PAM4)
    - SNR penalty of ~3dB can be further reduced by increasing the echo cancellation complexity
  - Less complex equalization & Lower power PHY compared to 100Gbps SD-PAM4
  - Fully compatible with PCS and FEC of 802.3cd 100GBASE-KR2

Supportive of Proposed PAR & CSD

- Supports proposed PAR/CSD for operation over

  Proven and Familiar Media using Known or Developing Technology

- Economic Feasibility
  - Known cost factors in media and connectors – Similar to 50Gbps/lane
  - Known installation costs – Similar to 50Gbps/lane
  - Consideration of operational costs - Expected lower power than other techniques

- Broad market potential (lusted_100GEL_01a_118.pdf)
  - Copper cable and cost-effective backplane remain essential for Server access
  - ToR DAC server access and backplane represents the largest single part of the market potential today (CFI presentation, palkert_100GEL_02_0118.pdf, primary data in: http://www.ieee802.org/3/400GSG/public/13_11/booth_400_01a_1113.pdf

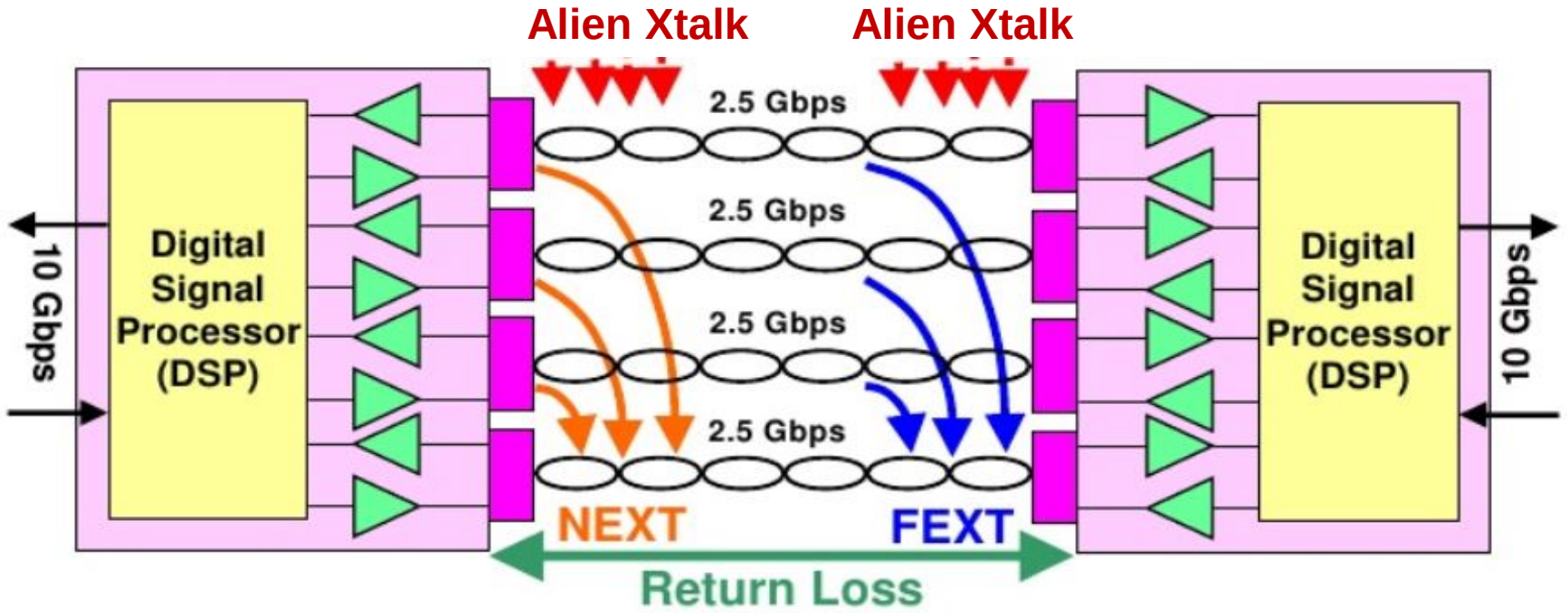
Supports Lusted_100GEL_01a_118.pdf Tech Feasibility

- The proposed project will build on the array of Ethernet component and system design experience, and the broad knowledge base of Ethernet network operation.
  - Component vendors have presented data on the feasibility of the necessary components for 100 Gb/s electrical signaling. Proposals, which either leverage existing technologies or employ new technologies, have been provided.
  - Component technology using 100 Gb/s electrical signaling rates is either under development for other projects (e.g. OIF) or has been demonstrated.

- Leverages existing technologies and component technology:
  - Media/Packaging – same as or similar to 50Gbps/lane
  - SI Design/layout practices – same as or similar to 50Gbps/lane
  - Equalization and Timing Recovery – same as 50Gbps/lane
- New techniques extended from existing & in development for other projects:
  - Echo cancellation builds on extensive experience at lower speeds but higher performance
  - Multi-Gbaud Echo cancellation already in development for other proprietary projects
- Modest media improvements provides room to de-risk new techniques

Thank you.

Dual Duplex Architecture: A Known Art



- Modulation: DSQ128 → 10.5dB less SNR margin than PAM4
- 2.5Gbps/pair in both directions over 100m UTP → Exposed to Alien Xtalk/Noise
- Insertion Loss (100m CAT6A)=~45dB@Nyquist → ~15dB higher IL
- 10GBASE-T PHY needs to perform >60dB Echo & >40dB Xtalk Cancellation

  → More Complex Dual Duplex PHYs already implemented to address limited channel capacity

100Gbps/Lane PAM8

- 1.5x the 53Gbps PAM4 baud rate → 35.3Gbaud
- Advantage:
  - Signaling BW (Nyquist) = 17.8GHz (33% less than 106Gbps PAM4)
- Disadvantages:
  - Requires 7.4dB higher input SNR to PAM4 for same BER
    - PAM4: Input SNR=18.8dB→ BER=1E-15 (Post KP4 FEC)
  - High Probability of Error Propagation in DFE :
    - PAM4 (Non-Interleaved KP4 FEC) → Uncorrectable Error Probability=(3/4)^74= 5.7E-10
    - PAM8 (Non-Interleaved KP4 FEC) → Uncorrectable Error Probability=(7/8)^50= 1.26E-3
    - PAM8 (3x-Interleaved KP4 FEC) → Uncorrectable Error Probability=(7/8)^150= 2.0E-9

      →Requires extra 1.7dB margin, **total ~9.1dB**, to PAM4 SNR to deliver same BER (sun_nea_01a_0517)

- PAM8: BER=1E-15 (Post FEC)→ Input SNR=27.9dB & 3x-Interleaved KP4 FEC

100Gbps/Lane PAM16

- Same baud rate as 53Gbps PAM4 → 26.5Gbaud
- Advantage:
  - Signaling BW (Nyquist) = 13.25GHz (50% less than 106Gbps PAM4)
- Disadvantages:
  - Requires ~14dB higher input SNR to PAM4 for same BER
  - Very High Probability of Error Propagation in DFE :
    - PAM16 (Non-Interleaved KP4 FEC) → Uncorrectable Error Probability=(15/16)^37= 1.11E-1
    - PAM16 (4x-Interleaved KP4 FEC) → Uncorrectable Error Probability=(15/16)^148= 7.11E-5
    - PAM16 (8x-Interleaved KP4 FEC) → Uncorrectable Error Probability=(15/16)^296= 5.1E-9

      → Requires extra ~2dB margin, **total 16dB**, to PAM4 SNR to deliver same BER

- PAM16: BER=1E-15 (Post FEC)→ Input SNR=34.8dB & 8x-Interleaved KP4 FEC