Interleaved Trellis Coded Modulation & Decoding

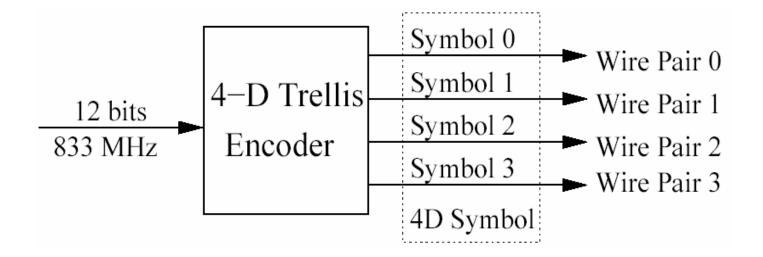
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Coding & Modulation Scheme

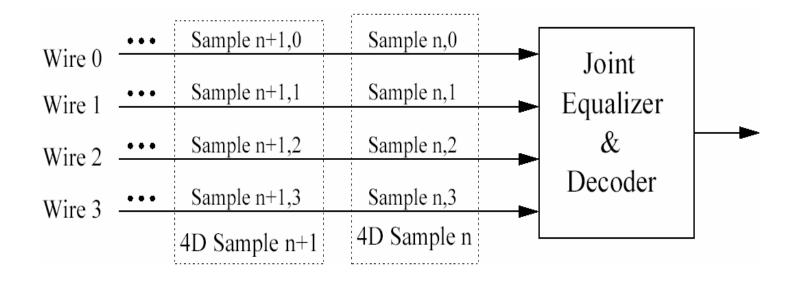
- PAM-10
- 4D, 8-state trellis code
- 12 bits per 4D symbol
- 833 Mbaud

Traditional Trellis Encoding Scheme



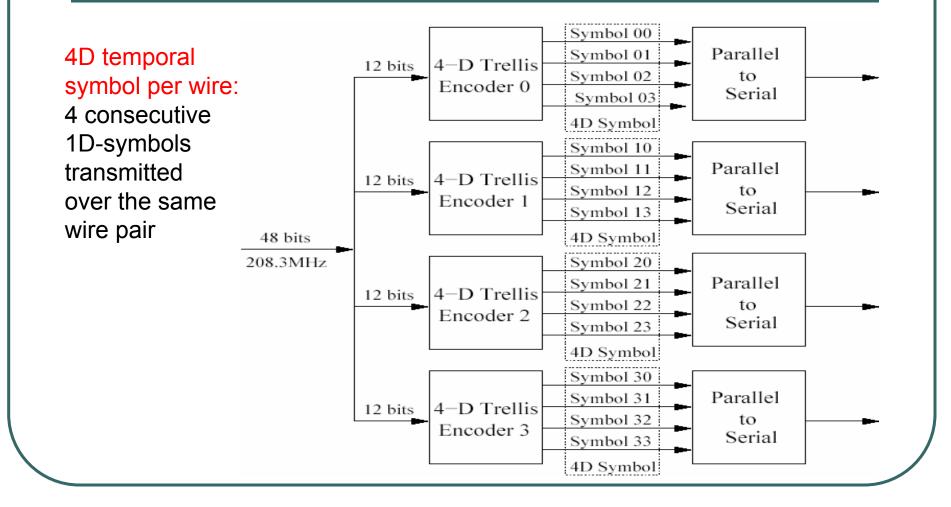
4D spatial symbol: 4 1D-symbols simultaneously transmitted over four different wire pairs (one dimension per pair)

Traditional Decoding Scheme

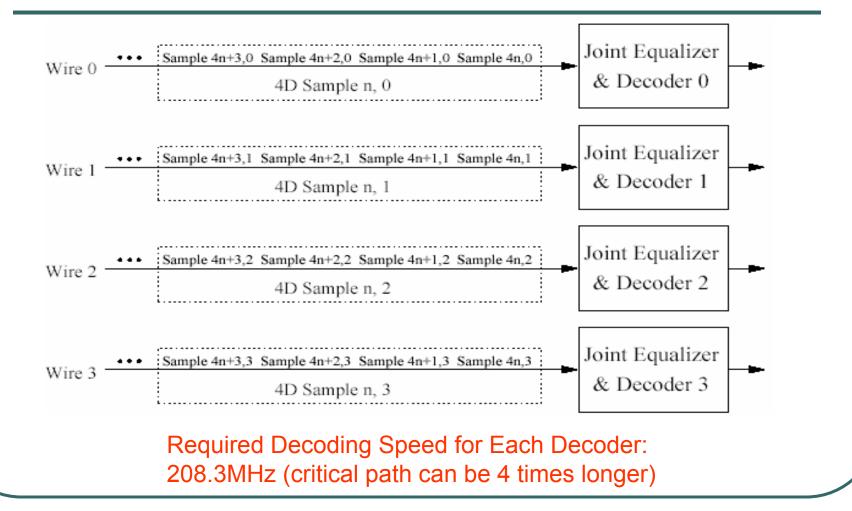


Required Decoding Speed for the Decoder: 833MHz (Clock Speed Hard to Achieve Due to Long Loop Critical Path)

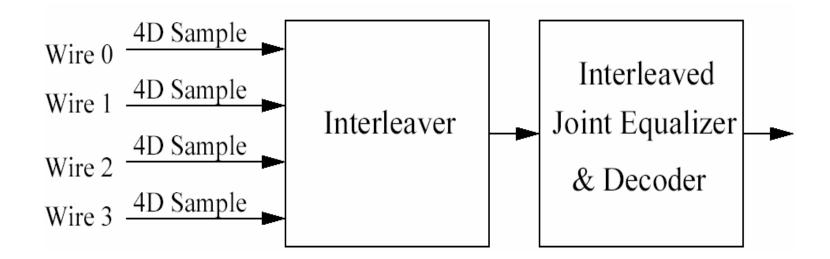
Proposed Interleaved Trellis Encoding Scheme



Interleaved Trellis Decoding Scheme



Interleaved Trellis Decoder

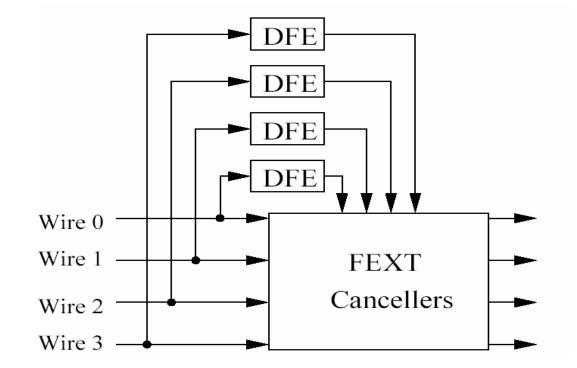


- 1) Low hardware overhead: 1 decoder instead of 4 (Time Multiplexing or folding)
- 2) Each delay in the decoder is replaced by four delays. The critical path is reduced by a factor of 4 after path balancing by retiming.
- 3) Clock speed increased by factor 4 to 833 MHz with 1/4-th critical path of traditional non-interleaved decoder.

Decoder Complexity Reduction

- Dependence among temporal 4 1-D samples due to ISI increases Branch Metric Complexity which Increases Loop Critical Path
- Achievable Speedup may be 3 instead of 4!
- Current work is in progress for complexity reduction

FEXT Cancellation



Conclusion

- Interleaved Trellis Coded Modulation by temporal interleaving
- Reduction of Critical Path by a Factor of 4 makes Decoder Design Easier!
- Proposed Idea is similar to PAM-5 10 Gbps Optical Receiver Proposal for IEEE 802.3-ab (http://grouper.ieee.org/groups/802/3/ae/public/mar0 0/agazzi_1_0300.pdf) (Interleaving exploited for 4 wires instead of 1 cable; Interleaved joint equalizer and decoder instead of parallel)