Working towards ISI generator impulse responses for the comprehensive stressed receiver test

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4th April 2005

Severity of channel responses for robust performance?

During our conference call of 22nd March, Jim McVey requested that the EDC chip suppliers advise on the severity of channel responses for which receivers, using our products, can be designed to perform robustly.

In this presentation we (four EDC chip suppliers nearing completion of products developments) propose a simple process to able us to provide our response.

PIE-D

John Ewen and Robert Lingle, Jr. have shown that

i. Rank ordering of channels for dispersion penalty with an unbounded complexity DFE receiver (this penalty is PIE-D), and

ii. Rank ordering of channels for dispersion penalty with various finite equalizers

do not match.

For this reason, our view is that PIE-D is not a suitable metric of response difficulty or receiver capability, for the purpose of development of the receiver test.

Candidate stressors

John Ewen has shown how to create "ISI generator" impulse responses, each having the property that:

- The dispersion penalty of the resulting stress test response has a uniform rank order position (for a given population of channels) across a wide range of finite equalizers.

We call these "Ewen responses" on the next slide.

Proposed stressor selection process

Ask John Ewen to provide three sets of "Ewen responses":

- A pre-cursor set, a post-cursor set and a symmetric set;
- Each to be a family of graduated difficulty responses (with PIE-D values in range 3.5dB to 4.5dB).

For each of these three sets of responses:

- We (EDC chip suppliers) will use our knowledge and experience with our products to identify the most severe of the responses for robust, volume manufacture of 10GBASE-LRM modules using our chips.

The result will be our response to Jim McVey's request.

Analysis considerations

Primary objectives for 10GBASE-LRM

- Low cost - PAR is very specific about this;
- Low power - PAR is specific about requirement for support of serial form-factor modules;
- Need for manufacturing margin (for high yield, volume, manufacturing). This is a cost consideration;
- Time to market imperative.

Implementation non-idealities. These include:

- Manufacturing spreads (photo detector, TIA as well as equalizer);
- Implementation impairments;
- Variations in performance with temperature and voltage.

Conclusion

We have presented an approach that will enable us (four EDC chip suppliers) to respond to Jim McVey request for advise on the severity of channel responses for which receivers, using our products, can be designed to perform robustly.

The method results in a quantitative response that is appropriate for real, finite complexity equalizers. It enables us to take into account the knowledge and experience gained during the development of our products.