10Gb/s Physical Layer Options & Coding Issues

John Ewen
IBM Corporation
3605 Highway 52 North
Rochester, MN 55901

Phone: +1 507 253 0799
Email: jfewen@us.ibm.com

Outline

- Physical Layer Options
  - Parallel & Serial
- Laser Safety for Parallel Optics
- Coding Issues: 8B/10B
  - Characteristics
  - Circuit Implications
Technology Cost/Performance Options

Box-Box Environment: 10x 1Gb/s Parallel

Advantages
- reuses existing technology
- low speed electronics and OE devices
- lower terminal cost

Disadvantages
- 10x laser diodes
- laser safety & reliability
- higher media cost (ribbon cable)
Parallel Optics Issues

△ Opportunity to reallocate link budget
  ● Little or no installed base of ribbon cable
  ● specify high-bandwidth fiber
  ● relax requirements on Tx and Rx
    ■ Tx minimum launch power
    ■ extinction ratio
    ■ Rx sensitivity

△ Class 1 laser safety
  ● total launch power of multiple links constrained by safety limit
    ⇒ severe link budget constraints
  ● implement handshaking to allow reasonable link budget

Laser Safety

△ Open Fiber Control (OFC)
  ● maximum flexibility in launch power
  ● maximum complexity
  ● long response times

△ Safety Channel Approach
  ● one channel must be inherently Class 1 safe
  ● handshaking protocol to enable other links when fiber is connected
  ● minimize complexity and impact at system level
Safety Channel

- Designate one channel as the master "safety channel"
- Safety channel must be Class 1 safe at all times
- Loss-of-signal (LOS) detected by receiver
  - transmitter disables N-1 channels (no light)
  - safety channel remains active
- Transmitter enables all channels when LOS is not active
- Advantages
  - launch power not reduced relative to serial links
  - maintain reasonable link budgets & Class 1 safety
  - minimal delay

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Campus Environment: 10Gb/s x 1 Serial

- "OLM"-like partitioning
  - link rate signals remain in the module
  - multi-byte low speed interface
  - options
    - potential to integrate framer & serdes (BiCMOS)
    - integrate framer with adapter logic
10Gb/s Clock & Data Recovery Circuit

Input Eye Diagram

Regenerated Output Eye Diagram

Recovered Clock

Block Coding vs. Scrambling

- Common Objective: lowest total system cost

LAN Environment
- Terminal cost dominates
  - highly integrated circuits
  - ASIC technologies
  - coding enables low-cost implementations
  - class 1 laser safety required

WAN Environment
- Infrastructure cost dominates (distance is paramount)
  - coding efficiency
  - launch power
  - low loss (1550nm)
**Coding Terminology**

- **Run-Length**
  - number of consecutive 1's or 0's (binary symbols)
- **Running Digital Sum (≡ running Disparity)**
  \[ b_k = \sum A_k \delta(t - kT) \quad \text{RDS} = \sum A_k \]
- **Digital Sum Variation**
  - peak-to-peak difference between minimum and maximum running digital sum
  - bounded DSV \(\leftrightarrow\) spectral null at DC
- **Normalized offset**
  - RMS average of the running digital sum
  - useful estimate of the low frequency content
- **Comma**
  - indicates proper byte boundaries
  - can be used for instantaneous acquisition or verification of character & word boundaries
  - cannot occur in any other bit positions within a character or between characters
- **Special (or control) characters**
  - valid transmission character which does not translate into a valid data byte

**Examples**

- **8B/10B**
  - Fiber Channel
  - 1000BASE-X
  - P1394
  - Max. run-length= 5
  - Digital sum variation= 6
  - error detection
  - comma or control characters available

- **4B/5B**
  - HPPI-6400
  - Max. run-length= 11
  - Digital sum variation= 13
  - some error detection (based on disparity)
  - no comma or control characters

- **Scrambling**
  - SONET / SDH
  - Max. run-length= statistical
  - Digital sum variation= statistical
  - no error detection
  - no comma characters
8B/10B Benefits

- 256 data values (8 bits) and 12 special characters (e.g. command, Byte Sync) yielding a total of 268 encoded sequences.
- Maintains DC balance
- No more than 5 running 0’s or 1’s.
- K28.5 ("comma") character is unique regardless of combination of data/phase.
- Improves data reliability (monitor code violations)
- Has a simple, fast encoding/decoding scheme.

8B/10B Characteristics

- 256 data values (8 bits) and 12 special characters (e.g. command, Byte Sync) yielding a total of 268 encoded sequences.
- The 8 data bits split into 3 + 5 bits. The 3 bit field is encoded into 4 bits, the 5 bit field is encoded into 6 bits totaling 10 encoded bits.
- Of the 268 encoded characters, 134 are balanced.
- Each of the disparity dependent characters has an analog with the opposite sign
- The sum of the disparity of both versions of an encoded character is always 0.
- Which of the two versions of the characters sent on the link is dependent on the current value of the running disparity.
- Maximum error spread is 5.
Circuit Implications: Baseline Wander

Cutoff = 0.1% baud rate

Worst case 8B10B pattern

SONET CID pattern

Circuit Implications (cont.):

▲ Long run-lengths ⇒ narrow PLL bandwidths
  • larger filter components required
    □ may not be able to integrate filter on chip
    □ more board/module real estate
    □ more cost
  • increased clock jitter
    □ intrinsic phase noise becomes more important
    □ susceptibility to power supply noise increases
**8B/10B Implementation**


![Diagram of 8B/10B implementation](image)

- **CMOS Framer**
  - coding
  - byte/word synchronization
  - >20 Gb/s possible with 0.18μm CMOS technology
- **GaAs or Si(Ge) Serdes**
  - simple MUX/DEMUX
  - clock generation & recovery
  - serial interface to OE
- **Possible integration using BiCMOS technologies**
8B/10B Summary

- Comma & control characters available
  - byte, word, & frame synchronization
- Error detection (code violations)
  - *any* odd number of bit errors will cause a code violation
  - *many* even number of bit errors will also cause code violations
  - code complements CRC
  - error correction option
- Well controlled frequency spectrum
  - max. run-length of 5, DSV= 6
  - good transition density (min. of 30% in data)
  - minimal baseline wander (easy AC coupling)
- Coding efficiency
  - 25% overhead (symbol rate)

  *enables low-cost implementations in an ASIC environment*

Summary

- Multiple PHY options should be defined
  - LAN and WAN requirements are significantly different
- Parallel optics is a viable option for short distances
- 10Gb/s serial for building and campus environments (and beyond)
  - good line coding essential for low cost implementations
  - 8B/10B proven in high speed LAN environment