

Low overhead coding proposal 10GbE serial links

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Outline

- Goals
- Motivation
- Code Overview
- Code Properties
- Comparison to SONET
- Typical Application
- Summary



Goals

- provide full 10.000 Gb/s bandwidth for LAN applications
- provide PMD for long-distance (10km - 40km+) LAN requirements
- interface directly to common MAC/PCS/PMA interface (HARI, 4x3.125 GBaud) with control code transparency
- ensure robust DC-balance, transition-density, and frame synchronization properties suitable for either copper or fiber transmission
- achieve a low enough coded baud-rate to be compatible with existing SONET laser designs

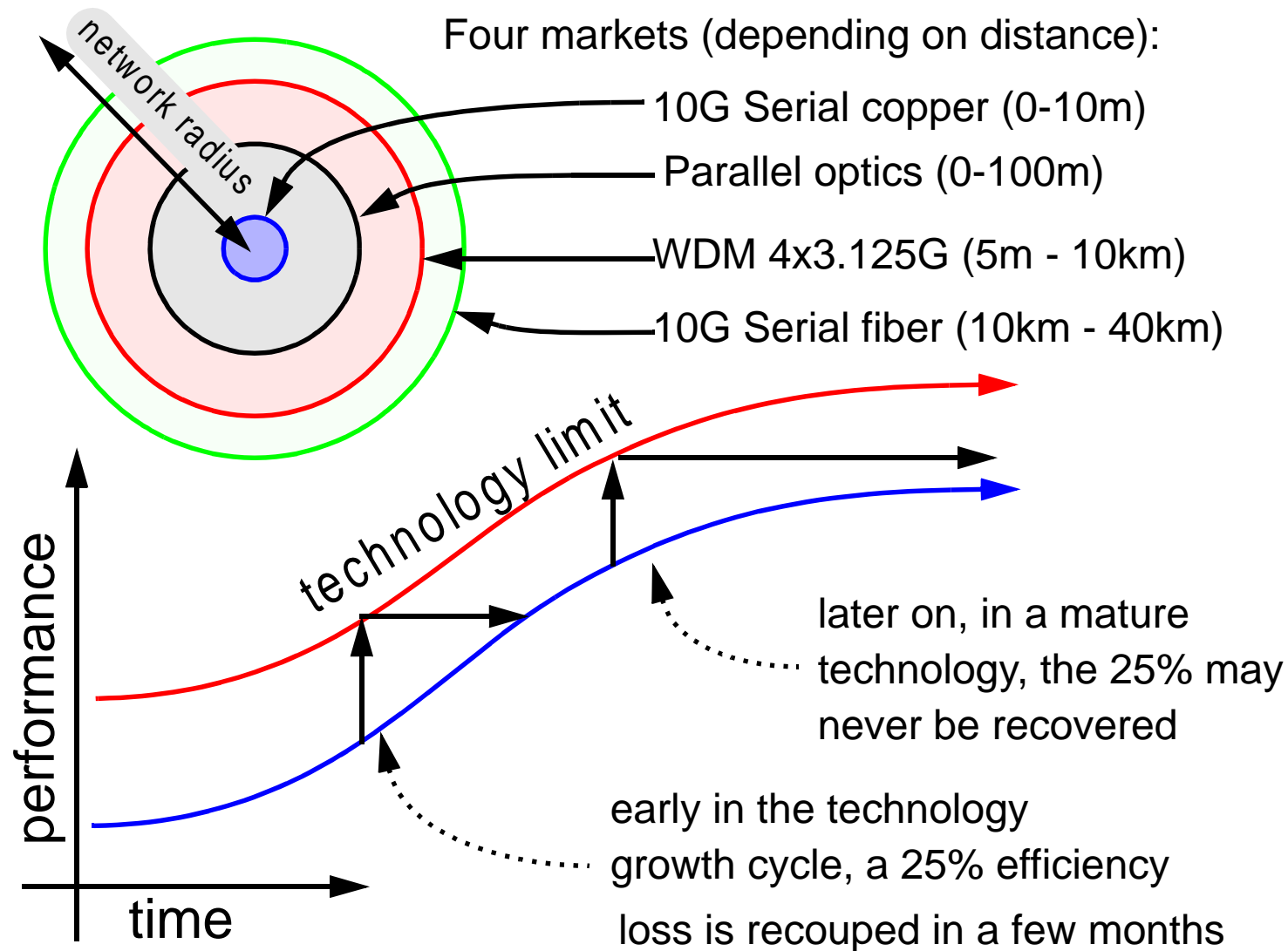


Motivation

- Both optics and copper implementations become much more difficult to implement above 10 Gbaud
- An efficient code can leverage existing SONET 10Gbaud lasers rather than requiring fundamentally new technology
- A simple code can be efficiently implemented in many processes

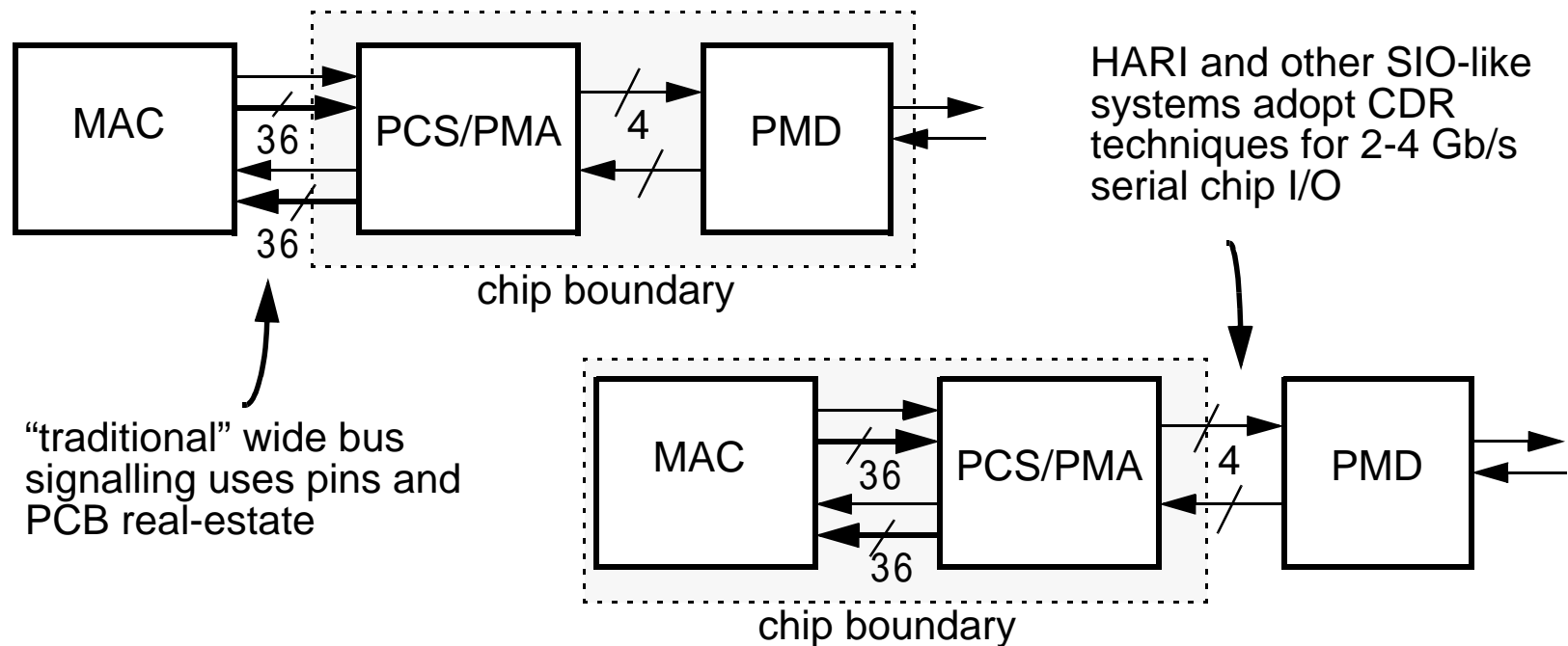


Why an efficient 10Gb serial code?



Two views of the future

- System density and performance put increasing pressure on pin and package count
- 2-4 Gb/s serial links will be pervasive in future designs



Overview of Code

If octets are either data or control, then at least an 8B/9B code is required - hardly a significant improvement over 8B/10B.

Two properties of HARI 10GbE proposal allow for a more efficient code:

- Only a limited number of control characters are needed (K,R,S,T,E...) which can be coded in 7 bits.
- Data is transmitted in contiguous blocks of at least 64 octets always starting with S and ending with T.

If we code on 64 bit (8 octet)-sized blocks, each block can only contain one transition from control to data or vice-versa.

A two-bit preamble allows frame synchronization and gives a 66/64 code with only 3.125% overhead



Overview of Code (cont.)

Data Codewords have “01” sync preamble

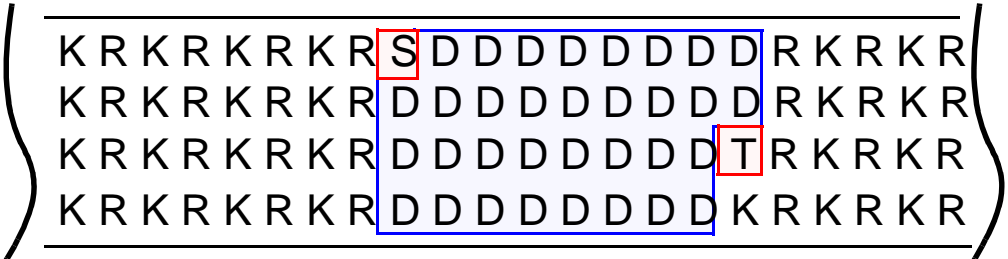


Mixed Data/Control frames are identified with a “10” sync preamble. The coded 56 bit payload and TYPE field is also scrambled.



00,11 preambles are considered as code errors

Building frames with proposed HARI 10GbE mapping

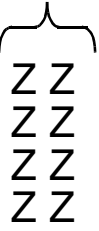


S,T = SOP, EOP
 K,R = control words (Z)
 D = Data octets

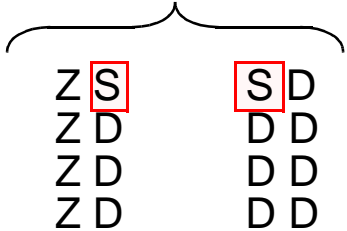
pure data



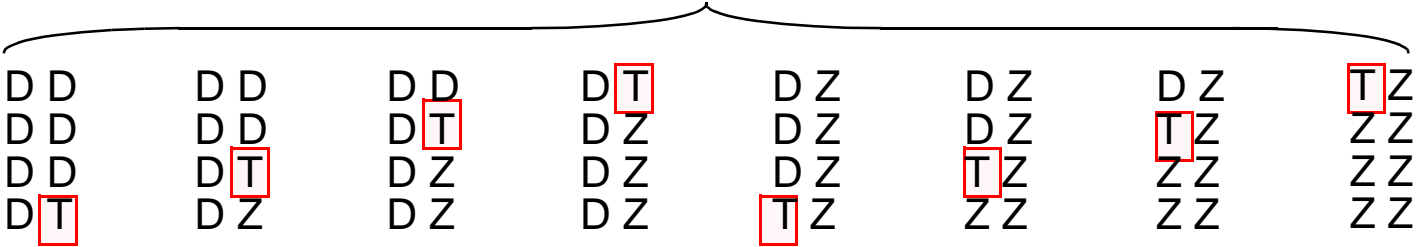
pure control



two possible packet startings

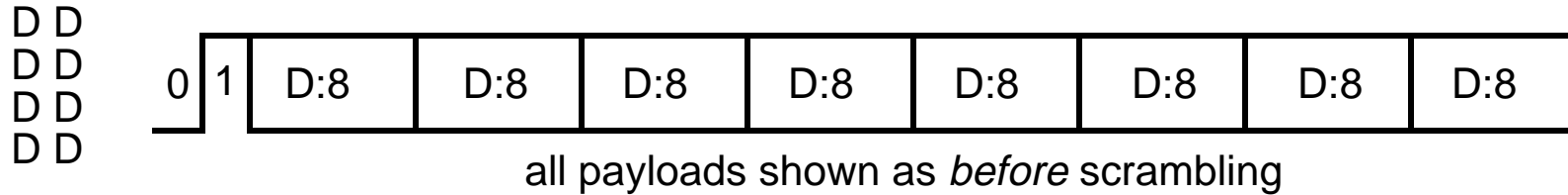


eight possible packet endings

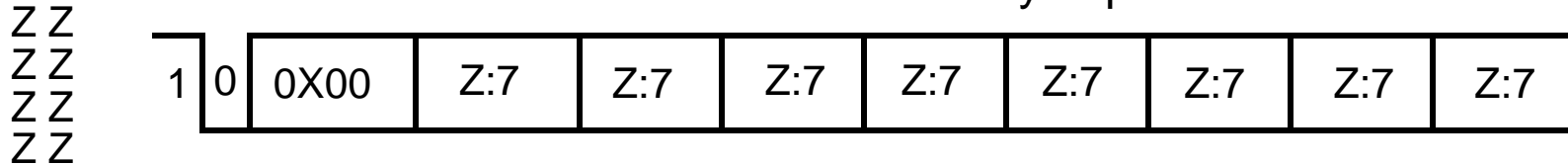


Code definition

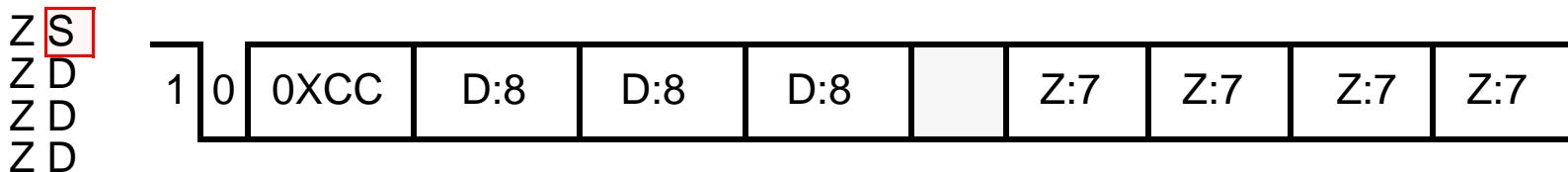
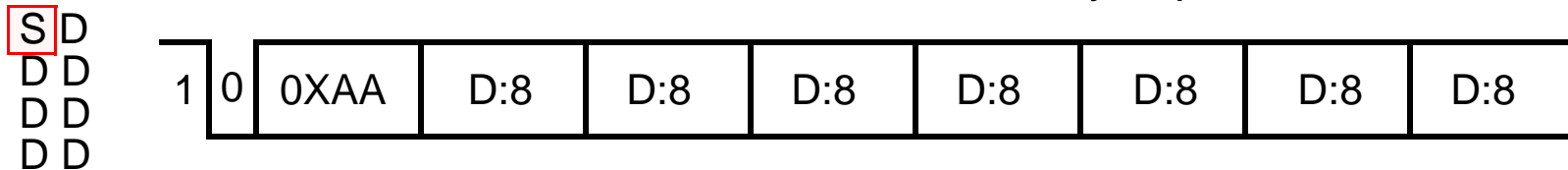
Pure Data Frame with 01 sync preamble



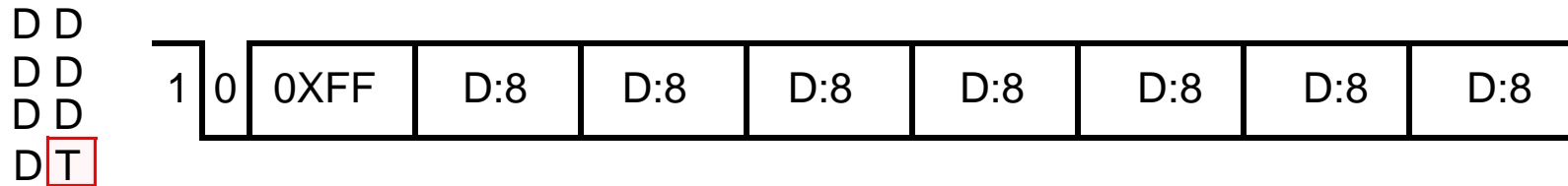
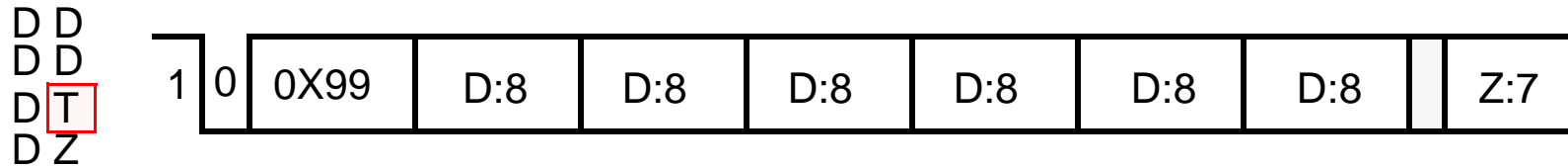
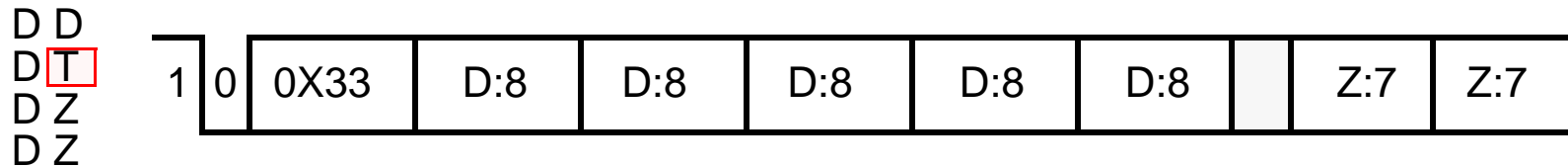
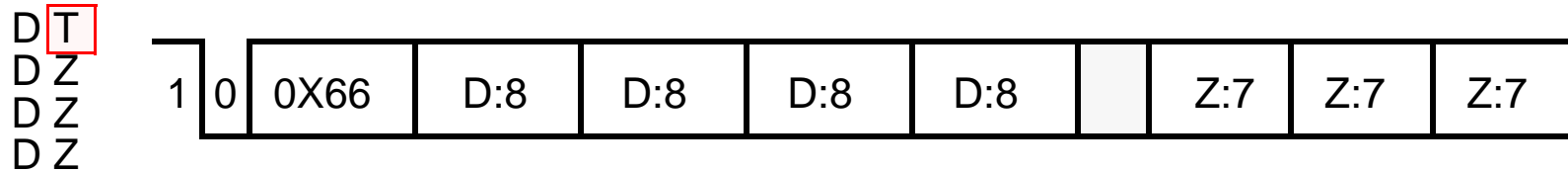
Pure Control Frame with 10 sync preamble



Mixed Data/Control Frames with 10 sync preamble



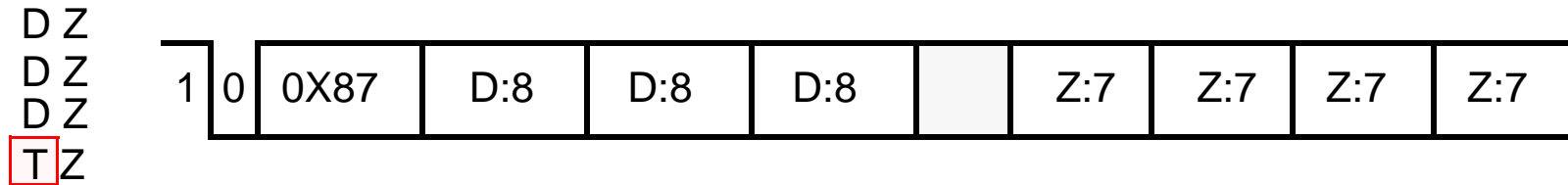
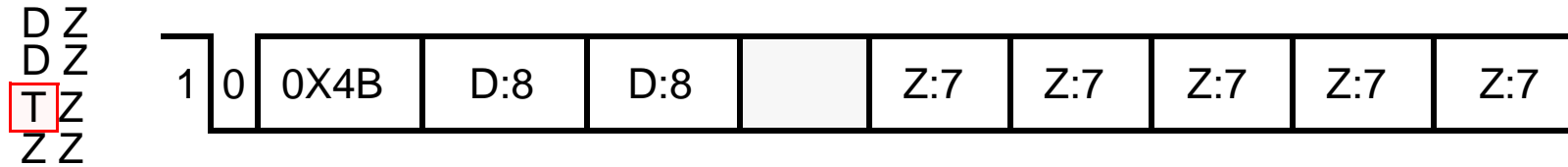
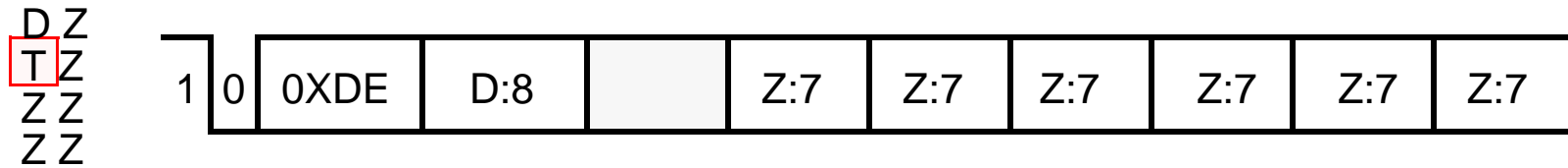
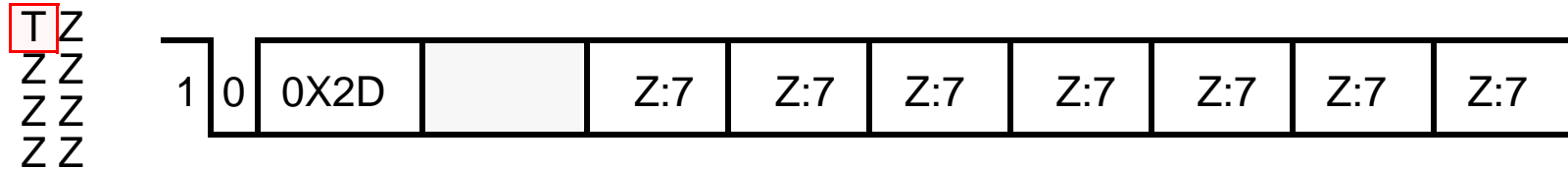
Code definition (cont.)



SOP (S) and EOP (T) are implicitly transmitted by the TYPE byte

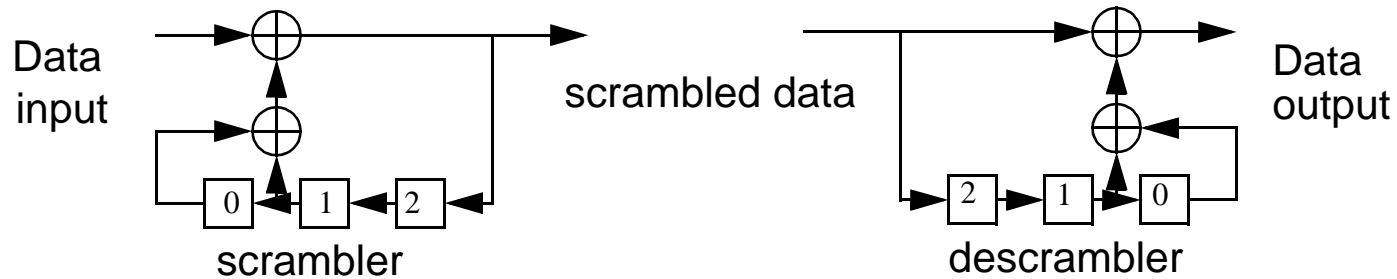


Code definition (cont.)

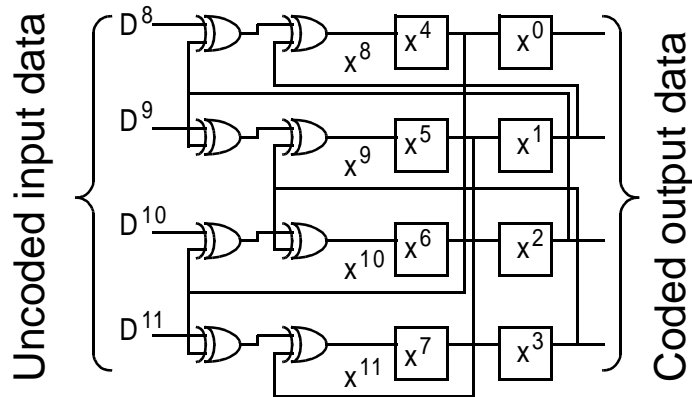


Scrambling principle

example scrambler/descrambler in serial form:



parallel form:



- Self synchronizing (Westcott-style scrambler)
- Can be parallelized for efficient implementation
- Recommend long pattern length to reduce possibility of jamming (eg: $x^{31}+x^3+1=0$)
- Long pattern length self-synchronizing scramblers exist that do not compromise Ethernet CRC coverage

Code Properties

- maximum run-length is guaranteed to be 64 or better due to 2-bit preamble (better than SONET)
- DC balance is suitable for laser transmission (slightly better than SONET)
- overhead is $66/64 = 1.03125$
- frame lock is acquired by bit-slipping the de-multiplexor until the complementary 2-bit preamble bits are found to be statistically stable.
- Alternatively, 64-bit frame boundaries can be rapidly acquired using the handshake scheme in Walker, et al. "A 1.5 Gb/s Link Interface Chipset for Computer Data Transmission", IEEE JSAC, V9 No. 5, June 1991.



Comparison with SONET

- two-bit preamble is analogous to SONET's A1/A2 sync bytes.
- SONET CDRs are designed to accommodate an 80 bit run length. This new code is deterministically limited to 64 bit run length due to the periodic preamble bits.
- Both codes use similar bit-slipping method to acquire frame sync.
- This code is similar in spirit to the SONET code. It is not in any way compatible, but inherits much of SONET properties while being much simpler to implement.
- Much less on-chip buffering required
- Lower latency

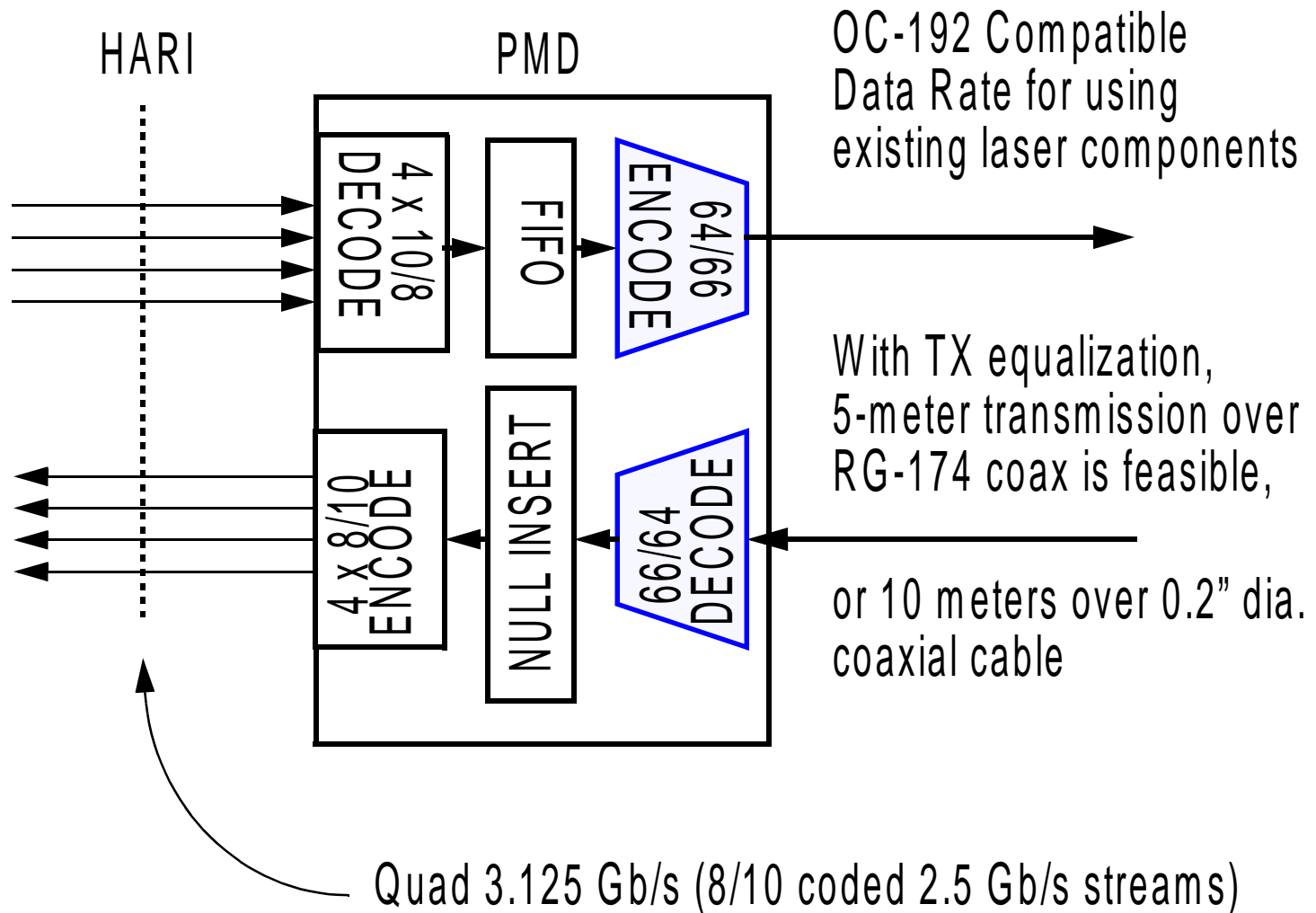


Code Robustness

- 2 bit Hamming distance between data (01) and mixed frames (10)....code could be modified to have 3 bit distance at the cost of raising overhead from 3.1% to 4.7%
- TYPE fields within mixed frames have 4-bit Hamming distance
- There exist long-period scramblers that do not impair CRC coverage and are difficult to jam (details can be provided)



A possible implementation



Conclusion

- A simple, low overhead SONET-like code is possible
- HARI (4 x 3.125Gbaud) becomes a common interface for all PMDs:
 - 4-color WDM (Spectra-LAN)
 - Parallel fiber
 - 0.5 meter chip-chip, card-card interface on PCB
 - Serial 10.3 Gb/s (copper to 15m, fiber to 40km)

