400G Optical Transceivers

Economic Comparisons in Silicon Photonics

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Background Materials

1. 400G PMD Requirements for Broad Market Potential
   - http://www.ieee802.org/3/400GSG/public/13_07/palkert_400_01_0713.pdf

2. An Economic Comparison of PSM4, PAM, and LR4
   - http://www.ieee802.org/3/bm/public/jan13/welch_01b_0113_optx.pdf

3. SMF Link Costs over Time
   - http://www.ieee802.org/3/bm/public/jul13/welch_01_0713_optx.pdf

400G Optical Transceivers: Economic Comparisons

- **This presentation is** an economic comparison of potential 400G optical transceivers

- **This presentation is not** a technical comparison of potential 400G optical transceivers

400G Optical Transceivers: Economic Comparisons

- Compares: Module and Link Costs (vs. Distance)
  - Using a material basis [2]
- Assumes all solutions are equally technically feasible.
  - No parametric yield impairments for ‘harder’ solutions
- Assumes all solutions are shipping in the same volume
- Does not include amortization of development cost in cost comparisons
- Doesn’t look at all potential solutions
  - Tries to cover the ‘space’, from simple to complex

Potential Solutions under Comparison

First Generation

- PSM16
  - Electrical: 16x25 Gbps
  - Optical: 16x25 Gbps
- 4xPAM4
  - Electrical: 16x25 Gbps
  - Optical: 4x100G (PAM4)
- 4λ-PAM4
  - Electrical: 16x25 Gbps
  - Optical: 1x400G
    - 4λ LWDM
    - PAM4

Comparison Baseline: 100G – PSM4

Second Generation

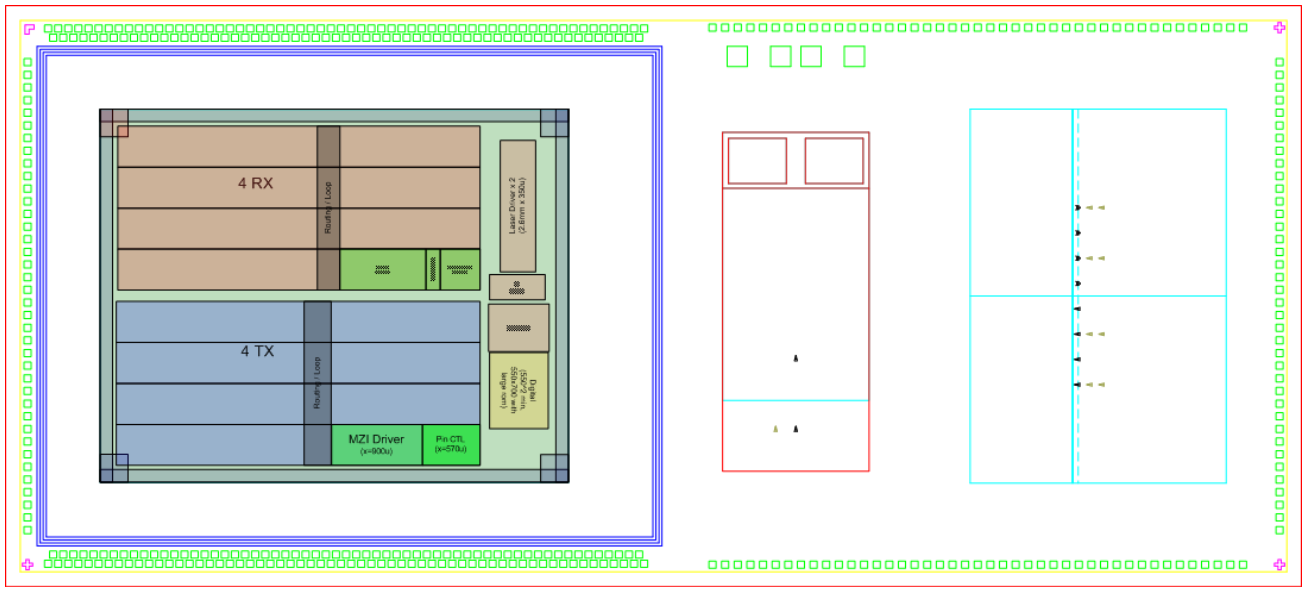
- PSM8
  - Electrical: 8x50 Gbps
  - Optical: 8x50 Gbps
- 4xPAM4
  - Electrical: 8x50 Gbps
  - Optical: 4x100G (PAM4)
- 4λ-PAM4
  - Electrical: 8x50 Gbps
  - Optical: 1x400G
    - 4λ LWDM
    - PAM4

Only PSM8 is an envisioned optical spec revision between First and Second Generations

Module Costs

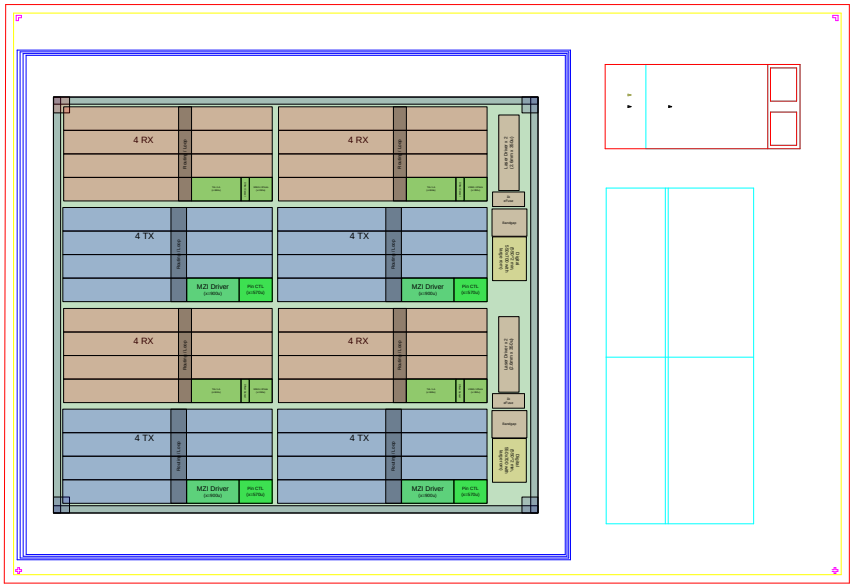
PSM4 – From Welch_01b_0113_optx

	Area / Count	per Wafer
Silicon Photonics Area	68 mm^2	880
CMOS Area	17 mm^2	3576
Light Source(s)	1	3000



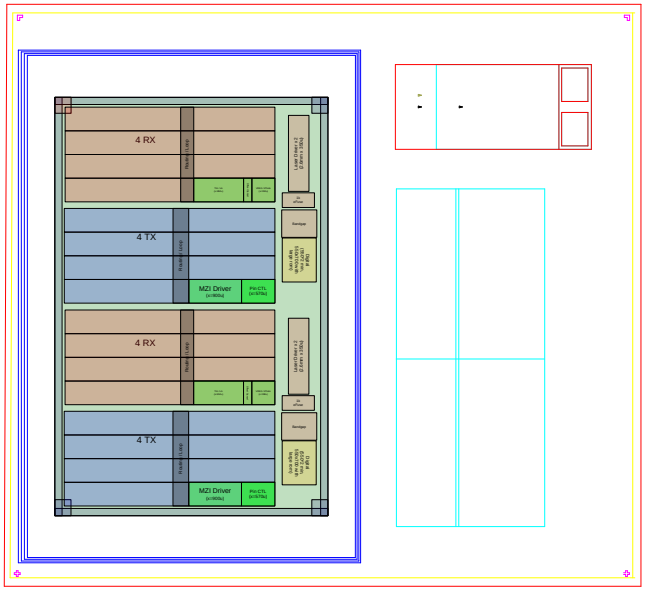
PSM16 and PSM8

PSM16 – Gen 1



	Area / Count	per Wafer
Silicon Photonics Area	144 mm^2	408
CMOS Area	60 mm^2	1020
Light Source(s)	1	2400-3000

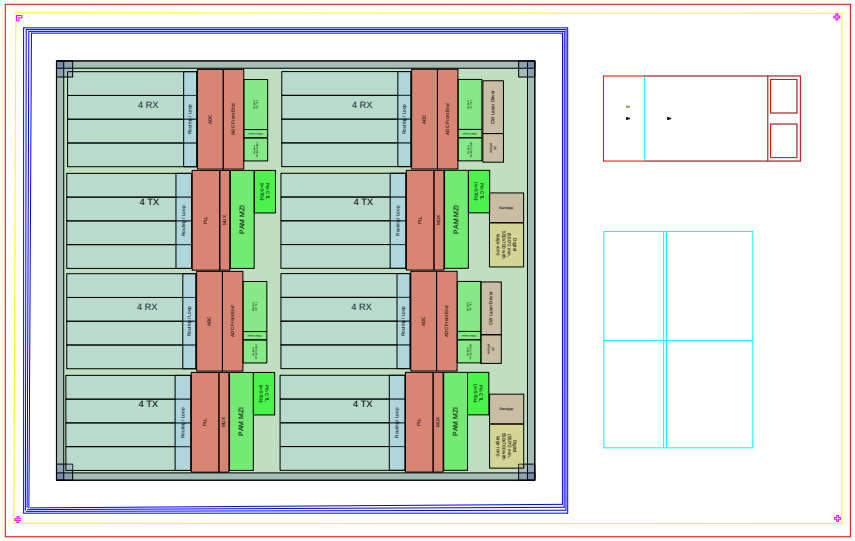
PSM8 – Gen 2



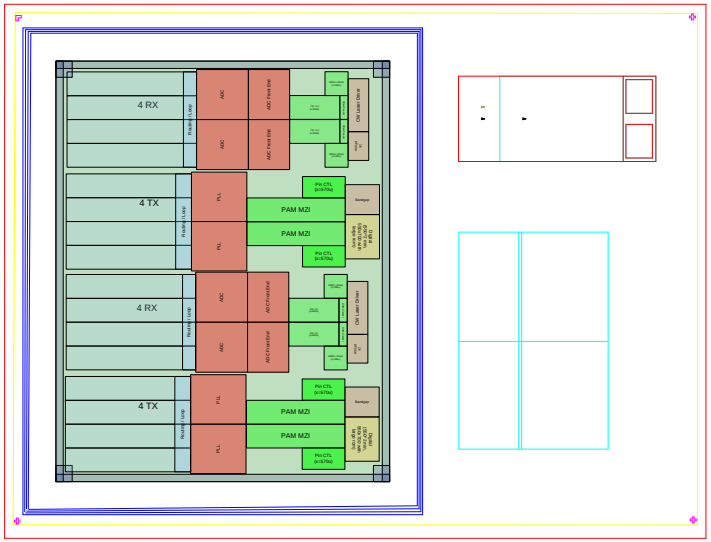
	Area / Count	per Wafer
Silicon Photonics Area	108 mm^2	553
CMOS Area	33 mm^2	1827
Light Source(s)	1	2400-3000

4xPAM4

4xPAM4 – Gen 1



4xPAM4 – Gen 2

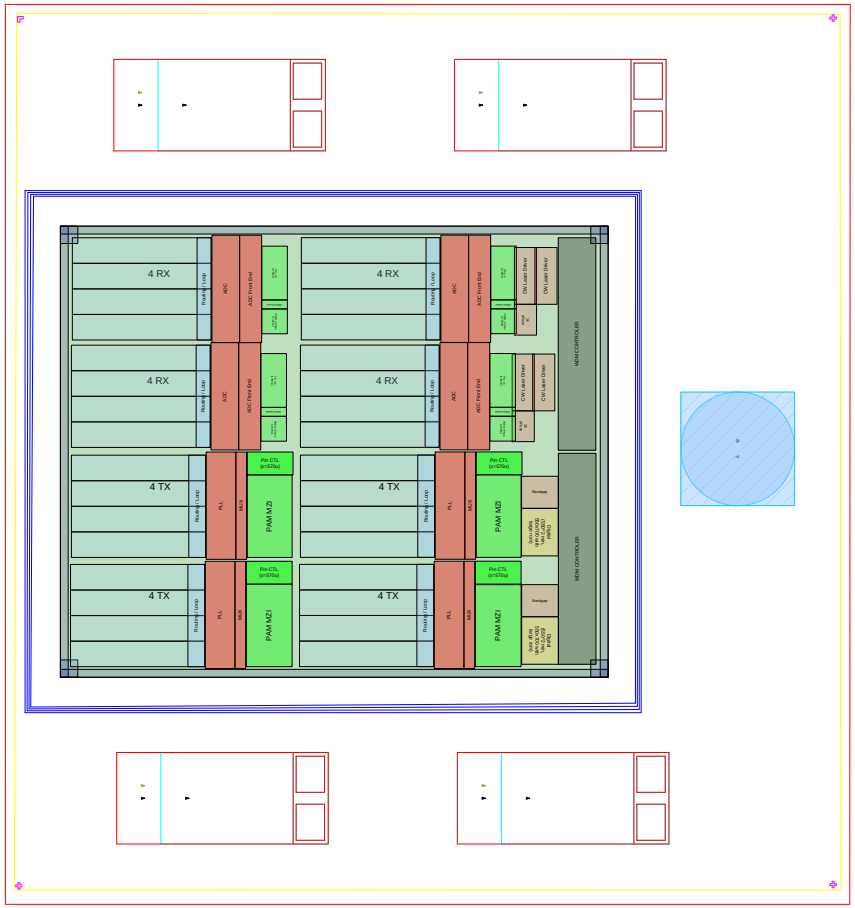


	Area / Count	per Wafer
Silicon Photonics Area	130 mm^2	453
CMOS Area	58 mm^2	1052
Light Source(s)	1	2400-3000

	Area / Count	per Wafer
Silicon Photonics Area	108 mm^2	552
CMOS Area	40 mm^2	1509
Light Source(s)	1	2400-3000

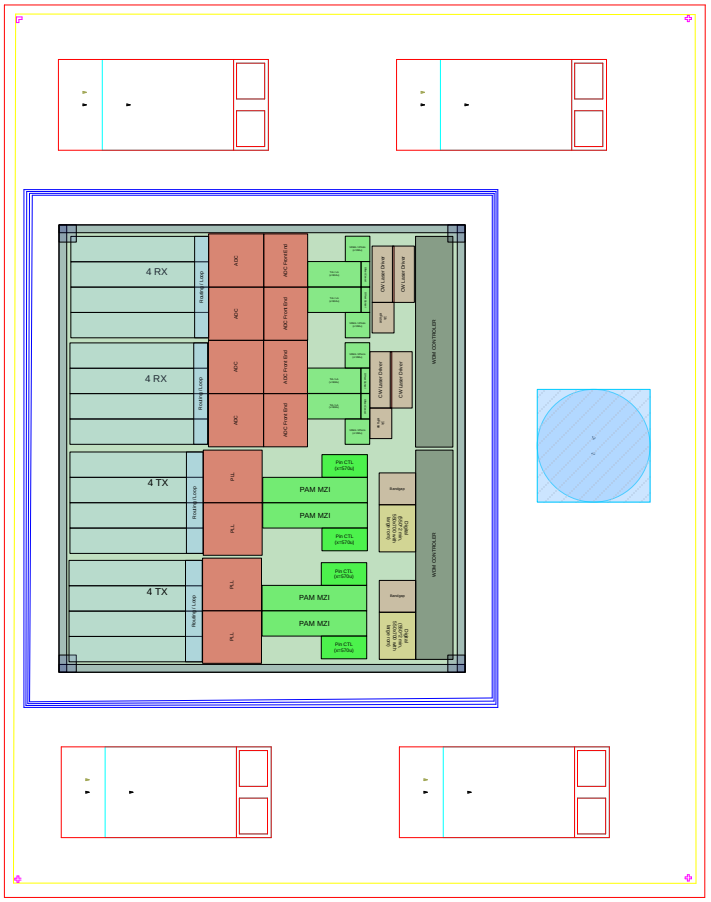
4λxPAM4

4λxPAM4 – Gen 1



	Area / Count	per Wafer
Silicon Photonics Area	191 mm^2	306
CMOS Area	62 mm^2	975
Light Source(s)	4	600-750

4λxPAM4 – Gen 2



	Area / Count	per Wafer
Silicon Photonics Area	159 mm^2	370
CMOS Area	46 mm^2	1314
Light Source(s)	4	600-750

Chipset BOM Comparison

DPW	PSM4	PSM16	4xPAM4-G1	4λxPAM4-G1	PSM8	4xPAM4-G2	4λxPAM4-G2
Silicon Photonics IC	880	408	453	306	553	552	370
CMOS IC	3576	1020	1052	975	1827	1509	1314
Light Source(s)	3000	2400	2400	600	2400	2400	600

Relative Cost	PSM4	PSM16	4xPAM4-G1	4λxPAM4-G1	PSM8	4xPAM4-G2	4λxPAM4-G2
Silicon Photonics IC†	0.67	1.45	1.30	1.93	1.07	1.07	1.59
CMOS IC	0.33	1.16	1.12	1.21	0.65	0.78	0.89
CMOS Total Area	*1.00*	*2.61*	*2.42*	*3.14*	*1.72*	*1.85*	*2.48*
Light Source(s)	1†	1	1	4	1	1	4

† May use lower power light source

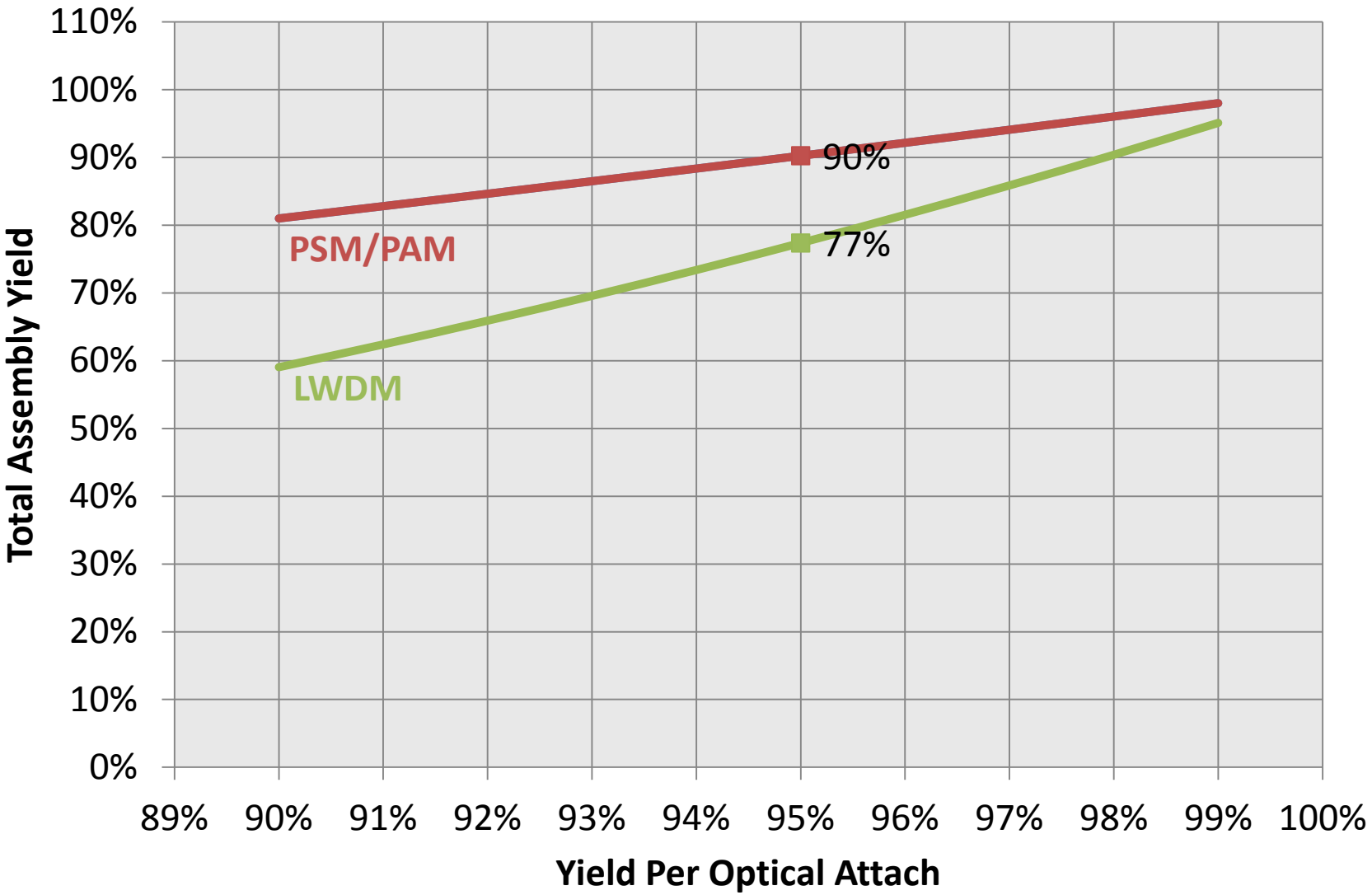
Module Comparison - BOM

Components	PSM4	PSM16	4xPAM4-G1	4λxPAM4-G1	PSM8	4xPAM4-G2	4λxPAM4-G2
CMOS Total	1.00	2.61	2.42	3.14	1.72	1.85	2.48
Light Source(s)	1	1	1	4	1	1	4
TEC(s)	0	0	0	4	0	0	4
Optical Coupler	8 Fiber	32 Fiber	8 Fiber	2 Fiber	16 Fiber	8 Fiber	2 Fiber
Optical Connector	8 Fiber	32 Fiber	8 Fiber	2 Fiber	16 Fiber	8 Fiber	2 Fiber
PCB	1	1	1	1	1	1	1
Housing	1	1	1	1	1	1	1

Module Cost	PSM4	PSM16	4xPAM4-G1	4λxPAM4-G1	PSM8	4xPAM4-G2	4λxPAM4-G2
Chipset	2	4.11	3.92	11.14	3.22	3.35	10.48
Normalized Module (Un-Yielded)†	1	2.05	1.96	6.6	1.61	1.66	5.27

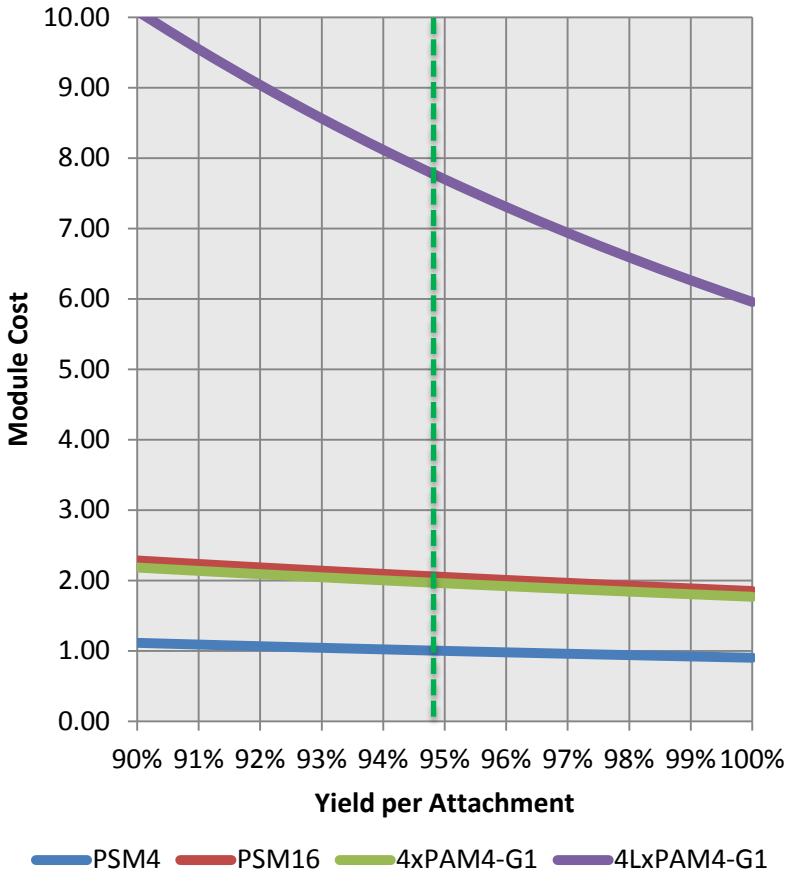
† With Packaging and Transformation Costs Applied

Module Assembly Comparison - Yield

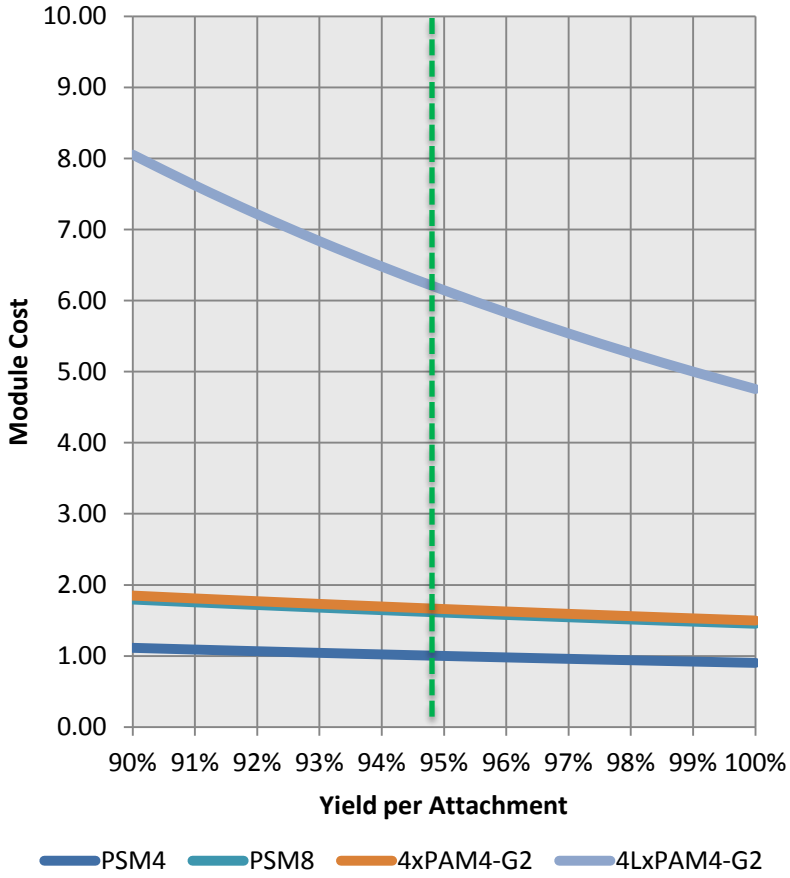


Yielded Module Cost

First Generation



Second Generation

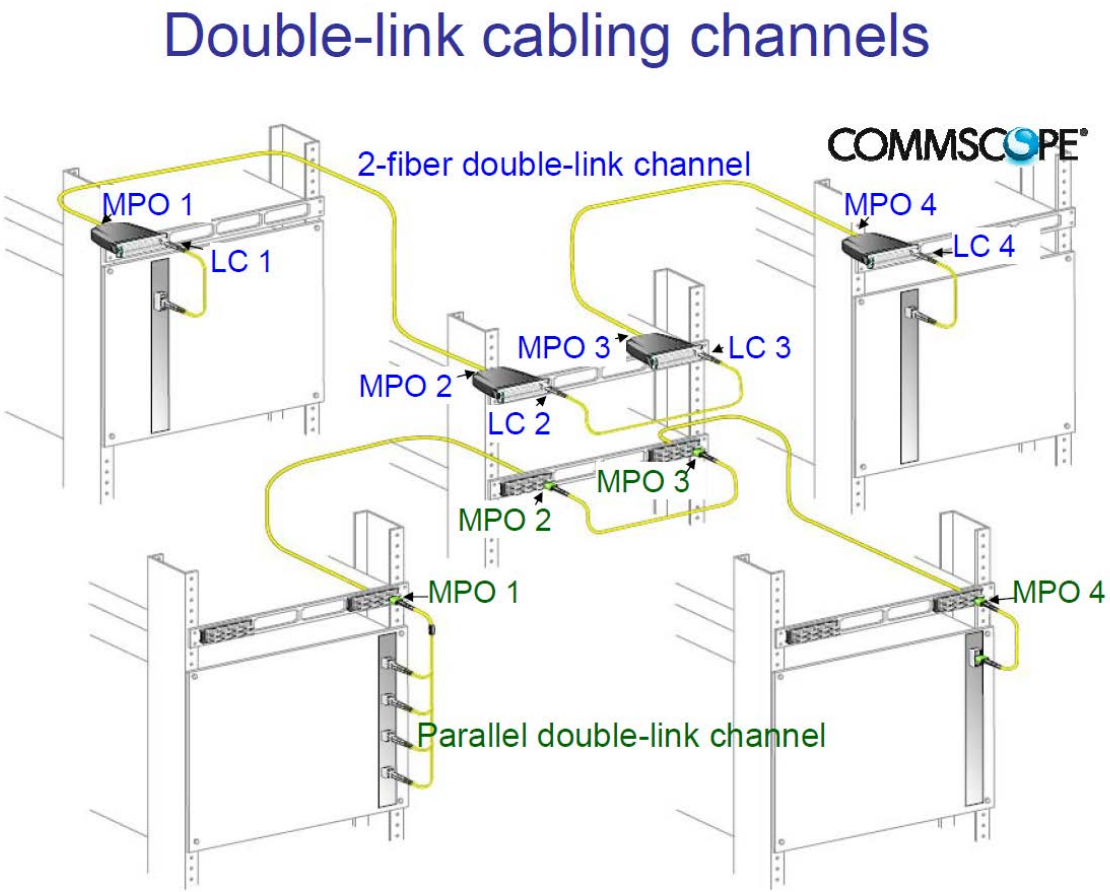


Module Cost	PSM4	PSM16	4xPAM4-G1	4λxPAM4-G1	PSM8	4xPAM4-G2	4λxPAM4-G2
@ 95% Yield	1	2.05	1.96	8.53	1.61	1.66	6.81

Link Costs

Link Costs

- Uses link architectures from kolesar_02_0313_optx.pdf



Link Cost Methodology

- Prior Modeling Methodologies:
  - Summation Model (2xModule Cost + Fiber Plant Cost)
    - Pros: Simple
    - Cons: Does not account for different lifetimes of modules and fiber plant
  - NPV Model
    - Pros: Accounts for the different lifetimes of modules and fiber plant
    - Cons: Requires assumptions about future module costs
- New Modeling Methodology:
  - Depreciation Model (2xModule Cost + Depreciated Value of fiber plant)
    - Pros:
      - Accounts for different lifetime of modules and fiber
      - Does not require any assumptions on future module costs
- Other Updates:
  - Revised materials costing on fiber and connectors

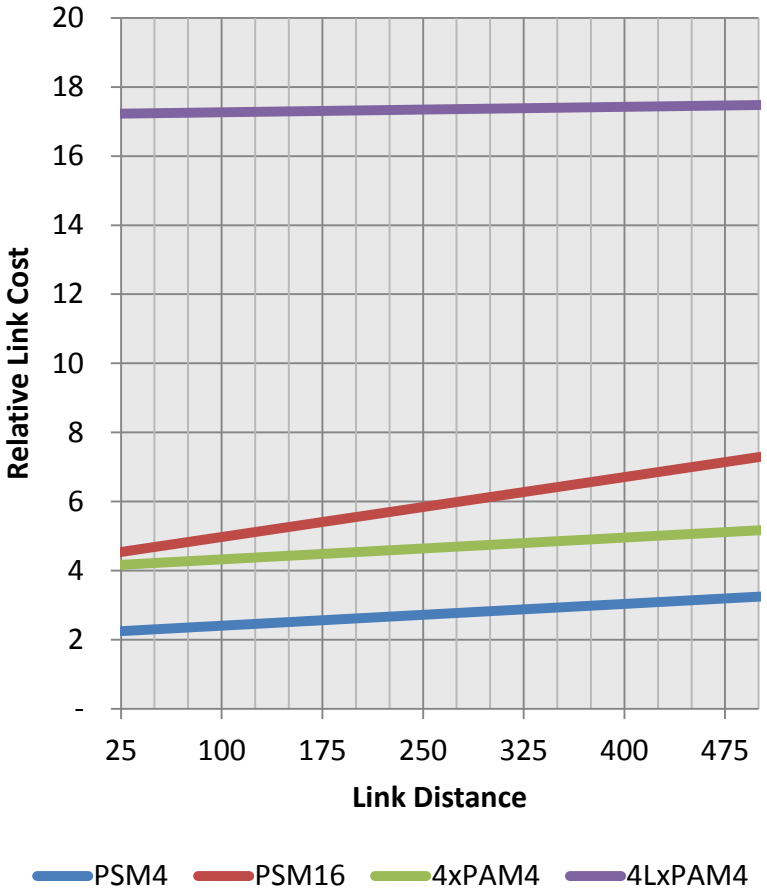
Depreciation Model

- Uses MACRS depreciation table to derive 'value used' of a fiber plant.
  - Years 0 and 10 are ½ years
- Assumes 10 year average life of fiber plant
- Assumes 3.5 year average life of module
- 'Depreciated value' over said time is:
  - 0.1+0.18+0.144+0.115 = 0.539
  - 53.9% of Fiber plant value consumed in first generation

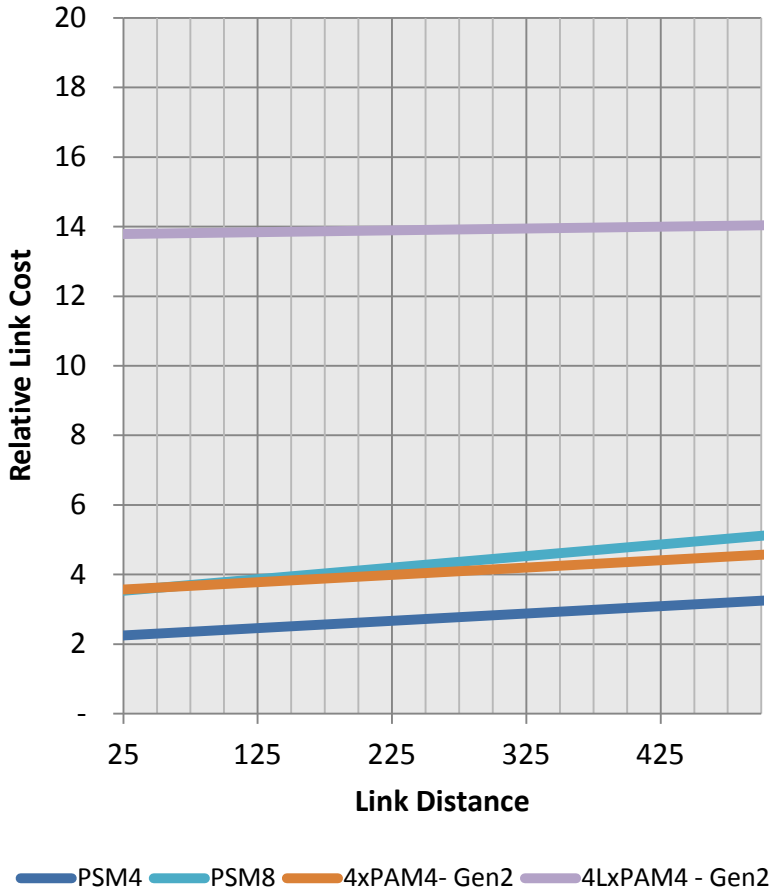
Year	Depreciation
0	0.1
1	0.18
2	0.144
3	0.115
4	0.092
5	0.074
6	0.066
7	0.066
8	0.065
9	0.065
10	0.033

Link Costs – 25m to 500m

First Generation

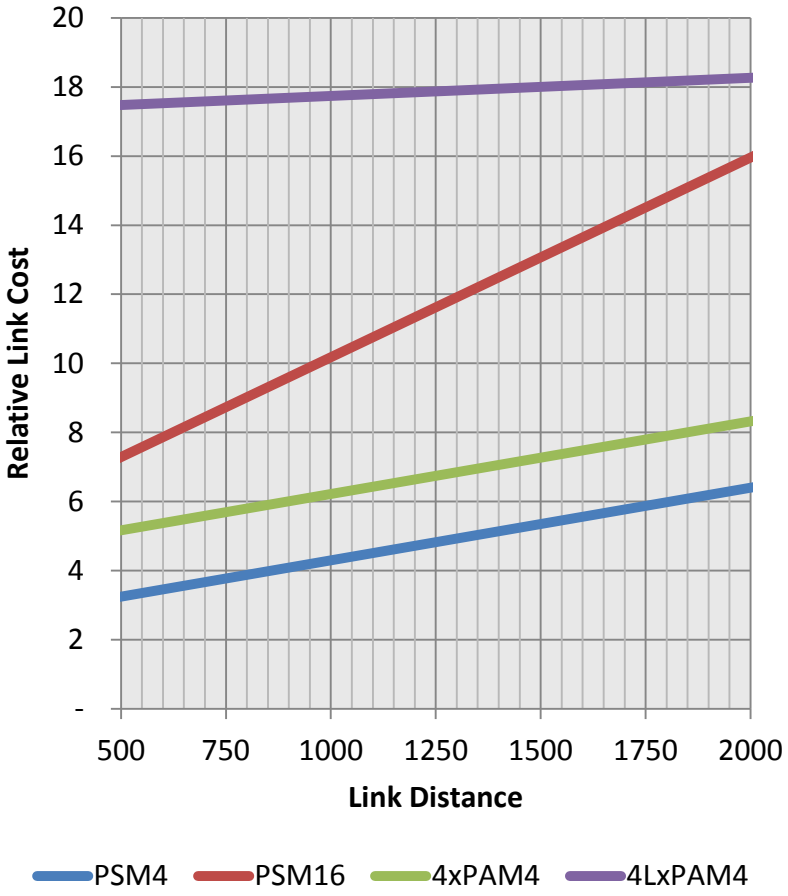


Second Generation

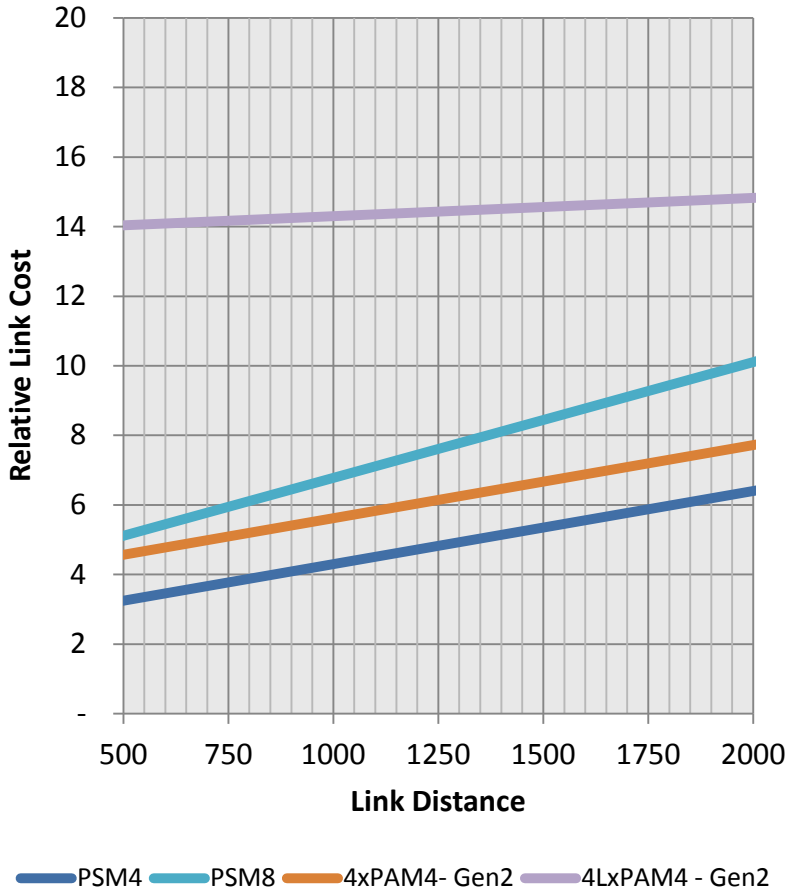


Link Costs – 500m to 2,000m

First Generation

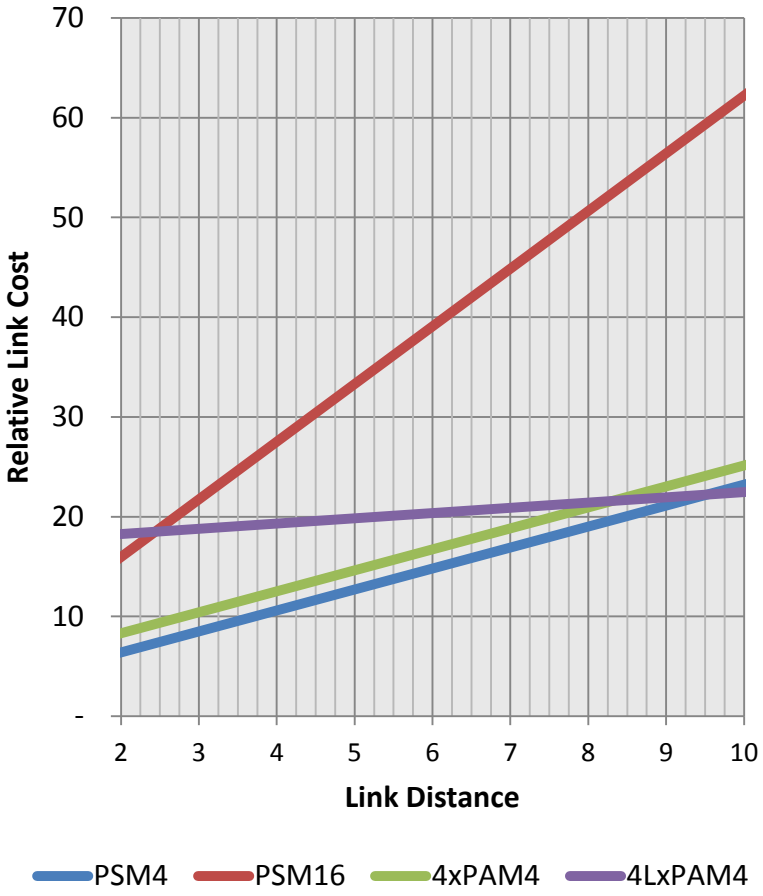


Second Generation

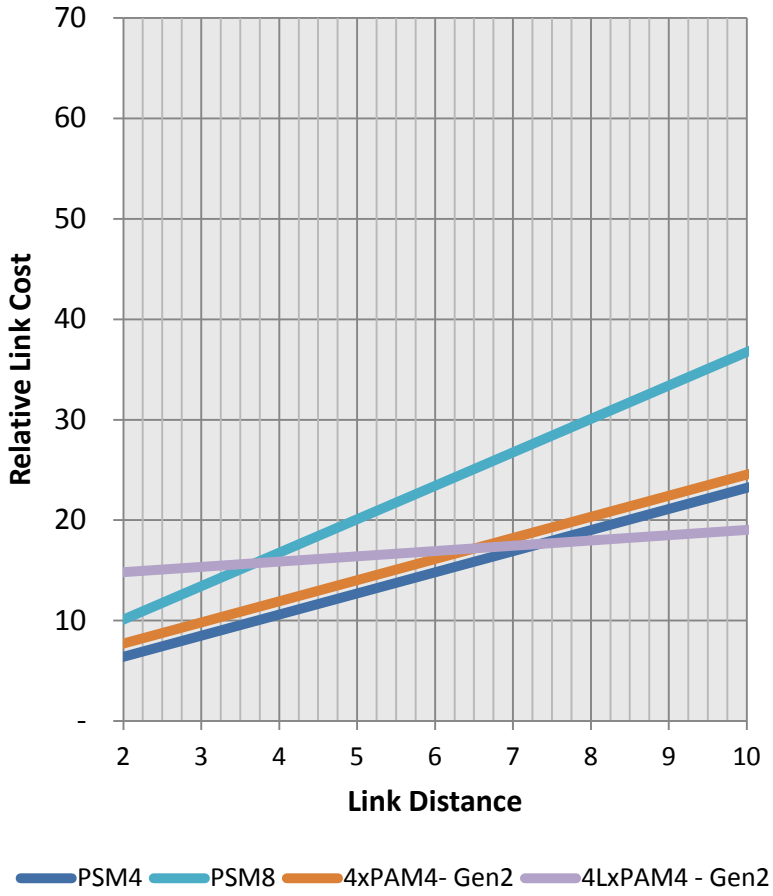


Link Costs – 2,000m to 10,000m

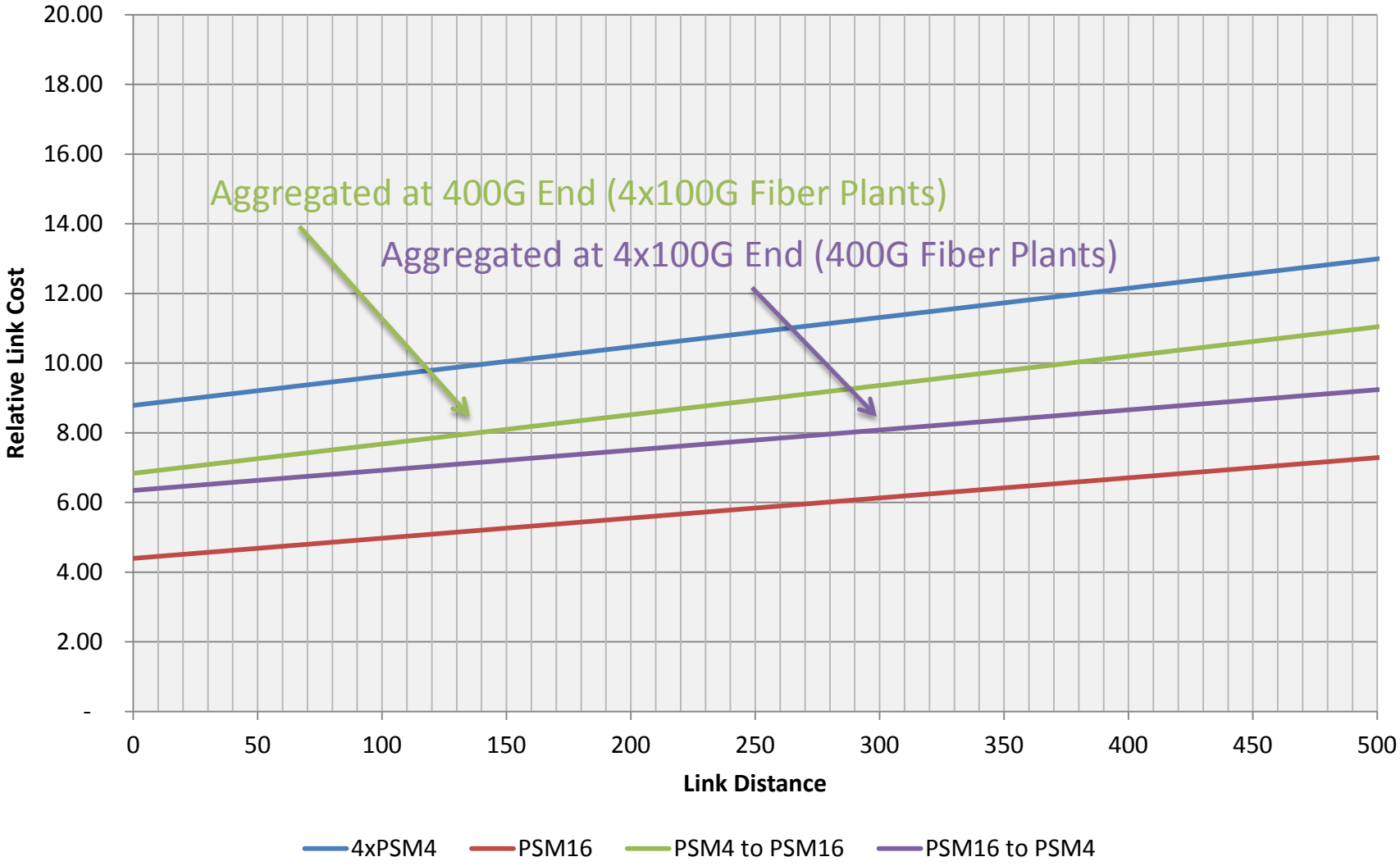
First Generation



Second Generation



Example: 400G to 4x100G Breakout Links



Other Costs and Considerations

Other Costs and Considerations

- Development Costs and Amortization
  - Some solutions may have higher development costs than others
  - Amortization of development costs can have a significant impact on product COGS
    - Especially at low volumes and/or slow deployment growth rates
- Time to Market
  - Differing levels of development complexity can lead to very different product availability dates
- Price elasticity of demand
  - Higher cost solutions can drive down volumes, begetting even further cost increases
- Availability of ports
  - Highest volume port type is typically that deployed for short reach interconnects
  - Enabling a common port for SMF interconnects can enable a larger TAM, subsequently attracting more investment in cost optimized solutions

Summary and Conclusions

Summary and Conclusions

- There are economically viable 400G solutions.
- Cost can be a strong function of objective definition
  - Objectives optimizing for 10km reaches unlikely to yield cost optimized solutions for sub 500m reaches.
- Parallel SMF will be vital to the 500m objectives and market.