

### Comment (#140, 412, #413, #414,#415, #416, #417):

1. TDL #275 and #276 D2.1 (comments: #108, #420, #421, #281 D2.2) was not fully implemented.
2. In addition, editor has noted that due to comment #452 D2.2 (removal of PPort\_PD) we can't use the term PPort\_PD. 33A.1 was written to address Type 1 PSE and PD. It is still relevant for Type 2 PSE. It was updated not to address Type 3 and Type 3 system therefore it should be limited for clause 33 only. As a result, Pport\_PD term can be use.
3. To move this material to clause 33 and file maintenance request.

### Proposed Remedy:

#### Make the following changes:

### PSE-PD stability

#### 33A.1 Recommended PSE design guidelines and test setup

In order to prevent potential oscillations between the PSE and PD, the sum of the PSE port output impedance ( $Z_{o\_pse}$ ), the cable impedance ( $Z_c$ ), the PD input port circuitry impedance ( $Z_{cir\_pd}$ ) and the PD EMI output filter impedance ( $Z_{emi}$ ) should be lower than the PD power supply input impedance ( $Z_{in\_ps\_pd}$ ). All the above impedances are converted to the equivalent series impedance form as described by Figure 33A-1.

PSE PI output impedance consists of two parts:

- PSE power supply output impedance ( $Z_{o\_ps}$ ), which is a function of the load at the PSE PI, and
- the series elements ( $Z_{ser}$ ) that connect the PSE power supply output to the PSE PI.

Therefore, the PSE PI output impedance during normal powering mode is  $Z_{o\_pse}=Z_{o\_ps}+Z_{ser}$ .

In order to maintain PSE-PD stability, the following guidelines apply:

- $Z_{o\_ps\ max} = 0.3\ \Omega$  at frequencies up to 100 kHz at the highest output power level that the PSE supports, as defined in Table ~~33-13~~33-7 At lower power  $P_{pse\_actual}$ ,  $Z_{out\_ps\_max} = 0.3\ \Omega \times P_{Class} / P_{pse\_actual}$ .  $P_{pse\_actual}$  is the actual power that the PSE support below PClass.  $Z_{o\_ps}$  can be extracted from  $Z_{o\_port}$  by measuring VPort\_PSE-2P/ IPort (with an external power dynamic analyzer system) as a function of frequency and subtracting from  $Z_{o\_port}$  the value of  ~~$Z_{ser}$~~  $Z_{o\_ser}$  which is limited by the value of  $Z_{o\_ser}$  at DC (low frequency).

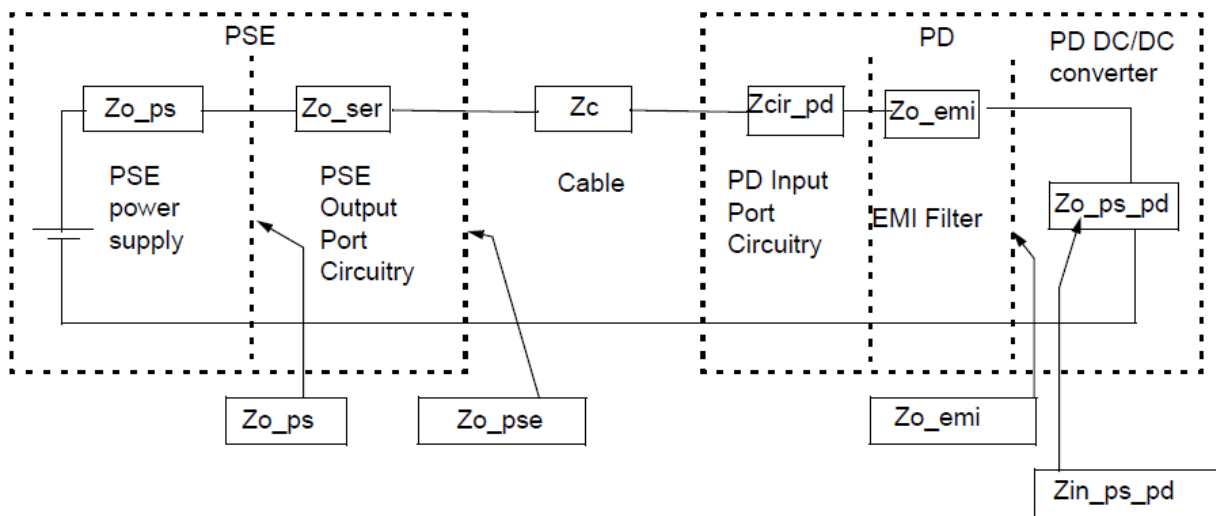
~~— If  $Z_{o\_ps} < Z_{o\_ser}$  and VPort 2P is kept to VPort 2P min and VPort 2P max as defined in Table 33-17 during dynamic load changes from 10 Hz to 100 kHz, then the value of  $Z_{o\_ps}$  is not limited.~~

- The value of  $Z_{o\_ps}$  is not limited if the following conditions are met simultaneously:

- 1)  $Z_{o\_ps} < Z_{o\_ser}$
- 2)  $V_{pse}$  is kept in the range of  $V_{Port\_PSE-2P}$  as defined in Table 33-17 33-11 during dynamic load changes from 10 Hz to 100 kHz.

Verification of these guidelines can be made by measuring the PSE PI output impedance from 10 Hz to 100 kHz at the highest output power level that the PSE supports, as defined in Table 33-7 with the maximum load per the PSEs assigned Class, as defined in Table 33-13 at short cable length, or by performing simulations.

See Figure 33A-1 for the PSE-PD system impedance allocation.



### 33A.2 Recommended PD design guidelines

PD PI input impedance consists of the following two parts:

- PD PI input circuits  $Z_{cir\_pd}$  and the EMI filter  $Z_{emi} Z_{o\_emi}$ ,
- PD power supply input impedance  $Z_{in\_ps\_pd}$ .

In order to maintain stability with the PSE, the PD power supply input impedance  $Z_{in\_ps\_pd}$  should be higher than the output impedance of the total network that precedes it ( $Z_{o\_emi} + Z_{cir\_pd} + Z_c + Z_{o\_pse}$ ).

The worst-case scenario is when the channel length is zero (in terms of lower damping factor).

Access to the PD input power supply is not possible through the PD port for evaluating the various impedances in the PD and derivation of the above individual impedances. The following guidelines are recommended when measuring the PD input impedance:

- The PD power supply input impedance ( $Z_{in\_ps\_pd}$ ) at  $P_{class\_PD}$   $P_{Class\_PD}$  as defined in Table 33-30 33-18 should be higher than 30  $\Omega$  at any frequency up to the PD power supply crossover closed loop

frequency. If the PD power supply is consuming less than  $P_{Class\_PD\_max}$ , -as defined in Table-~~33-~~  
~~3033-18~~ i.e.  $P_{pd\_actual}$ , then  $Z_{in\_ps\_pd\ min} = 30 \times \frac{P_{port\_PD\_max} - P_{Class\_PD}}{P_{port\_PD}}$ .  $P_{port\_PD}$  is  
the actual power consumed by the PD below  $P_{Class\_PD}$ .

~~Comment D2.2/#452 removed  $P_{port\_PD}$ . Replacing the above by  $P_{Class\_PD}$  would be incorrect.  
Solution needed.~~

— The PD power supply EMI filter output impedance should be  $Z_{o\_emi} = 2.7 \Omega$  max. If the PD power  
supply is consuming less than  $P_{Class\_PD}$ , then  $Z_{o\_emi} = 2.7 \times \frac{P_{port\_PD\_max} - P_{Class\_PD}}{P_{port\_PD}}$ .

See Figure 33A–1 for the PSE-PD system impedance allocation.

**End of Baseline**