PSE State Diagram, v3

Considerations for Staggered Power-on of Dual-Signature PDs

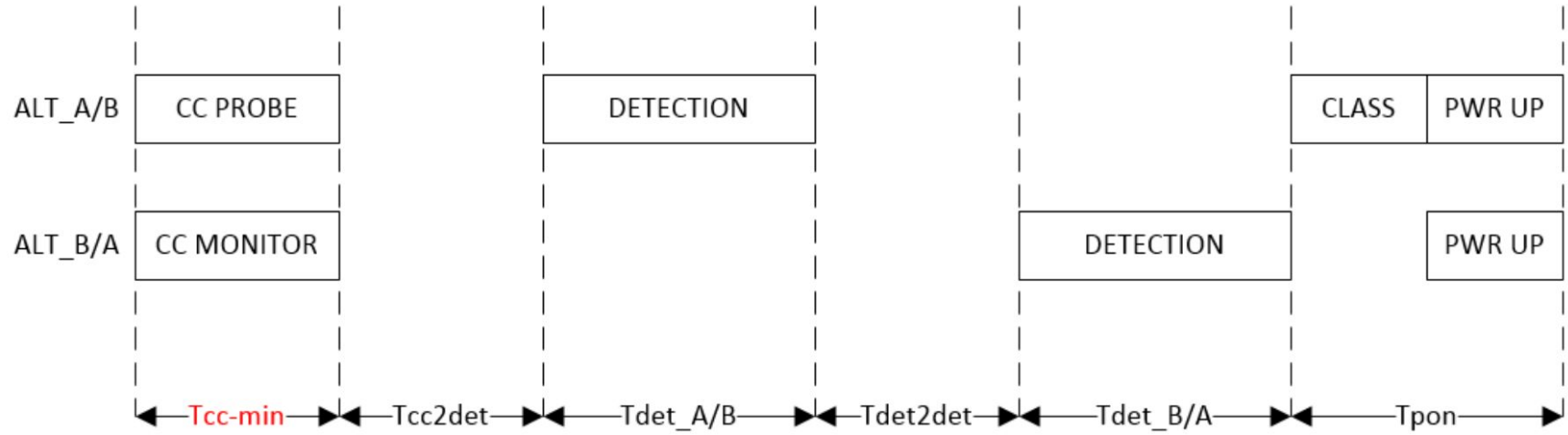
Proposal for Additional CC/Det/Cls Sequence

Sequence 3

Staggered Power-up of DS PDs

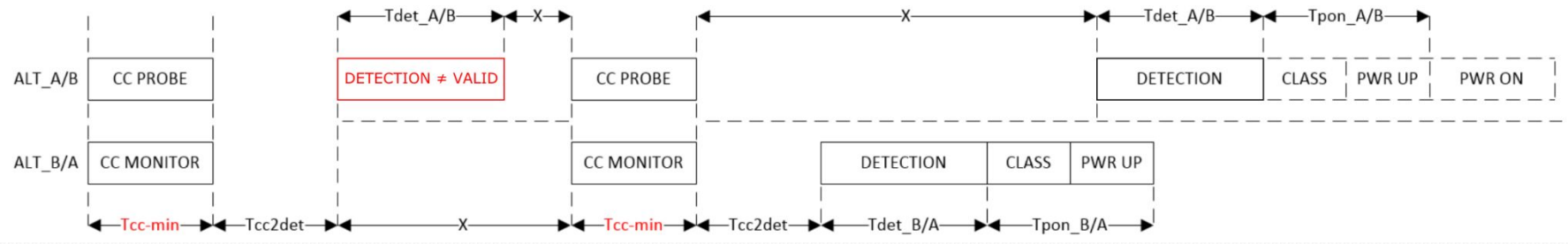
CC → Alt_A/B (→ CC) → Alt_B/A

CC → Alt_A/B → Alt_B/A (SS PDs)



- Tcc-min (>200ms) to circumvent cable-plug issue
- Sequence remains viable and most of the implementation details are left to the reader

CC → Alt_A/B (→ CC) → Alt_B/A (T1-T4 DS PD)



- Tcc-min (>200ms) to circumvent cable-plug issue
- Tcc2det ensures link remains inactive for no longer than 400ms
- Tcc2det, Tdet, Tpon are enforced for each pairset