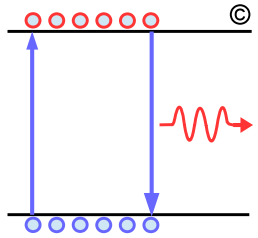

PCS and AUI Considerations for 50 GbE and NG 100 GbE

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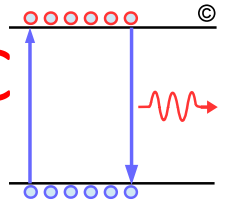
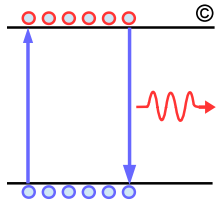
April 27, 2016

Compatibility, Synergy, and Interaction with FEC

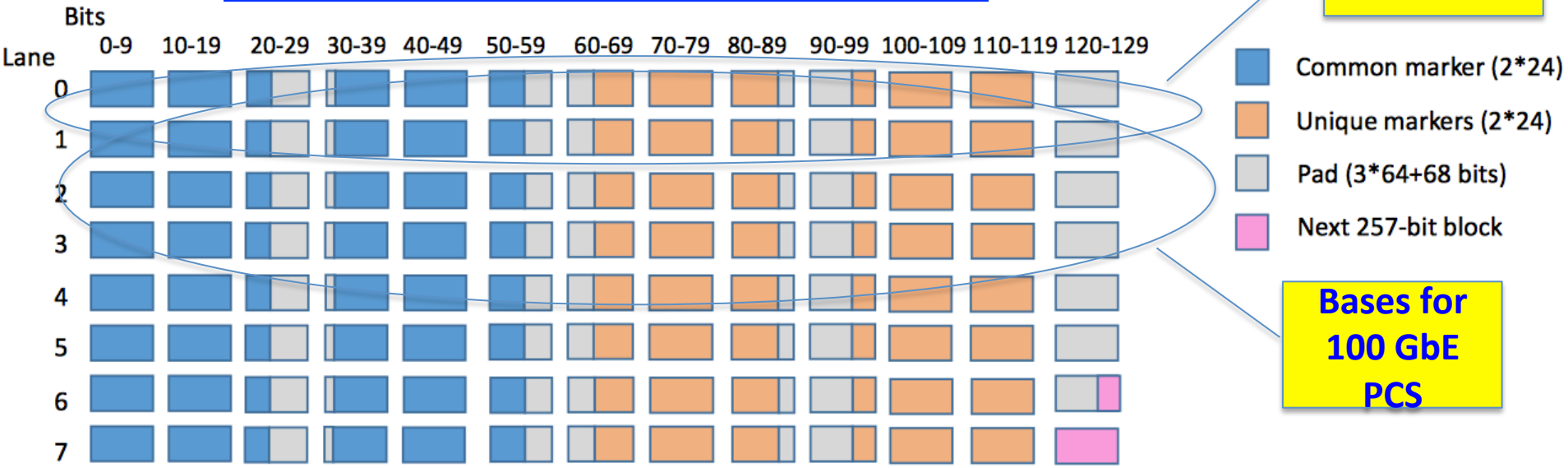


- **During the study group need to investigate ideally a common FEC addressing all 50 GbE PMDs with likely choices:**
  - RS-FEC (528,514)
  - RS-FEC (544,514)
- **During the study phase need to investigate if RS-FEC (528,514) can meet NGOATH 100 GbE PMDs requirements:**
  - If RS-FEC (528,514) can meet NG PMDs requirements preferable for backward compatibility otherwise KP4 should be considered
    - Legacy 100 GbE PMD use all of the KR4 FEC gain unless CAUI-2 can operate error free similar to CAUI-4 (1E-15) compatibility with legacy PMDs may not be feasible
- **50G/lane Cu and optical PMDs should drive the FEC choice and coding gain**
  - Bit mux would be preferable but may have a penalty under burst error
  - Symbol mux advantage is that data could come from two logical lanes without penalty
- **Transition to 50G/lane optics may happen faster than migration to ASICs with 50G IO**
  - 50 GbE or NG 100 GbE implementation may take advantage of 400 GbE hardware which supports 16x25G electrical but 50G/lane or 100G/lane optics
  - To support flexible migration the 50 GbE PCS and NG 100 GbE PCSs should support respectively 50AUI-2/1 and CAUI-4/2 PMAs
    - It assumed that 50GAUI-2 and CAUI-4 are based on 2 and 4 lanes NRZ respectively
    - It assumed that 50GAUI-1 and CAUI-2 are based on 2 and 4 lanes PAM4 respectively
- **Application overlay should be key consideration to allow building common ports supporting overlay/breakout ports**
  - 1x400GbE, 2x200GbE, 4x100GbE, 8x50GbE.

Option I: 50 GbE and NG 100GbE Base on Clean Sheet of Paper Based on 25G PCS Lane

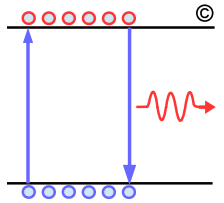


- **25G PCS lanes builds on synergy with 400 GbE PCS format**
  - http://www.ieee802.org/3/bs/public/adhoc/logic/feb9_16/gustlin_01_0216_logic.pdf



- 50 GbE can be based on 1x257b blocks, pad is filled with free running PRBS9
- 100 GbE can be based on 2x257b blocks, pad is filled with free running PRBS9
  - To provide backward compatibility with 100 GbE per CL82 require more complex PMA-PMA chip
- Implementation will support 50GAUI-2/1 and CAUI-4/2

Option IIA: 50 GbE and NG 100GbE Based on 5G PCS Lane



- **Per CL82 with 100GbE having 20 PCS lanes**
  - For 50 GbE use half number of PCS lanes as was proposed:
    - http://www.ieee802.org/3/50G/public/adhoc/archive/gustlin_020316_50GE_NGOATH_adhoc.pdf
  - May support 25 GbE MSA implementation with simpler PMA chip
  - Implementation will support 50GAUI-2/1 and CAUI-4/2
  - If RS-FEC (544,514) is required is there value to preserve 5G PCS lane over synergy with .bs PCS?

FEC Lane	Reed-Solomon symbol index (10 bit symbols 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33					
0	AM0 (0 … 63)	AM4	AM8	AM12	AM16	
1	AM0	AM5	AM9	AM13	AM16	
2	AM0	AM6	AM10	AM14	AM16	
3	AM0	AM7	AM11	AM15	AM16	

Bases for 50 GbE PCS With LAUI-2

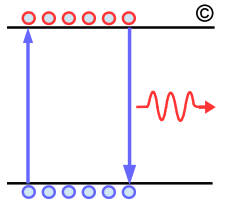
5b pad

Existing 100GbE FEC(528,514)

Bases for 100 GbE PCS with CAUI-2

FEC Lane	Reed-Solomon symbol index (10 bit symbols 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31 32 33 0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19 20 21 22 23 24 25 26 27 28 29 30 31									
0	AM0 (0 … 63)	AM0	AM4	AM6	AM8	AM10	AM12	AM14	AM16	AM18
1	AM0	AM0	AM5	AM7	AM9	AM11	AM13	AM15	AM17	AM19

Option IIB: Leverage CL82 PCS for 50 GbE with 4 PCS lanes and NG 100GbE Based on 20 PCS Lanes



- **Based on CL82 100 GbE lanes and 50 GbE based on speed up version of 40 GbE 10G PCS lane**

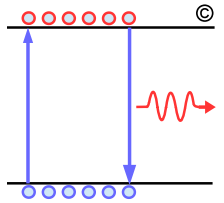
Table 82–3—40GBASE-R Alignment marker encodings

PCS lane number	Encoding[a] $\{M_0, M_1, M_2, BIP_3, M_4, M_5, M_6, BIP_7\}$
0	0x90, 0x76, 0x47, BIP_3, 0x6F, 0x89, 0xB8, BIP_7
1	0xF0, 0xC4, 0xE6, BIP_3, 0x0F, 0x3B, 0x19, BIP_7
2	0xC5, 0x65, 0x9B, BIP_3, 0x3A, 0x9A, 0x64, BIP_7
3	0xA2, 0x79, 0x3D, BIP_3, 0x5D, 0x86, 0xC2, BIP_7

[a]Each octet is transmitted LSB to MSB.

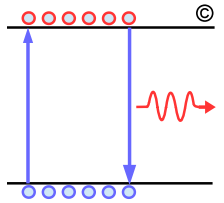
  - 50 GbE based on CL82 speed up 10G (12.5G) PCS lanes and could be made compatible with the 25 GbE MSA implementation of 50 GbE based on two lanes
  - Implementation will support 50GAUI-2/1
  - PMD under consideration should determine if KR4 FEC is sufficient otherwise KP4 FEC
  - Options for forming the FEC lanes
    - If KR4 FEC sufficient then FEC lanes could be formed by bit/symbol mux of 2 lanes 50 GbE MSA
    - If KP4 FEC is necessary then FEC gets bolted on top of 2 lanes 50 GbE MSA PCS bit/symbol mux to be determined based on FEC study.

Option III: Possible 50 and 100 GbE PCS Format

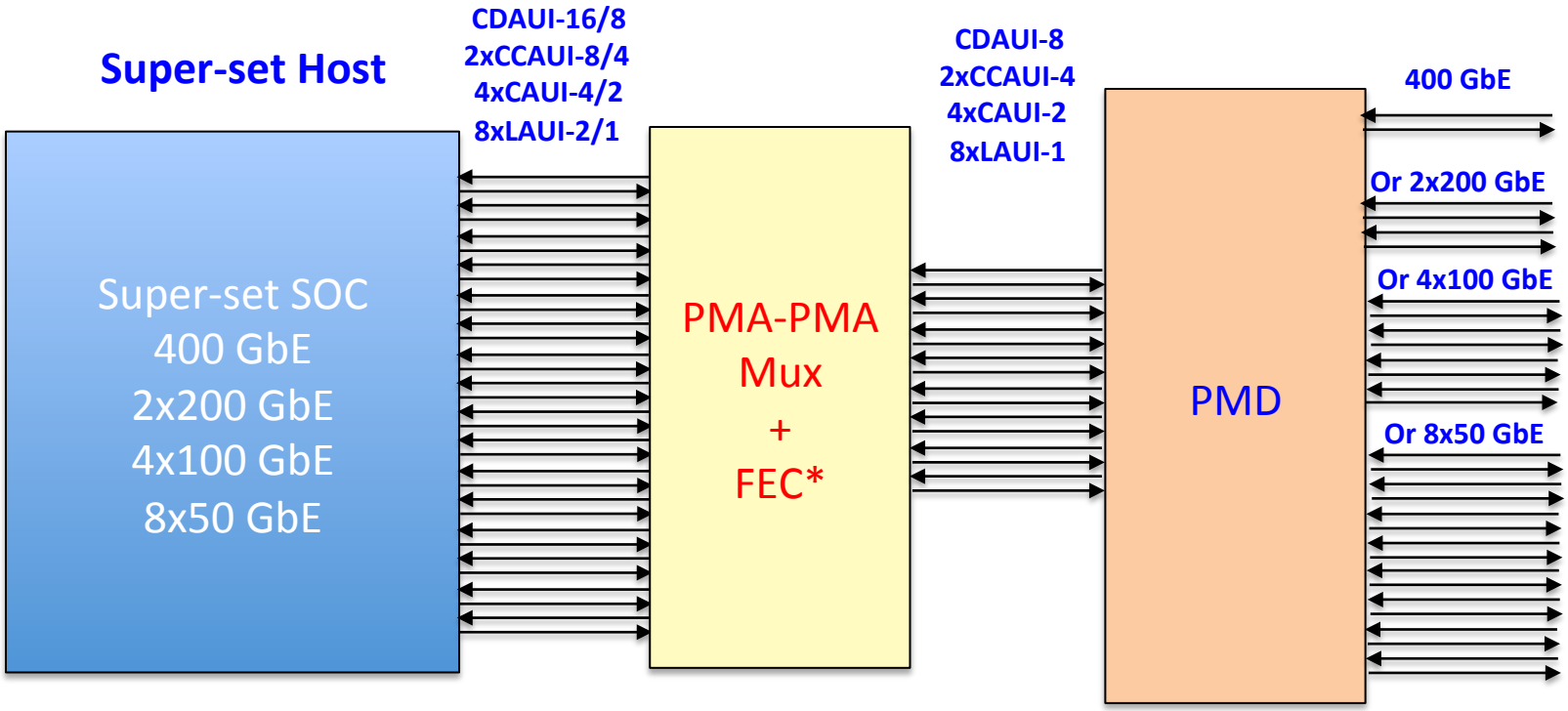


- **Follow CL49 10GBase-R PCS without any AM**
  - No clear advantage
  - No synergy with 100GbE, 200GbE, 400 GbE
  - Will only support CAUI-1 where there is no PMD objective for it
  - Will not support LAUI-2
- **CL49 does not offer viable PCS solution!**

Application Overlay

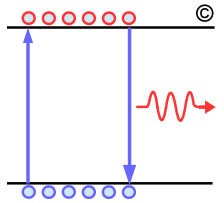


- **A key consideration of the 50 GbE and NG 100 GbE is application overlay with 200 GbE/400 GbE in support of break out from common port**
  - Supporting both 50GAUI-2/1 is required for 50 GbE application overlay
    - CAUI-4 already exist
  - 25G/lane early implementation as well as providing transition for 50 GbE MSA and 100 GbE.

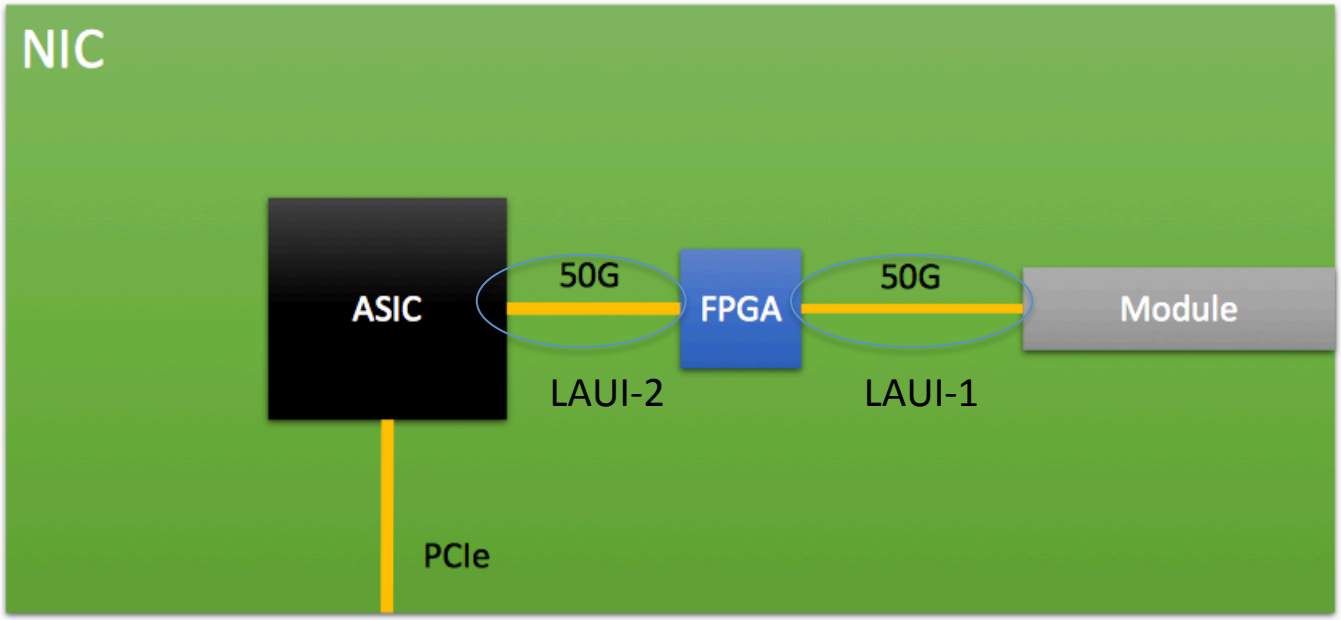


* In some implementation FEC may be part of the PMA-PMA otherwise in the super-set host.

Example NIC/NPU with No Immediate Benefit from 50G I/O

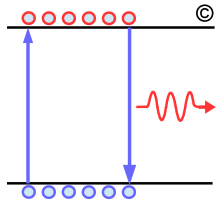


- **50G I/O does not offer benefit in low port count applications**
  - Limited availability of 50G SerDes can be costly and/or not available
  - The ASIC may already have 50 GbE based on two lanes MSA
  - Not having the option of 50GAUI-2 may force a new ASIC development with costly 50G SerDes
  - The standard should offer flexibility and choice to either use 50GAUI-2 or 50GAUI-1.



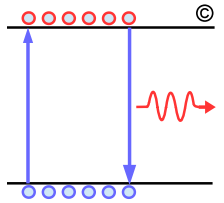
http://www.ieee802.org/3/50G/public/Mar16/booth_50GE_NGOATH_01a_0316.pdf

Why 50GAUI-2 Is Needed



- **25 GbE 1st task force meeting was Jan 2015 where products (switches, NIC, Phys, CFP2, CFP4, and QSFP28) already available in the market place based on 25G/lane**
  - 25GbE was based on the definition of the 25G MSA which happened to leverage CL49 instead of the MLD PCS
- **Today the maturity of the 50G/lane IO is not at the same level as 25G IO was 2014/2015 time frame**
- **Following class of product do not benefit from migration to 50G/lane IO**
  - Core limited
  - NIC/NPU applications with just a few ports
- **Unless application can benefit from 50G not having the option of the 50GAUI-2 forces the eco-system to higher risk and cost 50G IO over commodity 25G IO!**

Summary



- **PCS/FEC options for 50 GbE**
  - Clean sheet of paper based on 25G PCS lane is forward compatible with 400 GbE
  - Speed up CL82 with 4 PCS lanes (12.5G) offers backward compatible 50 GbE MSA
  - Either of the above options supports 50GAUI-2/50GAUI-1
  - Both RS-FEC(528,514) and (544,514) need to be further studied in conjunction with baseline PMDs under consideration
- **PCS/FEC options for NG 100 GbE**
  - Ease of full backward compatibility should not come at expense of sacrificing NG 100 GbE PMD performance as the backward compatibility can always be solved with the PMA-PMA device
  - Clean sheet of paper assumes 25G PCS lane forward compatible with 400 GbE
  - Use CL82 100GbE PCS base on 5G PCS lane offering backward compatibility
  - Either of the above options supports CAUI-4/CAUI-2
  - Both RS-FEC(528,514) and (544,514) need to be further studied in conjunction with baseline PMDs under consideration
- **With 50 GbE MSA and 100 GbE already existing in the market place ease of backward compatibility offers greater value than forward compatibility to 400 GbE.**