COMPATIBILITY CONSIDERATIONS FOR 50 AND 100G

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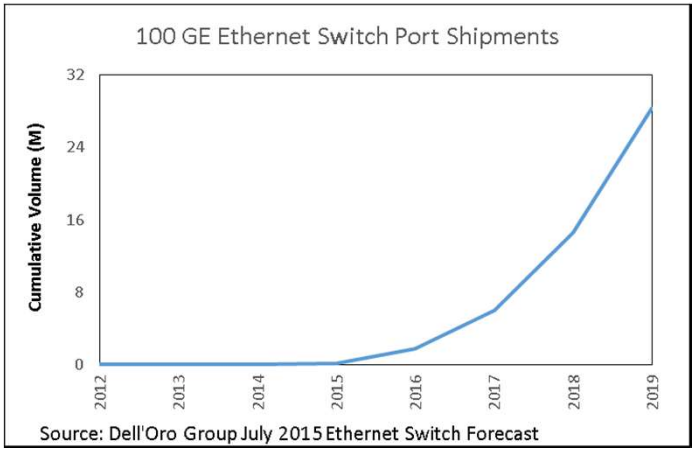
MARKET NEED

- **Both 100GE and 50GEc are existing MAC rates**
- **There will be a large and growing installed base of 100GE (~ 16M in 2018)**
  - Data applies to 4 x 25 G interfaces used in switch applications
  - [These ports can typically be configured as 4 x 25GE, or 2 x 50GEc also]



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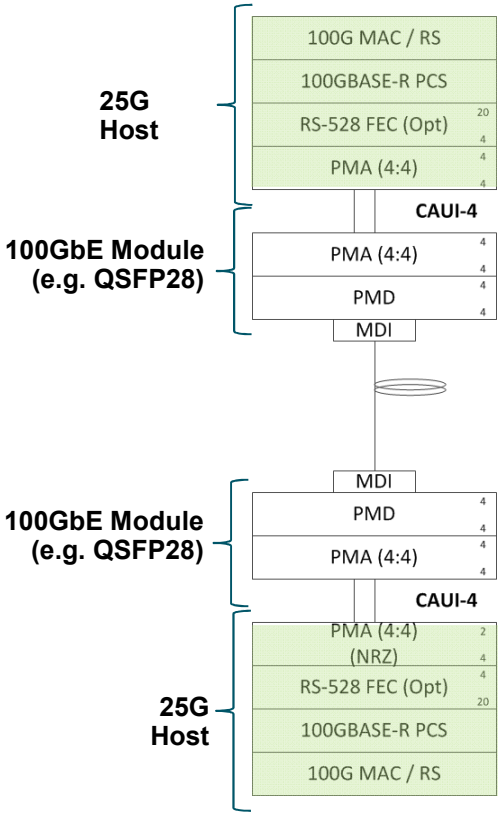
- **Do we need to make consideration in 50 / NOGOATH for connection of new 50G based PMDs to these "legacy" 100 & 50G ports?**

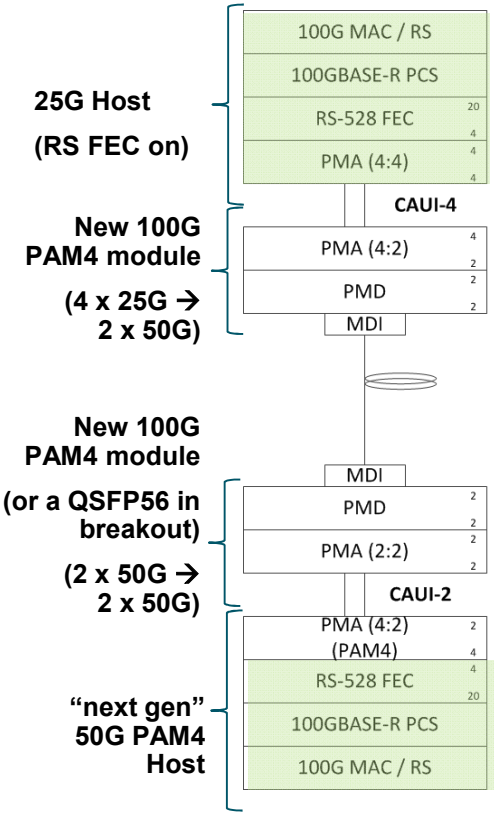
POSSIBLE GOALS FOR NEXT SET OF 50G PCS & PMDS

- **An architecture which permits straightforward connection of 50G / lane capable hosts to existing devices / technologies –**
  - 100GBASE-R4 PHYs
  - 50GEc (2 x 25G) PHYs – (non-IEEE variant - 25 / 50G Consortium Specification)
- **Offer low power and low latency where possible**
- **Cost optimized**
  - Permits legacy designs to take advantage of new 50G based PMDs
  - Use appropriate FEC where possible to ease implementation challenges (applies to both optics and electrical PMDs)
- **Consider re-use where practical of existing work / developed IP**
  - FEC
  - MACs
  - PMAs
  - Modules / management interfaces

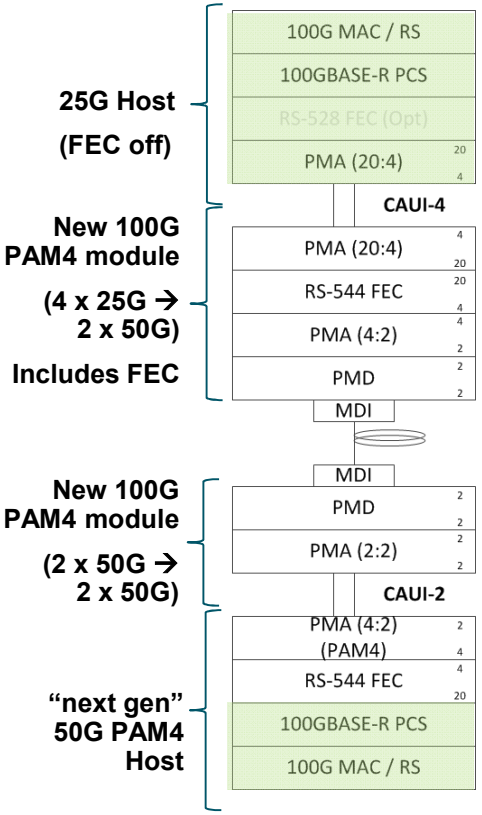
100GBE ARCHITECTURE EXAMPLES:



Existing 100GBASE-R4 (Today)



End – end RS-528 FEC (option a)

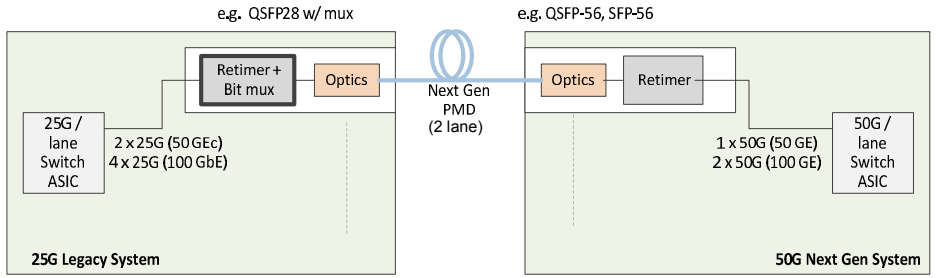


PMD protected RS-544 FEC (option b)

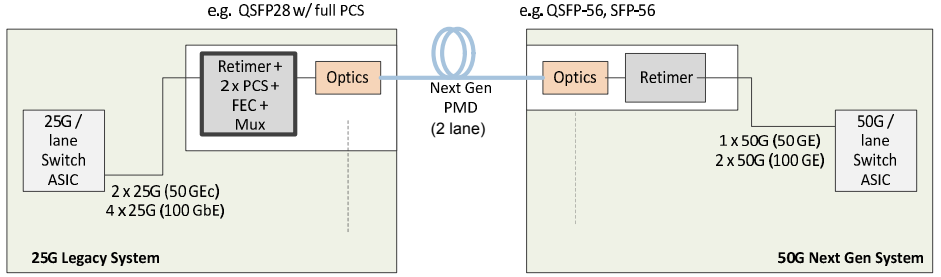
Existing in 100GBASE-R4 logic

OBSERVATIONS (100G)

- **The most simple architecture relies on end-end FEC borrowed from 100GBASE-R4 (option a)**
  - This enables an QSFP28 with a simple PMA mux (4 x 25G → 2 x 50G lanes) – no change to CAUI-4 spec, or module mangement
  - Initially looks attractive for module applications due to low power and cost adder
  - Would enable plug and play upgrade to 100G over 2 lane PMD with *no hardware change on legacy designs*
  - Open question – does RS-528 provide adequate end – end gain for the 50G based PMDs and AUI?
  - Cons: no passive copper support, as requires the mux function in the module



- **One alternative is to add RS-544 FEC with appropriate PMAs to Module PHY or Gearbox on PCB (option b)**
  - Drawback for Module: Power envelope, BOM cost adder
  - Drawback for PCB: No longer a legacy hardware design
  - Drawback for management – SFF 8636 update / management for full PCS / FEC (would be required to be managed over I2C, or transition to MDIO and use CL45)



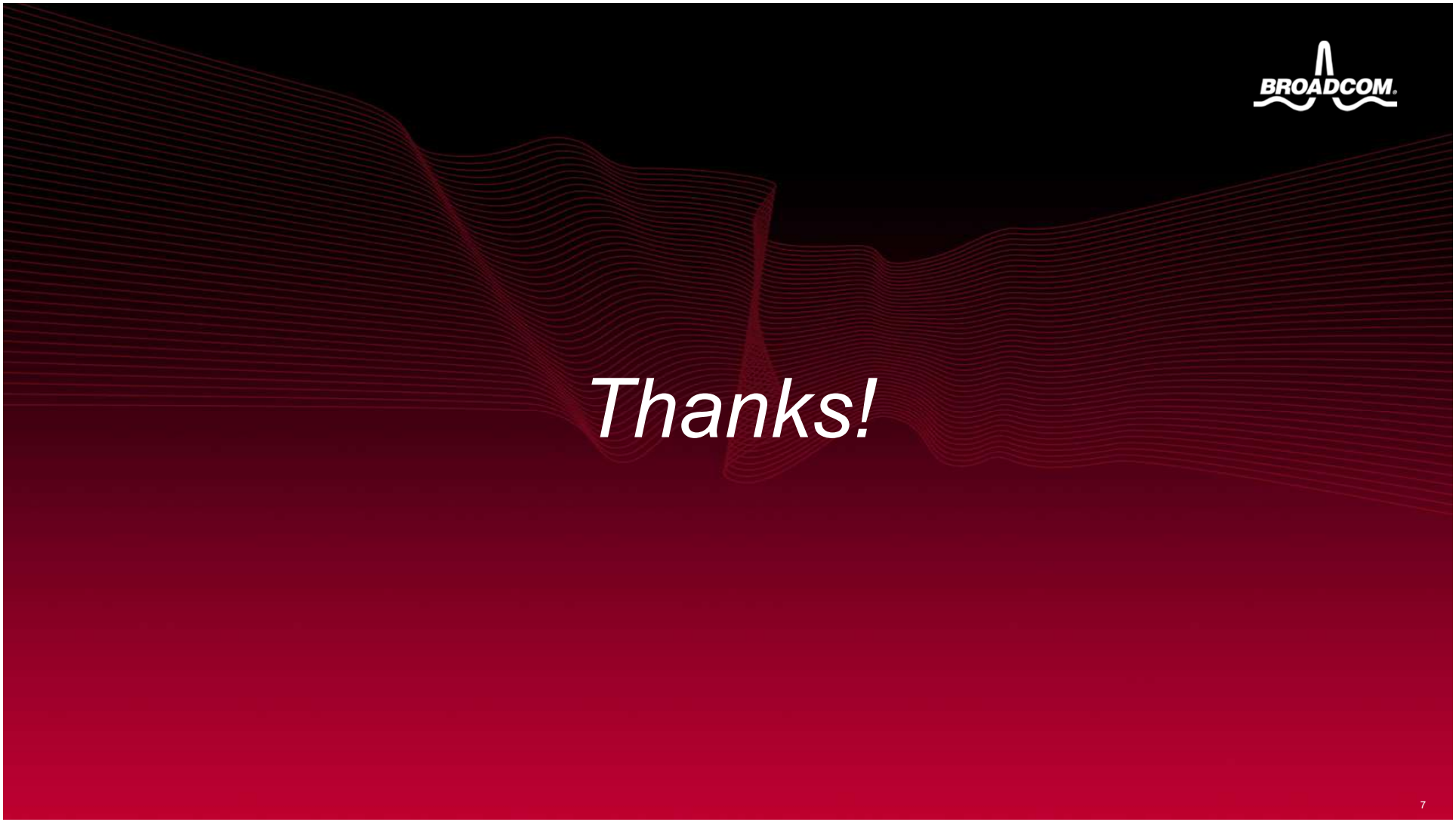
- **"Do nothing" alternative is to not make allowance for backwards compatibility**
  - Force 50G next gen designs to run in 25G "down speed" mode to connect to legacy
  - Increases lane use by x 2 on next gen silicon, reduces switch radix which is undesirable

FOR DISCUSSION

- **For 50 GbE and 100 GbE, should we consider an architecture which enables optional connection to existing 50 and 100GbE hosts based on 25G lane rate technology?**

- **Simplest architecture (option a) would put a bit-mux in the module CDR, and requires that the AUI / PMD is protected with the existing end – end RS-528 FEC**
  - Is this adequate FEC gain for a subset of candidate PMDs?

- **Alternative view: Make no consideration for backwards compatibility with existing PHYs in 50G / NGOATH**
  - e.g. require a 200GBASE-R4 port be operated down-speed at 100GBASE-R4 to connect to legacy 25G silicon
  - Drawback: this mode handicaps the 50G host by requiring a down-speed of the AUI to 25G, with associated loss in radix / IO capacity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Thanks!