

# **Backwards Compatibility Considerations for 50 and 100G – Revisited**

NGOATH Ad-hoc Study Group 2/17/16

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# AUI & FEC Potential Combinations

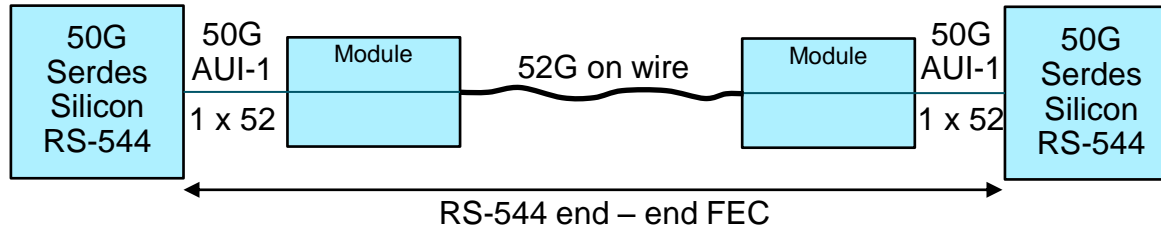
Port Speed	AUI exists today?	FEC exists today?	Combination exists today?	Comment
100G	4 x 25G	RS-528	Yes	<b>Existing 802.3bm</b>
	4 x 26G	RS-544	No	Typically RS-544 is only implemented with a PAM4 capable serdes for backplane, not AUI
	4 x 25G	Other	No	
	2 x 51G	RS-528	No	
	2 x 53G	RS-544	No	
	2 x 51G	Other	No	
50G	2 x 25G	RS-528	Yes	<b>Existing 50Gc</b>
	2 x 26G	RS-544	No	Typically RS-544 is only implemented with a PAM4 capable serdes, for backplane not AUI
	2 x 25G	Other	No	
	1 x 51G	RS-528	No	
	1 x 53G	RS-544	No	
	1 x 51G	Other	No	

streamlined backwards compatibility desired with these ports

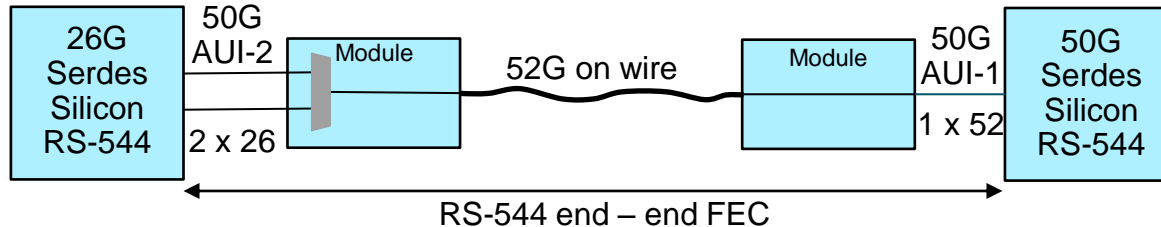
implemented or defined today
not implemented today (blue is new!)
typically not commonly implemented today

# Green Field Cases Being Discussed (all new silicon and hosts)

## Green Field Case 1:



## Green Field Case 2:



## Goals:

- Optimal PMD design, leverage FEC
- Architectural Commonality with 802.3bs
- Optimal PMD design, leverage FEC (maybe at reduced gain / burst error protection)
- Enable *new* 25G Host to communicate with 50G Host, w/ 50G based PMD

- Neither of these cases addresses legacy backwards connectivity, as the host silicon is all new
- Questionable whether Case 2 has BMP (does nothing to improve IO density, latency, or backwards compatibility with existing PHYs)
- (not shown: Case 2 connected to 2 x 26G on wire – similar solution already exists in market, no unique identity / BMP)

Note: 50GE cases taken for simplicity, applies to 100GE as well

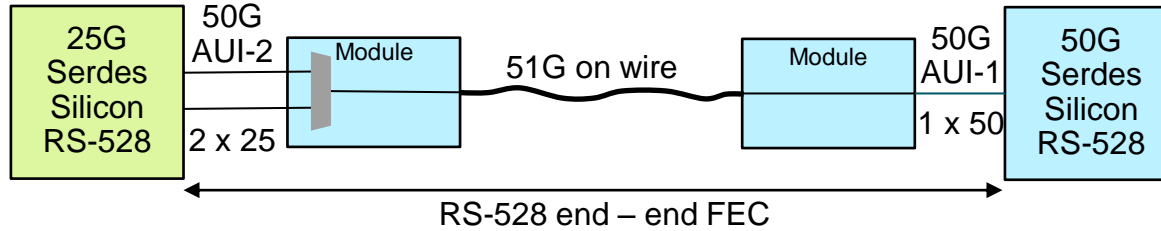
# Backwards Compatibility Cases (at least one “legacy” host / silicon)

Goals:

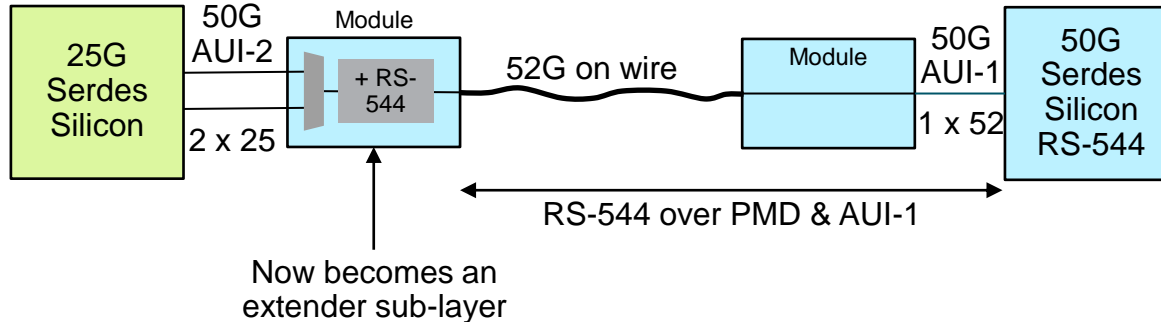
- Enable Legacy host to communicate with new 50G capable host
- Introduces an “adapter” module with 2:1 bit mux
- Impacts PMD choice due to lower performance FEC

- Enable Legacy host to communicate with new 50G capable host
- Introduces an “adapter” module with 2:1 bit mux and FEC
- No limitations on PMD choice due to FEC
- Requires module and host support for FEC extender sub-layer

**Brown Field Option A:**



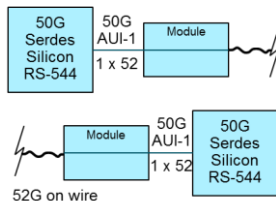
**Brown Field Option B:**



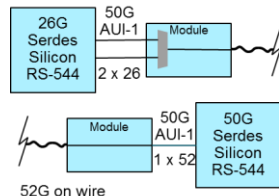
*Note: 50GE cases taken for simplicity, applies to 100GE as well*

# Summary

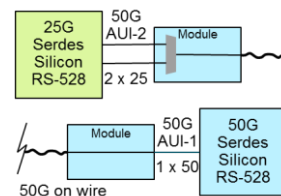
## Greenfield Case 1 (50G AUI-1 hosts, RS-544 end – end)



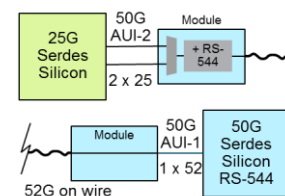
## Greenfield Case 2 (50G AUI-2 Host to AUI-1 Host RS-544 end – end)



## Brownfield Option A (2 x 25G AUI Host, RS- 528 end – end)



## Brownfield Option B (2 x 25G AUI Host, RS- 544 in module, over PMD and 50G AUI)



compatible with existing silicon / standards*	No	No	Yes	Yes
Uses existing host management software	N/A	N/A	Yes	No, due to extender sub-layer
maximizes PMD reach / FEC leverage	Yes	Yes	No	Yes
Commonality with 802.3bs PCS	Yes	Yes	No	Yes
Maximizes new host IO density	Yes	Yes	Yes	Yes
Latency / Power	?	?	?	?

\*With appropriate adapter module if needed

# Proposed Objectives [& Commentary]

- **Support optional single and two lane 50 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications**
  - [i.e. 50GAUI-1 & 50GAUI-2]
- **Support optional two lane 100 Gb/s Attachment Unit Interfaces for chip-to-chip and chip-to-module applications**
  - [i.e. CAUI-2]
- **Provide appropriate support for PCS backwards compatibility with existing CAUI-4 chip-to-module and chip-to-chip interfaces**
  - [Leaving this with some leeway for interpretation, but in essence support for one or both the brownfield options for 100G]
- **Provide appropriate support for PCS backwards compatibility with existing 2 x 25G PCS chip-to-module and chip-to-chip interfaces**
  - [same as previous bullet, but for 50G]



Thanks!