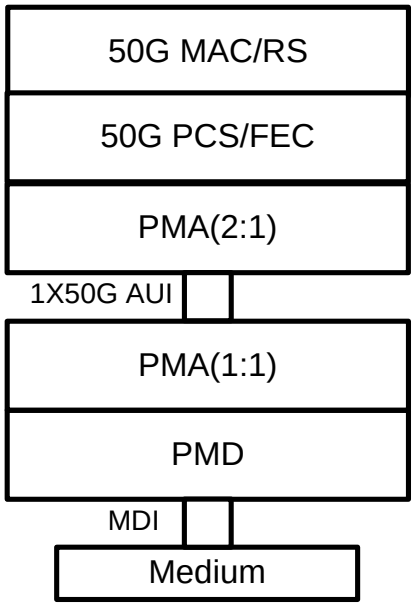
Options of PCS Lane Rate in 50/NG 100GbE

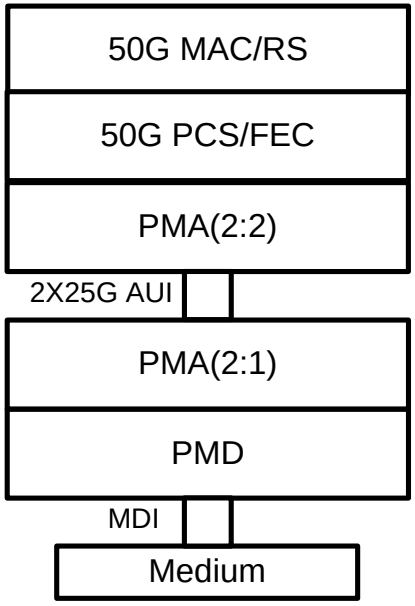
Tongtong Wang, Xinyuan Wang

Motivation

- Per discussion in 50G & NGOATH project, PCS architecture based on 25G or 50G PCS lane are considered.
  - For 200GbE in “gustlin_50GE_NGOATH_01_0116”:
    - Supports 8/4 lanes (25G and 50G)
  - For NG 100GbE in “gustlin_020316_50GE_NGOATH_adhoc”:
    - Based on 50Gb/s per lane signaling
  - For 50GbE in “gustlin_50GE_NGOATH_02_0116”:
    - Single lane PCS with existing RSFEC or RSFEC Interleaving
  - For 50/NG100/200GbE in “wang_50GE_NGOATH_01_0116”:
    - 25Gbps Per PCS lane
- This presentation gives more comparison between architectures based on 25G PCS lane and 50G PCS lane.

50GbE PCS Architecture w/ 25G PCS Lanes





- Pros
  - Enable 25G SerDes and 50G SerDes, expand the broad market potential of 50GbE by including two generations of SerDes technology and broader ASIC implementation space
  - Early 50GbE product can start with 2X25Gbps electrical interface and 50Gbps single lane PMDs.

- Risks
  - Need to consider 2:1 mux/de-mux scheme and its penalty.
    - Bit mux vs. Symbol mux
  - Or choose different PMA scheme for different PMDs?
    - Protocol aware symbol mux for backplane
    - Blind bit mux for pluggable modules (Coaxial and optical PMDs)

PMA: 2:1 Symbol Mux VS Bit Mux

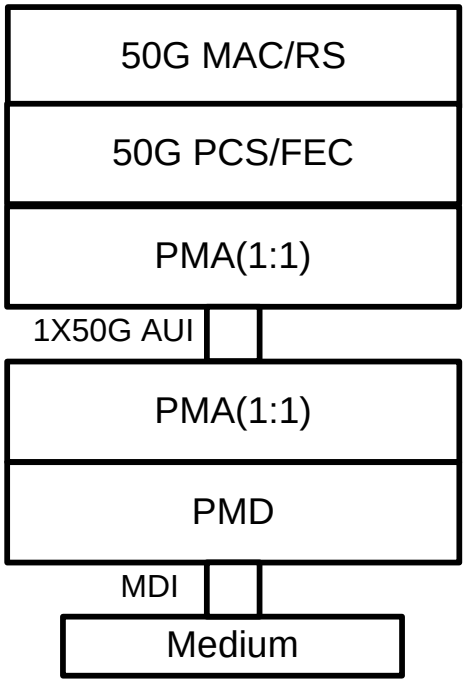
- Revisit multiplexing scheme and performance discussion in .bs project, option1 and option 2 in anslow_01_0815_logic and wang_x_3bs_01_0915 are corresponding to bit mux and symbol mux in 50GbE/NGOATH.
- Calculation result shows that FEC performance in these options are worse than 2-way interleaving, in exchange for shorter latency.

	At slicer output for FLR = 6.2E-11			
	Total electrical		Optical	
Same cwd (1), a = 0.75	Burst	2.9E-7*	Random	2.4E-4
Same cwd, symbol interleave (2), a = 0.75	Burst	7.5E-7*	Random	2.4E-4

Refer to anslow_01_0815_logic

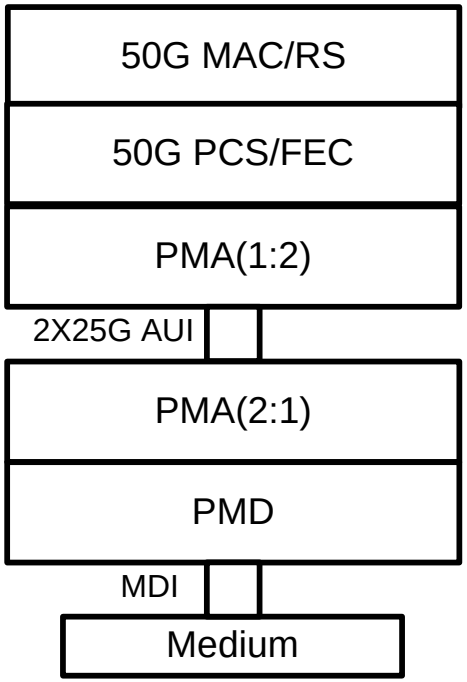
- Using symbol mux can get slightly better BER requirement than blind bit mux, however, both options can not meet 1E-6 BER requirement.
  - *This table is for 1e-13 BER objective, while 50G has 1e-12 BER objective.*
- More investigation is needed to mitigate these options.
  - How to reduce burst errors probabilities?
  - And what is the restrictions on applications with these measures?

50GbE PCS Architecture w/ 50G PCS Lane



- Pros
  - Easy to do symbol mux on PCS Lane;
    - Still need to limit burst errors to meet 1E-6 BER requirement on 1X50G Electrical interface
- Cons
  - No direct support for 25G SerDes;
    - Use inverse bit mux(see next slide)
  - More complexity in 50G/100G/200G/400GbE combo implementation due to heterogeneous PCS architectures

50GbE PCS Architecture w/ 50G PCS Lane (Cont'd)



- Using inverse bit mux to support 25G SerDes
  - No mature application in recent 802.3 PCS architectures
  - Need protocol aware to recover symbol boundary on 50G single lanes of PMDs

50G/NG 100GE PCS Architecture

- Either use 802.3bj similar PCS architecture or 802.3bs similar PCS architecture, without 2-way interleaving
  - Same issue about 2:1 mux/de-mux scheme and FEC performance penalty exists while using 25G SerDes electrical interface
  - Also Need to consider limitation of burst errors to enable 50G SerDes electrical interface

- 2-way interleaving for 50/NG 100GbE applications?
  - It can improve FEC performance as in 802.3bs project
  - For NG100GbE, additional ~51.2ns by interleaving, total FEC latency will be ~160ns by conservative estimation, comparing to ~112ns without interleave. Is this latency acceptable in NG100GbE?
  - For 50GbE, additional ~100ns by interleaving, total FEC latency will be ~290ns by conservative estimation, comparing to ~190ns without interleave. Is this latency acceptable in 50GbE?
  - Or we can endure more area cost, increase logic parallelism to further reduce the latency introduced by interleave.

Further Analysis for 50G & NGOATH PCS Architecture with 25G/50G PCS lane

- Need to know BER information on new PMDs and their corresponding FEC coding gain requirement.

- How to compensate FEC performance degrade concern by 2:1 sym mux or bit mux?
  - Limited DFE tap coefficient
  - Limited non-liner influence as in discussed in wang_x_3bs_01_0715
  - Leave enough margin to endure burst error impact
  - Possibility of 2-way FEC interleaving as in 802.3bs

Summary

- From broad market potential perspective of 50/NG100GbE standard and product , prefer to support 25Gbps PCS lanes
- Comprehensive work on different technical approaches to reduce burst error probabilities and thus enable 25G/50G SerDes with RS(544,514) FEC
- Update value for 1e-12 BER objective

Thank You