802.3bz Layers – CL45 Management Proposal

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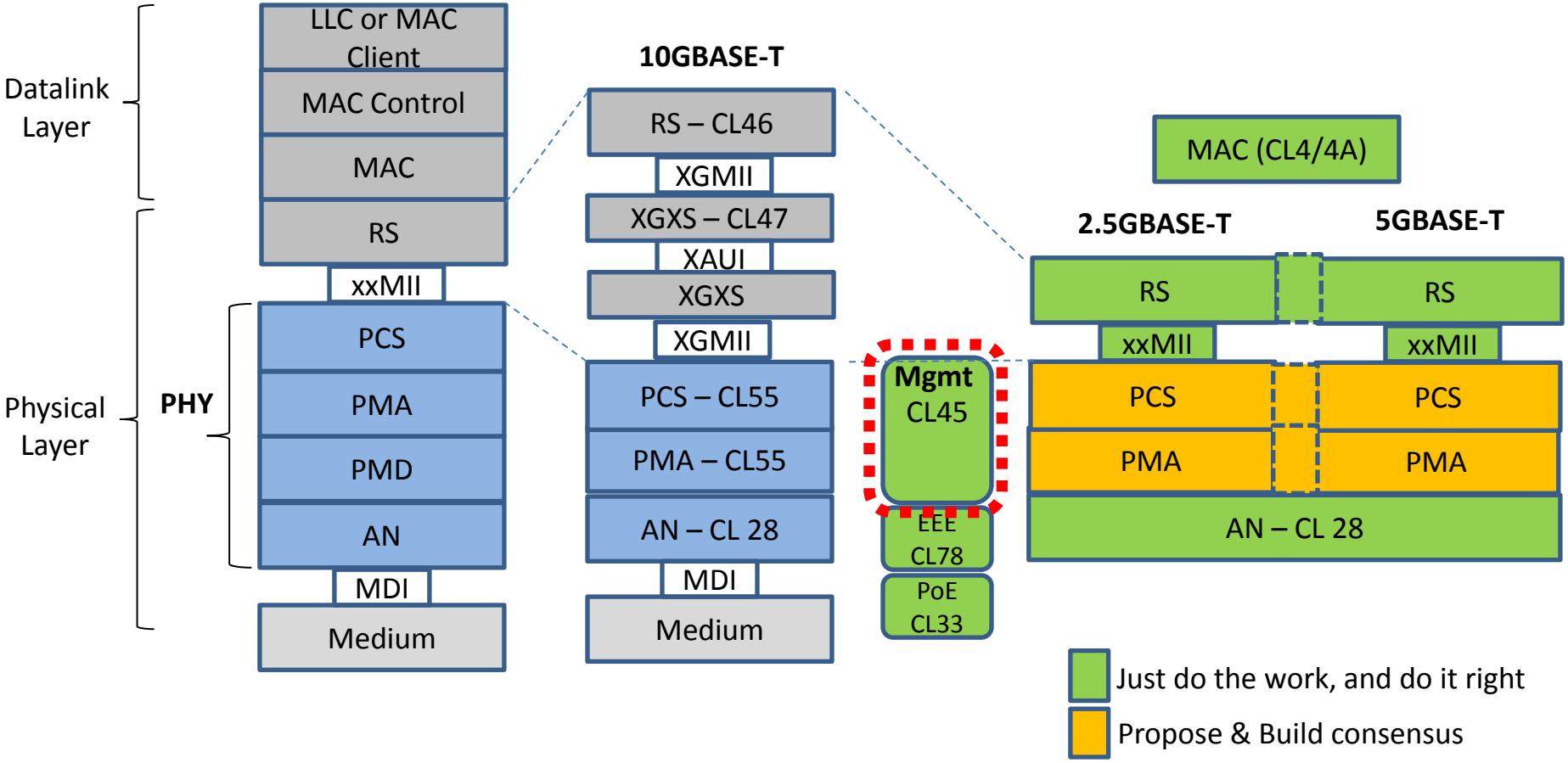
Requesting for your feedback.

on little ticket items.

Management & Statistics

2.5G and 5G BASE-T Layering considerations



CL45 MANAGEMENT PROPOSED CHANGES

&

PREPARED TO BE "BORED" – STRAIGHT FORWARD ADDITIONS AND CHANGES

Notes: References to 40GBASE-T are based on D2.0
References to 25G are based on .3by D1.0, .3bn also in blue.
.3bv (plastic), .3bs (400G) no draft yet, so no assignment collision.
"Notes" in following slides are feedback to .3bq and .3by. Not .3bz.
"Little Ticket"s sticky added to show new register to be defined. Like this ➔

Little Ticket Item
Need new Reg

MDIO REGISTERS – CL45.2

CL45 Table 45-3 – PMA/PMD Registers (Page 33)

Register address	Register name	Subclause
1.129	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T status	45.2.1.62
1.130	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T pair swap and polarity	45.2.1.63
1.131	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T TX power backoff and PHY short reach setting	45.2.1.64
1.132	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T test mode	45.2.1.65
1.133	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T SNR operating margin channel A	45.2.1.66
1.134	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T SNR operating margin channel B	45.2.1.67
1.135	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T SNR operating margin channel C	45.2.1.68
1.136	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T SNR operating margin channel D	45.2.1.69
1.137	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T minimum margin channel A	45.2.1.70
1.138	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T minimum margin channel B	45.2.1.71
1.139	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T minimum margin channel C	45.2.1.72
1.140	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T minimum margin channel D	45.2.1.73
1.141	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T RX signal power channel A	45.2.1.74
1.142	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T RX signal power channel B	45.2.1.75
1.143	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T RX signal power channel C	45.2.1.76
1.144	10GBASE-T/40GBASE-T/25/5/2.5GBASE-TRX signal power channel D	45.2.1.77
1.145 through 146	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T skew delay	45.2.1.78
1.147	10GBASE-T/40GBASE-T/25/5/2.5GBASE-T fast retrain status and control register	45.2.1.79

Table 45–4—PMA/PMD control 1 register bit definitions

Bit(s)	Name	Description	R/W
1.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved 0 1 1 1 = Reserved 0 1 1 0 = 5Gb/s 0 1 0 1 = 2.5Gb/s 0 1 0 0 = 25Gb/s 0 0 1 1 = 100Gb/s 0 0 1 0 = 40Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s	R/W

Note: 25G - 802.3by assignment ahead of 802.3bz

Table 45–6—PMA/PMD speed ability register bit definitions

Bit(s)	Name	Description	R/W
1.4.15:14	Reserved for future speeds	Value always 0	RO
1.4.13	5G capable	1 = PMA/PMD is capable of operating at 5 Gb/s 0 = PMA/PMD is not capable of operating as 5 Gb/s	RO
1.4.12	2.5G capable	1 = PMA/PMD is capable of operating at 2.5 Gb/s 0 = PMA/PMD is not capable of operating as 2.5 Gb/s	RO
1.4.11	25G capable	1 = PMA/PMD is capable of operating at 25 Gb/s 0 = PMA/PMD is not capable of operating as 25 Gb/s	RO
1.4.10	802.3bn EPOC	…	RO
1.4.9	100G capable	1 = PMA/PMD is capable of operating at 100 Gb/s 0 = PMA/PMD is not capable of operating as 100 Gb/s	RO
1.4.8	40G capable	1 = PMA/PMD is capable of operating at 40 Gb/s 0 = PMA/PMD is not capable of operating as 40 Gb/s	RO

Note: 25G - 802.3by assignment ahead of 802.3bz . EPOC took the bit 10

Table 45–7—PMA/PMD control 2 register bit definitions

Bit(s)	Name	Description	R/W
1.7.5:0	PMA/PMD type selection	5 4 3 2 1 0 1 1 1 1 1 x = reserved for future use 1 1 1 1 0 1 = 100BASE-T1 PMA/PMD 1 1 1 1 0 0 = reserved for future use 1 1 1 0 1 1 = reserved 1 1 1 0 1 0 = 25GBASE-SR PMA/PMD 1 1 1 0 1 0 = 25GBASE-KR PMA/PMD 1 1 1 0 1 0 = 25GBASE-CR PMA/PMD ~~1 1 0 x x x = reserved for future use~~ 1 1 0 1 x x = reserved for future use 1 1 0 0 1 1 = 10GPASS-XR-U PMA/PMD 1 1 0 0 1 0 = 10GPASS-XR-D PMA/PMD ~~1 1 0 0 0 x = reserved for future use~~ 1 1 0 0 0 1 = 5GBASE-T PMA/PMD 1 1 0 0 0 0 = 2.5GBASE-T PMA/PMD 1 0 1 1 1 1 = 100BASE-SR4 PMA/PMD …… 1 0 1 0 0 0 = 100GBASE-CR10 PMA/PMD ~~1 0 0 1 1 x = reserved for future use~~ 1 0 0 1 1 1 = reserved for future use 1 0 0 1 1 0 = 40GBASE-T PMA/PMD 1 0 0 1 0 1 = 40GBVASE-ER4 PMA/PMD ……	R/W

Note: 1 0 0 1 0 1 in .3bq D2.0 not right says “reserved” – just E error.
Note: 802.3bp did NOT take a value yet (missing)

Tables 45-9, 10, 11 TX/RX Fault & Disable Description

Table 45–9—Transmit fault description location

PMA/PMD	Description locations
40GBASE-T	113.4.2.2
25GBASE-T	TBD
5GBASE-T	TBD
2.5GBASE-T	TBD

Table 45–10—Receive fault description location

PMA/PMD	Description locations
40GBASE-T	113.4.2.4
25GBASE-T	TBD
5GBASE-T	TBD
2.5GBASE-T	TBD

Table 45–12—Transmit disable description location

PMA/PMD	Description locations
40GBASE-T	113.4.2.3
25GBASE-T	TBD
5GBASE-T	TBD
2.5GBASE-T	TBD

Table 45–14—PMA/PMD Extended Ability register bit definitions

Bit(s)	Name	Description	R/W
~~1.11.15:11~~ 1.11.15	Reserved	Value always 0	RO
1.11.14	5GBASE-T ability	1 = PMA/PMD is able to perform 5GBASE-T 0 = PMA/PMD is not able to perform 5GBASE-T	RO
1.11.13	2.5GBASE-T ability	1 = PMA/PMD is able to perform 2.5GBASE-T 0 = PMA/PMD is not able to perform 2.5GBASE-T	RO
1.11.12	25GBASE-T ability	1 = PMA/PMD is able to perform 25GBASE-T 0 = PMA/PMD is not able to perform 25GBASE-T	RO
1.11.11	40GBASE-T ability	1 = PMA/PMD is able to perform 40GBASE-T 0 = PMA/PMD is not able to perform 40GBASE-T	RO

Note: .3bq D2.0 references 45-14 as 45-16 w/ title “40G/100G PMA…” and states bit 1.13.6 (should be 1.11.11, the next reserved bit in order) – E. error.

Table 45–54—10G/40G/25G/5G/2.5GBASE-T status register bit definitions (RE: LP information Valid)

Bit(s)	Name	Description	R/W
1.129.0	LP Information valid	1 = Link partner information is valid 0 = Link partner information is not valid	RO

Change Table Names (and revise as necessary)

- **Table 45–55: 10/40/25/5/2.5GBASE-T pair swap and polarity register bit definitions**
- **Table 45–56: 10/40/25/5/2.5GBASE-T TX power backoff and PHY short reach setting register bit definitions**

Bit(s)	Name	Description	R/W
1.131	Short reach mode	1 = 10GBASE-T PHY is operating in short reach mode 0 = 10GBASE-T PHY is not operating in short reach mode	R/W

- **Table 45–57: 10/40/25/5/2.5GBASE-T test mode register bit definitions**
- **Table 45–58: 10/40/25/5/2.5GBASE-T skew delay register bit definitions**
- **Table 45–59: 10/40/25/5/2.5GBASE-T fast retrain status and control register bit definitions**

Note: .3bq D2.0 should make the Table 45-56 1.131 related change, ahead of 25GBT and .3bz

Table 45–119: PCS registers

Register address	Register name	Subclause
3.32	BASE-R, 10GBASE-T, ~~and~~ 25G/40GBASE-T, and 2.5G/5GBASE-T PCS status 1	45.2.3.13
3.33	BASE-R, 10GBASE-T, ~~and~~ 25G/40GBASE-T, and 2.5G/5GBASE-T PCS status 2	45.2.3.14

Note: .3bq D2.0 Subclause reference says 45.2.3.17 and 18, not right. E error.

Table 45–108: BASE-R, 10GBASE-T, ~~and~~ 40GBASE-T, 25GBASE-T, 5GBASE-T, and 2.5GBASE-T PCS status 1 register bit definitions

Bit(s)	Name	Description	R/W
3.32.12	BASE-R, 10GBASE-T, ~~and~~ 40GBASE-T, 25GBASE-T, 5GBASE-T, and 2.5GBASE-T receive link status	1 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T receive link up 0 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T receive link down	RO
3.32.1	BASE-R, 10GBASE-T, ~~and~~ 40GBASE-T, 25GBASE-T, 5GBASE-T, and 2.5GBASE-T high BER	1 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T reporting a high BER 0 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T not reporting a high BER	RO
3.32.0	BASE-R, 10GBASE-T, ~~and~~ 40GBASE-T, 25GBASE-T, 5GBASE-T, and 2.5GBASE-T PCS block lock	1 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T PCS locked to received blocks 0 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T PCS not locked to received blocks	RO

Table 45–129: BASE-R ~~and~~, 10GBASE-T, 25GBASE-T, 5GBASE-T, and 2.5GBASE-T PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W
3.33.15	Latched block lock	1 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T has block lock 0 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T does not have block lock	RO/LL
3.33.14	Latched high BER	1 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T has reported a high BER 0 = BASE-R or 10GBASE-T or 40GBASE-T or 25GBASE-T or 5GBASE-T or 2.5GBASE-T has not reported a high BER	RO/LH

RO = Read only, LL = Latching low, LH = Latching high, NR = Non Roll-over

Table 45–120—PCS control 1 register bit definitions

Bit(s)	Name	Description	R/W
3.0.5:2	Speed selection	5 4 3 2 1 x x x = Reserved 0 1 1 1 = 5Gb/s 0 1 1 0 = 2.5Gb/s 0 1 0 1 = 25Gb/s 0 1 0 0 = 100Gb/s 0 0 1 1 = 40Gb/s 0 0 1 0 = 10/1Gb/s 0 0 0 1 = 10PASS-TS/2BASE-TL 0 0 0 0 = 10Gb/s	R/W
3.0.1:0	Reserved	Value always 0	RO

Note: 25G assigned by .3by;

Table 45–122—PCS speed ability register bit definitions

Bit(s)	Name	Description	R/W
3.4.15:7	Reserved for future speeds	Value always 0	RO
3.4.6	5G capable	1 = PCS is capable of operating at 5 Gb/s 0 = PCS is not capable of operating at 25 Gb/s	RO
3.4.5	2.5G capable	1 = PCS is capable of operating at 2.5 Gb/s 0 = PCS is not capable of operating at 2.5 Gb/s	RO
3.4.4	25G capable	1 = PCS is capable of operating at 25 Gb/s 0 = PCS is not capable of operating at 25 Gb/s	RO
3.4.3	100G capable	1 = PCS is capable of operating at 100 Gb/s 0 = PCS is not capable of operating at 100 Gb/s	RO
3.4.2	40G capable	1 = PCS is capable of operating at 40 Gb/s 0 = PCS is not capable of operating at 40 Gb/s	RO
3.4.1	10PASS-TS/2BASE-TL capable	1 = PCS is capable of operating as the 10P/2B PCS 0 = PCS is not capable of operating as the 10P/2B PCS	RO
3.4.9	10G capable	1 = PCS is capable of operating at 10 Gb/s 0 = PCS is not capable of operating at 10 Gb/s	RO

FYI: 25G already assigned by .3by draft;

Little Ticket Item
Define extended field

Table 45–123: PCS control 2 register bit definitions

Bit(s)	Name	Description	R/W
~~3.7.15:3~~ **3.7.15:4**	Reserved	Value always 0	RO
~~3.7.2:0~~ 3.7.3:0	PCS type selection	**3** 2 1 0 1 1 x x = reserved 1 0 1 1 = Select 5GBASE-T PCS type 1 0 0 1 = Select 2.5GBASE-T PCS type 1 0 0 0 = Select 25GBASE-T PCS type 0 1 1 1 = Select 25GBASE-R PCS type 0 1 1 0 = Select 40GBASE-T PCS type 0 1 0 1 = Select 100GBASE-R PCS type 0 1 0 0 = Select 40GBASE-R PCS type 0 0 1 1 = Select 10GBASE-T PCS type 0 0 1 0 = Select 10GBASE-W PCS type 0 0 0 1 = Select 10GBASE-X PCS type 0 0 0 0 = Select 10GBASE-R PCS type	R/W

Note: 25G assigned by .3by, and used last value (1 1 1).
Propose to extend into reserved field (as intended) in .3bq when 25GBT gets in and ahead of .3bz.

Table 45–124—PCS status 2 register bit definitions

Bit(s)	Name	Description	R/W
3.8.13~~:12~~	Reserved	Value always 0	RO
3.8.12	5GBASE-T capable	1 = PCS is able to support 5GBASE-T PCS type 0 = PCS is not able to support 5GBASE-T PCS type	RO
~~3.8.9:6~~	~~Reserved~~	~~Value always 0~~	~~RO~~
3.8.9	2.5GBASE-T capable	1 = PCS is able to support 2.5GBASE-T PCS type 0 = PCS is not able to support 2.5GBASE-T PCS type	RO
3.8.8	25GBASE-T capable	1 = PCS is able to support 25GBASE-T PCS type 0 = PCS is not able to support 25GBASE-T PCS type	RO
3.8.7	25GBASE-R capable	1 = PCS is able to support 25GBASE-R PCS type 0 = PCS is not able to support 25GBASE-R PCS type	RO
3.8.6	40GBASE-T capable	1 = PCS is able to support 40GBASE-T PCS type 0 = PCS is not able to support 40GBASE-T PCS type	RO

Little Ticket Item
Need new Reg

Table 45–125—EEE capability register bit d

Bit(s)	Name	Description	R/W
3.20.15	5GBASE-T EEE	1 = EEE is supported for 5GBASE-T 0 = EEE is not supported for 5GBASE-T	RO
3.20.14	2.5GBASE-T EEE	1 = EEE is supported for 2.5GBASE-T 0 = EEE is not supported for 2.5GBASE-T	RO
3.20.13	100GBASE-R deep sleep	1 = EEE deep sleep is supported for 100GBASE-R …	RO
3.20.12	100GBASE-R fast wake	1 = EEE fast wake is supported for 100GBASE-R …	RO
3.20.11	25GBASE-R deep sleep	1 = EEE deep sleep is supported for 25GBASE-R 0 = EEE deep sleep is not supported for 25GBASE-R	RO
3.20.10	25GBASE-R fast wake	1 = EEE fast wake is supported for 25GBASE-R 0 = EEE fast wake is not supported for 25GBASE-R	RO
No Room!	25GBASE-T EEE	1 = EEE is supported for 25GBASE-T 0 = EEE is not supported for 25GBASE-T	RO
3.20.8 & 9	*40GBASE-R DS & FW*	*1 = EEE DS & FW respectively.*	*RO*
3.20.7	40GBASE-T EEE	1 = EEE is supported for 40GBASE-T 0 = EEE is not supported for 40GBASE-T	RO
3.20.0	LPI_FW	1 = Fast wake mode is used for LPI function 0 = Deep sleep is used for LPI function	R/W

Note: . Also no room for other projects in flight – so go somewhere else.

Table 45–200—Auto-Negotiation MMD registers

Register address	Register name	Subclause
7.32	10GBASE-T/40GBASE-T/25GBASE-T/5GBASE-T/2.5GBASE-T AN control	45.2.7.10
7.33	10GBASE-T/40GBASE-T/25GBASE-T/5GBASE-T/2.5GBASE-T AN status	45.2.7.11

Table 45–207: 10GBASE-T/40GBASE-T/25GBASE-T/5GBASE-T/2.5GBASE-T AN control register

Bit(s)	Name	Description	R/W
7.32.12	10GBASE-T ability	1 = Advertise PHY as 10GBASE-T capable. …	R/W
7.32.11	40GBASE-T ability	1 = Advertise PHY as 40GBASE-T capable 0 = Do not advertise the PHY as 40GBASE-T capable	R/W
7.32.9	25GBASE-T ability	1 = Advertise PHY as 25GBASE-T capable 0 = Do not advertise the PHY as 25GBASE-T capable	R/W
7.32.8	2.5GBASE-T ability	1 = Advertise PHY as 2.5GBASE-T capable 0 = Do not advertise the PHY as 2.5GBASE-T capable	R/W
7.32.7	5GBASE-T ability	1 = Advertise PHY as 5GBASE-T capable 0 = Do not advertise the PHY as 5GBASE-T capable	R/W
7.32.6	5GBASE-T Fast retrain ability	1 = Advertise PHY as 5GBASE-T fast retrain capable 0 = Do not advertise PHY as 5GBASE-T fast retrain capable	R/W
7.32.5	2.5GBASE-T Fast retrain ability	1 = Advertise PHY as 2.5GBASE-T fast retrain capable 0 = Do not advertise PHY as 2.5GBASE-T fast retrain capable	R/W
7.32.4	25GBASE-T Fast retrain ability	1 = Advertise PHY as 25GBASE-T fast retrain capable 0 = Do not advertise PHY as 25GBASE-T fast retrain capable	R/W
7.32.3	40GBASE-T Fast retrain ability	1 = Advertise PHY as 40GBASE-T fast retrain capable 0 = Do not advertise PHY as 40GBASE-T fast retrain capable	R/W
7.32.2	*(10G) LD PMA T Rst Req*	*1 = Local device requests that LP reset PMA training PRBS every frame*	*R/W*
7.32.1	*10GBASE-T Fast retrain ability*	*1 = Advertise PHY as 10GBASE-T fast retrain capable* *0 = Do not advertise PHY as 10GBASE-T fast retrain capable*	*R/W*
7.32.0	*(10G) LD Loop timing ability*	*1 = Advertise PHY as capable of loop timing* *0 = Do not advertise PHY as capable of loop timing*	*R/W*

Note: .3bq D2.0 does not add "10GBASE-T" to 7.32.2 nor 7.32.0, as done to 7.32.1. E error?

Little Ticket Item
Need "repeat" train?

Table 45–208—10GBASE-T/40GBASE-T/25GBASE-T/ 5GBASE-T/2.5GBASE-T AN status register

Bit(s)	Name	Description	R/W
7.33.8	Link partner 40GBASE-T capability	1 = Link partner is able to operate as 40GBASE-T 0 = Link partner is not able to operate as 40GBASE-T	RO
7.33.7	Link partner 25GBASE-T capability	1 = Link partner is able to operate as 25GBASE-T 0 = Link partner is not able to operate as 25GBASE-T	RO
7.33.6	Link partner 5GBASE-T capability	1 = Link partner is able to operate as 5GBASE-T 0 = Link partner is not able to operate as 5GBASE-T	RO
7.33.5	Link partner 2.5GBASE-T capability	1 = Link partner is able to operate as 2.5GBASE-T 0 = Link partner is not able to operate as 2.5GBASE-T	RO
7.33.4	2.5GBASE-T Fast retrain ability	1 = Link partner is capable of 2.5GBASE-T fast retrain 0 = Link partner is not capable of 2.5GBASE-T fast retrain	RO
7.33.3	5GBASE-T Fast retrain ability	1 = Link partner is capable of 5GBASE-T fast retrain 0 = Link partner is not capable of 5GBASE-T fast retrain	RO
7.33.2	25GBASE-T Fast retrain ability	1 = Link partner is capable of 25GBASE-T fast retrain 0 = Link partner is not capable of 25GBASE-T fast retrain	RO
7.33.1	10GBASE-T Fast retrain ability	1 = Link partner is capable of 10GBASE-T fast retrain 0 = Link partner is not capable of 10GBASE-T fast retrain	RO
7.33.0	40GBASE-T Fast retrain ability	1 = Link partner is capable of 40GBASE-T fast retrain 0 = Link partner is not capable of 40GBASE-T fast retrain	RO

Note: .3bq D2.0 40G "Repeat training" bit not reflected any where.

Little Ticket Item
Need new
Reg 7.62 ?

Table 45–210—EEE advertisement register (Register 7.60) bit definitions

Bits(s)	Name	Description	CL ref; NP bit number	R/W
No Room	5GBASE-T EEE	1 = Advertise that the 5GBASE-T has EEE capability 0 = Do not advertise that the 5GBASE-T has EEE capability	TBD	R/W
No Room	2.5GBASE-T EEE	1 = Advertise that the 2.5GBASE-T has EEE capability 0 = Do not advertise that the 2.5GBASE-T has EEE capability	TBD	R/W
7.60.15	25GBASE-KR or 25GBASE-CR EEE	1 = Advertise that the 25GBASE-KR or 25GBASE-CR has EEE deep sleep capability	TBD	R/W
7.60.14	25GBASE-KR-S or 25GBASE-CR-S EEE	1 = Advertise that the 25GBASE-KR-S or 25GBASE-CR-S has EEE deep sleep capability	TBD	R/W
7.60.13	100GBASE-CR4 EEE	1 = Advertise that the 100GBASE-CR4 has EEE deep sleep capability 0 = Do not advertise that the 100GBASECR4 has EEE deep sleep capability	73.7.7.1; U13	R/W
7.60.9	40GBASE-T EEE	1 = Advertise that the 40GBASE-T has EEE capability 0 = Do not advertise that the 40GBASE-T has EEE capability	113.6.1; U21	R/W
7.60.3	10GBASE-T EEE	1 = Advertise that the 10GBASE-T has EEE capability 0 = Do not advertise that the 10GBASE-T has EEE capability	28.2.3.4.1; U3 / 55.6.1; U24	R/W
7.60.1	100BASE-TX EEE	1 = Advertise that the 100BASE-TX has EEE capability 0 = Do not advertise that the 100BASETX has EEE capability	28.2.3.4.1; U1 / 55.6.1; U22	R/W
7.60.0	25GBASE-T EEE	1 = Advertise that the 25GBASE-T has EEE capability 0 = Do not advertise that the 25GBASE-T has EEE capability	TBD	R/W

Note: .3by does not have CL ref in its table

Little Ticket Item
Need new
Reg 7.63 ?

Table 45–211—EEE link partner ability (Register 7.61) bit definitions

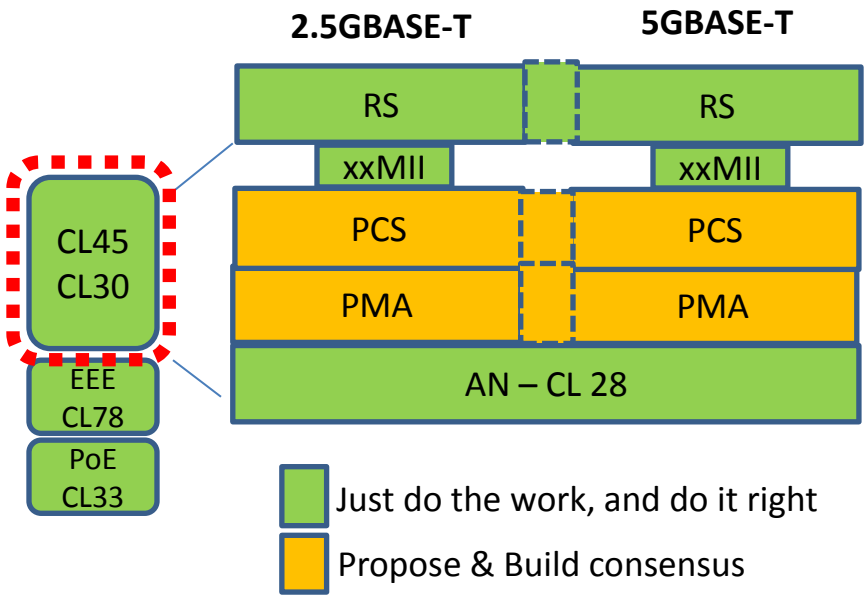
Bits(s)	Name	Description	CL ref; NP bit number	R/W
No Room	5GBASE-T EEE	1 = Link partner is advertising EEE capability for 5GBASE-T 0 = Link partner is not advertising EEE capability for 5GBASE-T	TBD	RO
No Room	2.5GBASE-T EEE	1 = Link partner is advertising EEE capability for 2.5GBASE-T 0 = Link partner is not advertising EEE capability for 2.5GBASE-T	TBD	RO
7.61.15	25GBASE-KR or 25GBASE-CR EEE	1 = Link partner is advertising EEE deep sleep capability for 25GBASE-KR or 25GBASE-CR	TBD	RO
7.61.14	25GBASE-KR-S or 25GBASE-CR-S EEE	1 = Link partner is advertising EEE deep sleep capability for 25GBASE-KR-S or 25GBASE-CR-S	TBD	RO
7.61.13	100GBASE-CR4 EEE	1 = Link partner is advertising EEE deep sleep capability for 100GBASECR4 0 = Link partner is not advertising EEE deep sleep capability for 100GBASECR4	73.7.7.1; U13	RO
7.61.9	40GBASE-T	1 = Link partner is advertising EEE capability for 40GBASE-T 0 = Link partner is not advertising EEE capability for 40GBASE-T	28.2.3.4.128; U3 / 113.6.1; U24	RO
7.61.1	100BASE-TX EEE	1 = Link partner is advertising EEE capability for 100BASE-TX 0 = Link partner is not advertising EEE capability for 100BASE-TX	28.2.3.4.1; U1 / 55.6.1; U22	RO
7.61.0	25GBASE-T EEE	1 = Link partner is advertising EEE capability for 25GBASE-T 0 = Link partner is not advertising EEE capability for 25GBASE-T	TBD	RO

Note:.3by does not have CL ref in its table.

Summary

- CL 45 Management changes straight forward.
  - Changes & Adds as proposed in this presentation.
  - Some “little ticket” items to be addressed via additional registers (next step).
  - Parallel project challenges -- .3bq and .3by – manageable.
  - TBDs are completely within expectations (e.g. references)
  - Coordinate new registers w/ .3bq (if it desires), or **let 25G move forward w/ .3bq and just focus on .3bz (and be self-consistent)**

- Next Steps
  - Add new registers (“no room”) that are identified.
  - Build consensus for .3bz mgmt. (Feedback, always welcome)
  - Consider as Mgmt (CL45) baseline into May interim meeting.



Thank you!