Proposed comment for P802.3cj

Adee Ran

Intel

Overview

- A draft comment and proposed change were presented in the November 29th teleconference (see ran_tp_01_2017_11_29).
- The proposed change was further refined in email correspondence following the teleconference, and in discussions in the December 13th teleconference.

Comment text

Following the October 2017 Liaison letter from ITU-T SG15/Q13, an ad hoc was formed to discuss concerns that were raised about Ethernet timing performance.

The ad hoc identified one source of variability in the reported path data delays that could be reduced in PHYs which include a FEC function. This variability is a source of perceived inaccuracy of timestamping, although in fact the sum of the delays in the FEC encoder and FEC decoder is constant.

This perceived inaccuracy can be eliminated if the path data delays in the transmitter and the receiver are reported in a specific manner.

In addition, for PHYs in which the FEC is a separate sublayer, there are no specified registers for the FEC delay reporting.

The recommendation of the ad hoc is to add a recommendation in clause 90 as detailed in the proposed change.

Proposed change

Insert the following paragraph after the first paragraph of 90.7:

"For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD is at the start of the FEC block."

Insert the following paragraph after the "NOTE 2" paragraph:

"NOTE 3—For PHYs that are specified with an FEC sublayer separate from the PCS, the data delay for the FEC sublayer should be included in either the PCS delay registers or the PMA/PMD delay registers of the MMD in which the FEC sublayer is implemented, but not in both."

Change with context

90.7 Data delay measurement

The TimeSync capability requires measurement of data delay in the transmit and receive paths, as shown in Figure 90–3. The transmit path data delay is measured from the beginning of the SFD at the xMII input to the beginning of the SFD at the MDI output. The receive path data delay is measured from the beginning of the SFD at the MDI input to the beginning of the SFD at the xMII output.

For a PHY that includes an FEC function, the transmit and receive path data delays may show significant variation depending upon the position of the SFD within the FEC block. However, since the variation due to this effect in the transmit path is expected to be compensated by the inverse variation in the receive path, it is recommended that the transmit and receive path data delays be reported as if the SFD is at the start of the FEC block.

The receiver of a multi-lane PHY is expected to include a buffer to compensate for skew between the lanes. This buffer selectively delays each lane such that the lanes are aligned at the buffer output. The earliest arriving lane experiences the most delay through the buffer and the latest arriving lane experiences the least delay through the buffer. The receive path data delay for a multi-lane PHY is reported as if the beginning of the SFD arrived at the MDI input on the lane with the smallest buffer delay.
(…)

NOTE 2—The data delay values represent only the data delay in the PHY sublayers. The TimeSync Client may need to adjust for delays within the gRS. For example, the TimeSync Client may need to subtract the value of the delay associated with the TS_SFD_Detect_TX function from the sum of the minimum transmit data delay values reported by individual MMD(s). Likewise, the TimeSync Client may need to add the value of the delay associated with the TS_SFD_Detect_RX function to the sum of the maximum receive data delay values reported by individual MMD(s).

NOTE 3—For PHYs that are specified with an FEC sublayer separate from the PCS, the data delay for the FEC sublayer should be included in either the PCS delay registers or the PMA/PMD delay registers of the MMD in which the FEC sublayer is implemented, but not in both.