XBI - Optional PMA Service Interface for Serial PMD's

IEEE P802.3ae La Jolla Meeting

July 10-14, 2000

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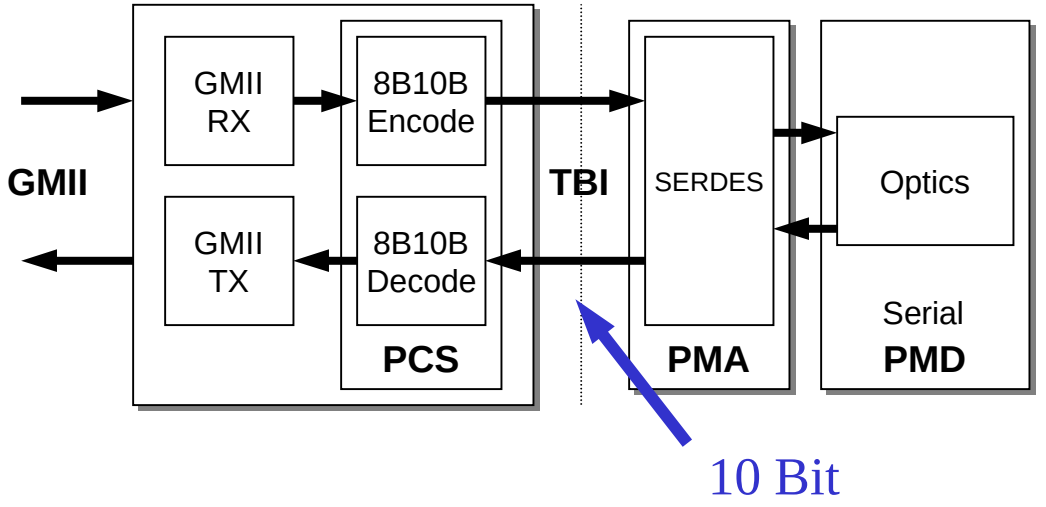
Optional PMA Interface Spec needed

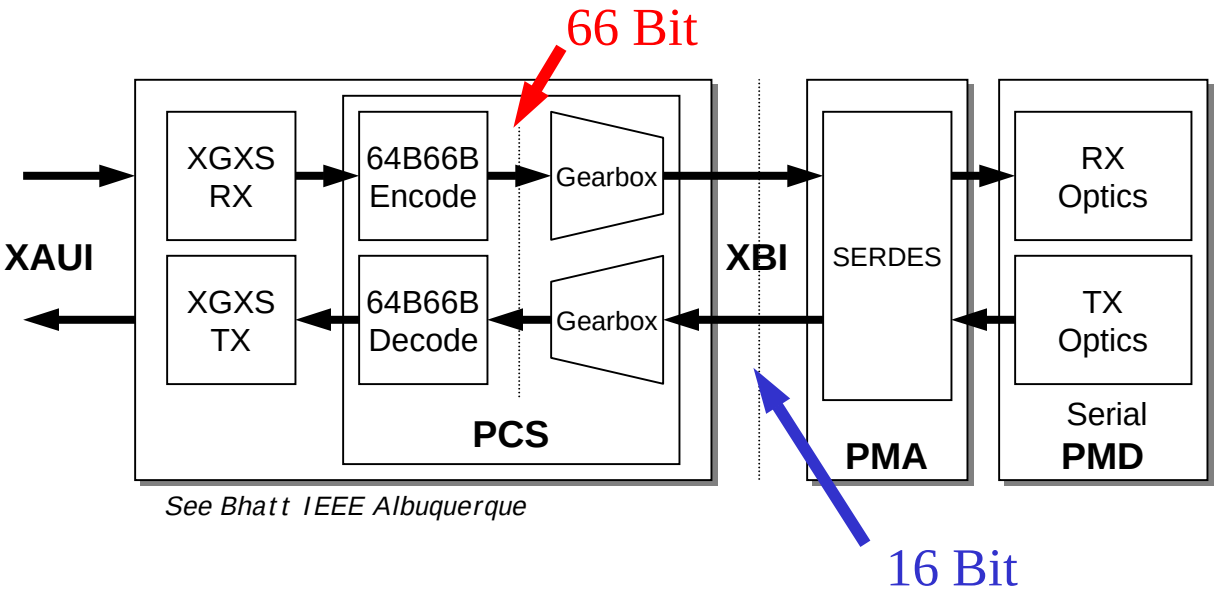
- An Optional PMA Interface (XBI) definition is needed
  - Ensure interoperability between Serial WAN/LAN PCS and SERDES chips (within optical module).
- PCS to PMA interface logical technology split
  - PCS likely in CMOS
  - PMA SERDES likely in SiGe, GaAs, Silicon Bipolar etc.
  - Potential to have these devices come from different vendors.
  - Interoperability definition required.

PMA Interface Precedent

- Gigabit Ethernet
- IEEE 802.3 1998 defines the Ten Bit Interface for serial transmission.
- Physical Instantiation of PMA (Clause 36.3.3 to 36.3.6).
- 8B/10B output is 10 bits wide.
- Narrow enough to use as the PMA Interface.



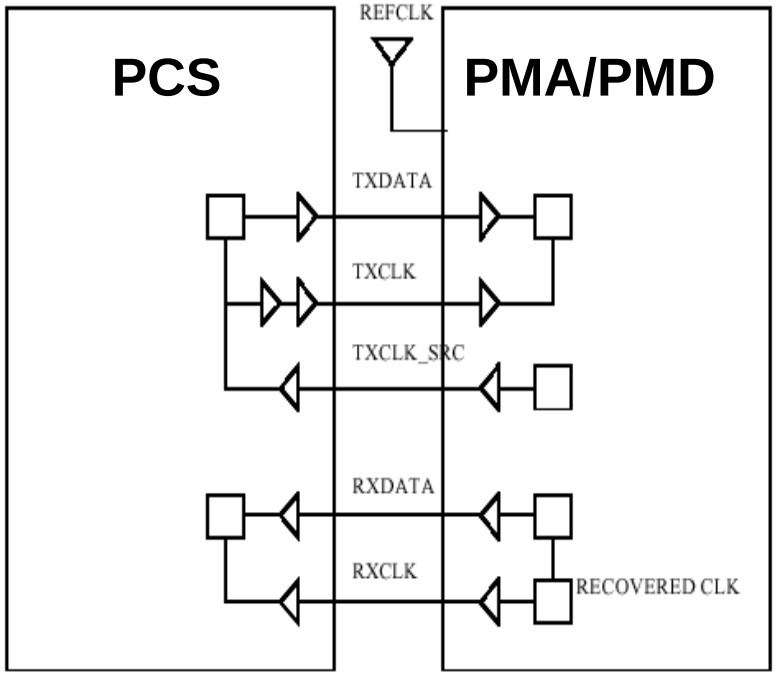
- 10 Gigabit Ethernet Serial LAN PHY
- 64B66B coder output is 66 bits wide.
- Gearbox solution to reduce pins to 16, a manageable number.



See Bhatt IEEE Albuquerque

PMA Service Interface XBI Proposal

- Aggregate rate of 9.953 - 10.3 Gbit/s.
- 16 differential pairs with 622-645 MHz operation, LVDS I/O
- 622-645 MHz Source synchronous clocking.
- REFCLK remains unspecified.



PMA Interface for Serial Transmission

SFI-4 16 Bit SERDES Interface

- OIF SERDES interface for OC-192 (SFI-4)
  - Aggregate rate of 9.953 Gbit/s.
  - 16 differential pairs with 622 MHz operation.
  - LVDS I/O (IEEE Std 1596.3-1996).
  - 622MHz Source synchronous clocking.
  - SFI-4 Applicable to speeds up to 10.66 Gbit/s.
- Status:
  - Specification in final ballot now. (reference doc number OIF1999.102).
  - Interface has been demonstrated in working silicon.
- 10GE Serial LAN PHY Rate Accommodated by Existing Spec
  - "Other reference clock frequencies in addition to the 622.08 MHz are allowed"
  - We are within the bounds of SFI-4 as long as encoded bit rate is less than 10.6Gbit/s.
  - Use SFI-4 16x622 as base - set operating range 622 to 645 MHz for 10.3 Gbit/s.
  - Relaxation of SFI-4 may be necessary for Ethernet applications.

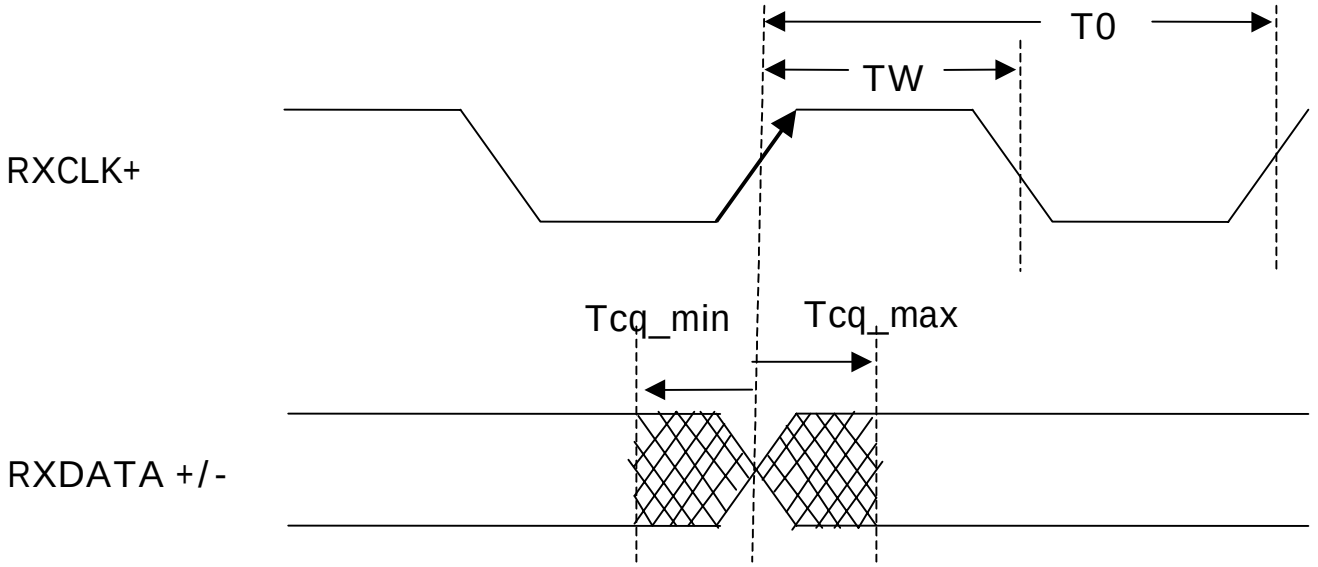
Why Add XBI to the IEEE 802.3ae standard

- OIF SFI-4 16x622 work has been done.
- Current SFI-4 spec allows higher freq, but does not specify them.
  - Thus, it is not guaranteed that vendors will build LAN PHY rate in an interoperable fashion
- OIF not a standards body (they create specifications for implementor's agreements) thus the IEEE P802.3ae cannot reference the SFI-4 specification.
- IEEE P802.3ae needs to control the PMA Interface definition so that it is not changed by the OIF.

XBI Interface Signals

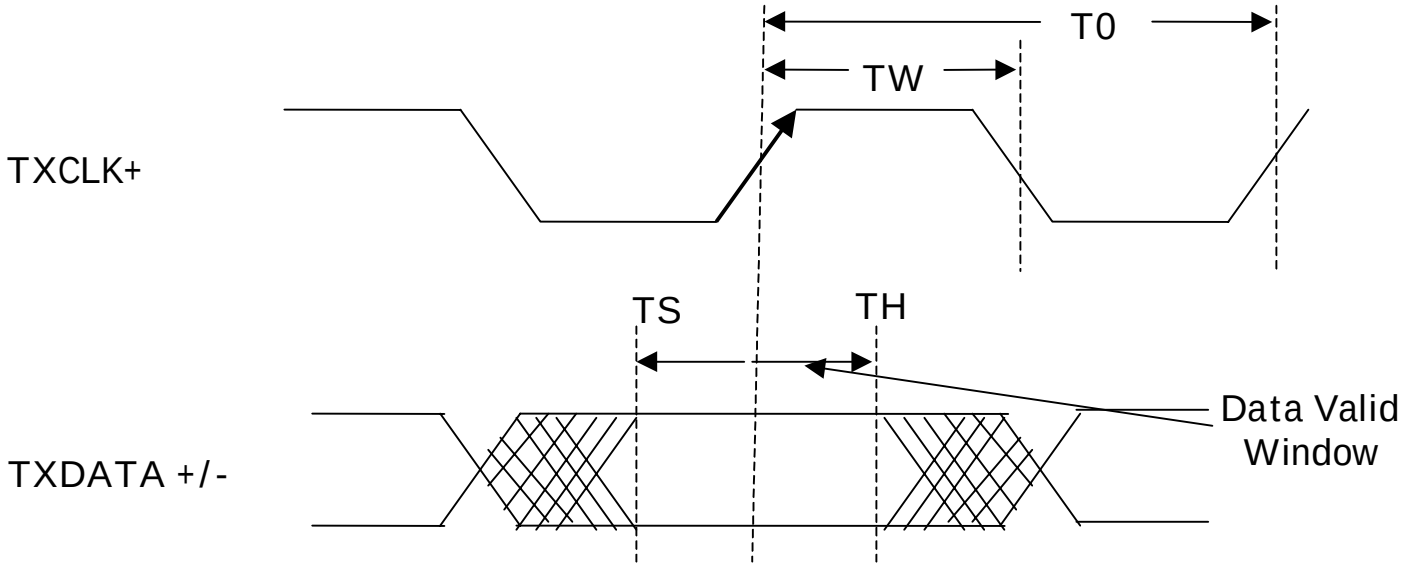
Symbol	Signal Name	Signal Type	Active Level	Description
PMA_TXDATA+<15:0> PMA_TXDATA-<15:0>	Transmit Data	I-LVDS	Diff	16 bit transmit data from the PCS to PMA.
PMA_TXCLK+ PMA_TXCLK-	Transmit Clock.	I-LVDS	Diff	Transmit clock to latch data into PMA. Ranges from 622 MHz to 645 MHz with +/- 100ppm tolerance.
PMA_TXCLK_SRC+ PMA_TXCLK_SRC-	Transmit Clock Source	I-LVDS	Diff	Transmit clock from the PMA to the PCS. May be used by PCS to generate the transmit clock.
PMA_RXDATA+<15:0> PMA_RXDATA-<15:0>	Receive Data	I-LVDS	Diff	16 bit received data presented to the PCS from the PMA.
PMA_RXCLK+ PMA_RXCLK-	Receive Clock	I-LVDS	Diff	Receive clock to latch data into PCS. Ranges from 622 MHz to 645 MHz with +/- 100ppm tolerance.

XBI PMA LVDS Output Waveforms



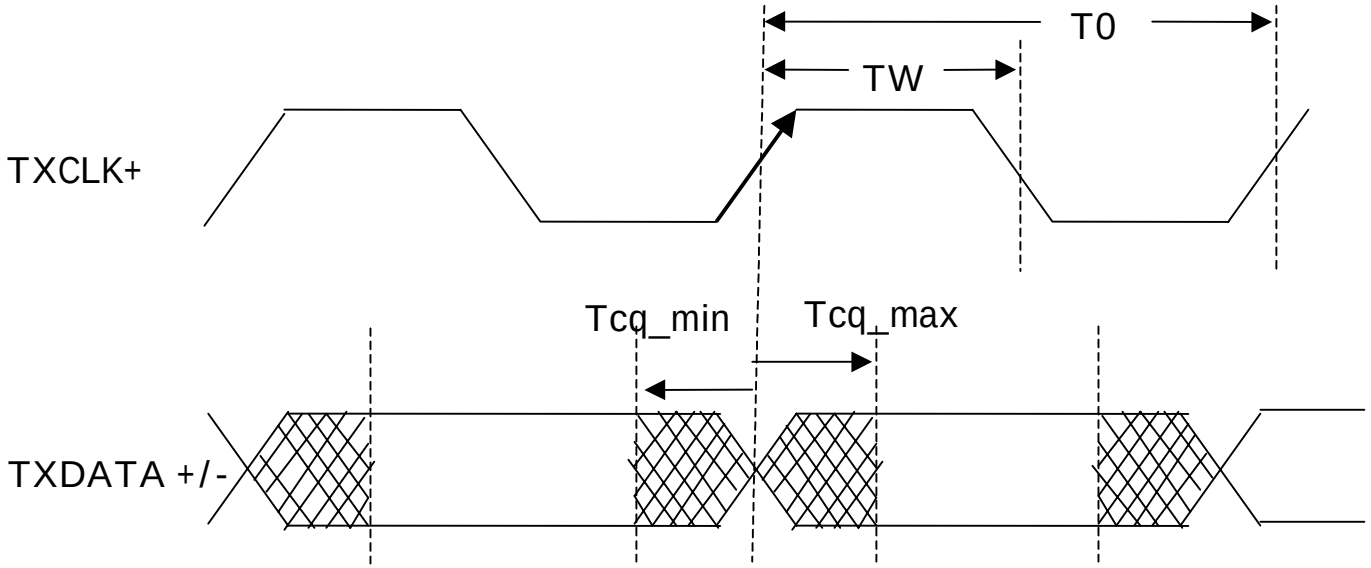
Parameter	Description	Value	Units
T0	Clock period	1.552 to 1.608	ns
TW/T0	duty cycl	0.45 < TW/T0 < 0.55	
TR, TF	20-80% rise, fall times	100-250	ps
Tcq_min, Tcq_max	Clock to out times	200, 200	ps

XBI PMA LVDS Input Waveforms



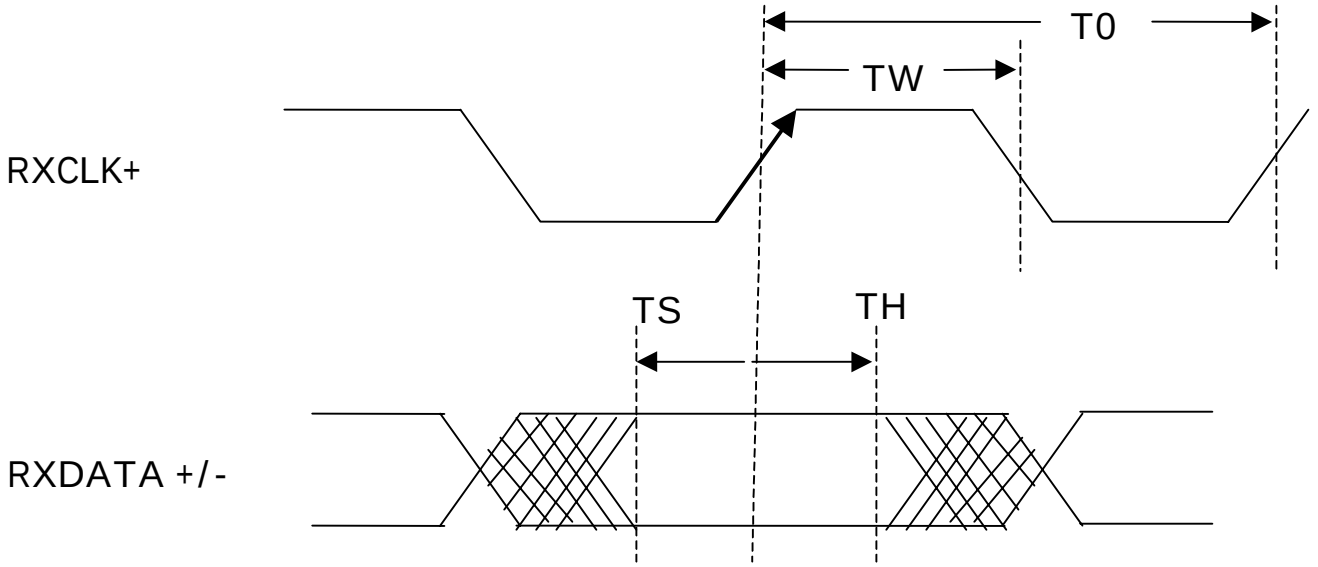
Parameter	Description	Value	Units
T0	Clock period	1.552 to 1.608	ns
TW/T0	duty cycl	0.4 < TW/T0 < 0.6	
TR, TF	20-80% rise, fall times	100-300	ps
Tcq_min, Tcq_max	Clock to out times	300, 300	ps

XBI PCS LVDS Output Waveforms



Parameter	Description	Value	Units
T0	Clock period	1.552 to 1.608	ns
TW/T0	duty cycle	0.4 < TW/T0 < 0.6	
TR, TF	20-80% rise, fall times	100-250	ps
TS, TH	Clock to out times	200, 200	ps

XBI PCS LVDS Input Waveforms



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TS, TH	Clock to out times	300, 300	ps

Issues to Resolve

- Determine appropriate jitter requirements.
  - To be addressed at a meeting at this plenary.

Summary

- An Optional Instantiation of the PMA Service Interface needs to be defined for the Serial PHYs in IEEE P802.3ae
  - Ensure interoperability between Serial WAN/LAN PCS and SERDES chips (in optical module).
  - Promotes multi-vendor chip interoperability.
- PCS-PMA Logical technology split.
- Builds on the precedent of Gigabit Ethernet TBI (Clause 36.3.3).
- Simply re-use OIF work to achieve Time to Market
  - SFI-4 16x622 specification is complete.
  - Cannot reference OIF SFI-4.
  - SFI-4 can accommodate both LAN & WAN PHY rates.
    - 622 – 645 MHz LVDS within current process capabilities
    - 622 – 645 MHz board implementation understood.
    - Relaxation may be necessary for Ethernet environments.