Optional Physical Instantiation of a PMA Service Interface for Serial PMD's

IEEE P802.3ae Ottawa Interim Meeting

May 22-26, 2000

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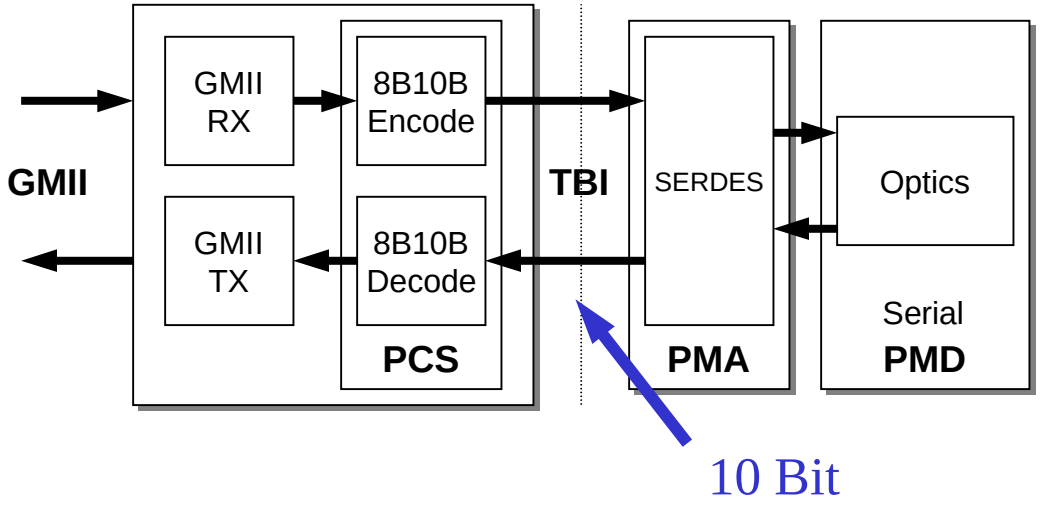
Optional PMA Interface Spec needed

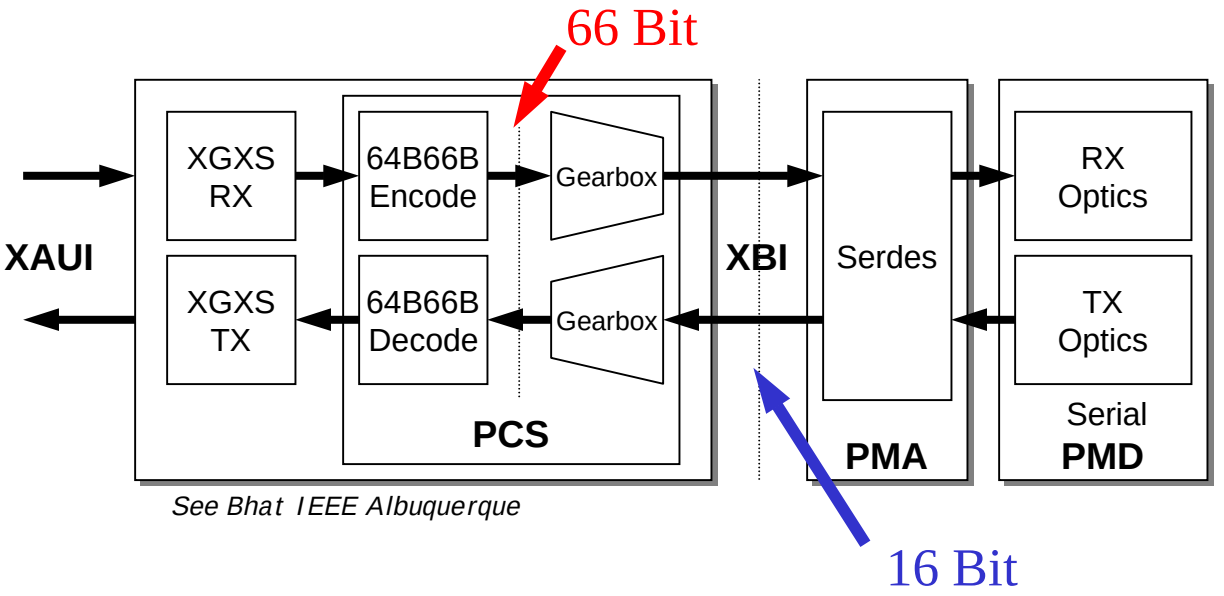
- An Optional PMA Interface (XBI) definition is needed
  - Ensure interoperability between Serial WAN/LAN PCS and SERDES chips (within optical module).
- PCS to PMA interface logical technology split
  - PCS likely in CMOS
  - PMA SERDES likely in SiGe, GaAs, Silicon Bipolar etc.
  - Potential to have these devices come from different vendors.
  - Interoperability definition required.

PMA Interface Precedent

- Gigabit Ethernet
- IEEE 802.3 1998 defines the Ten Bit Interface for serial transmission.
- Physical Instantiation of PMA (Clause 36.3.3 to 36.3.6).
- 8B/10B output is 10 bits wide.
- Narrow enough to use as the PMA Interface.



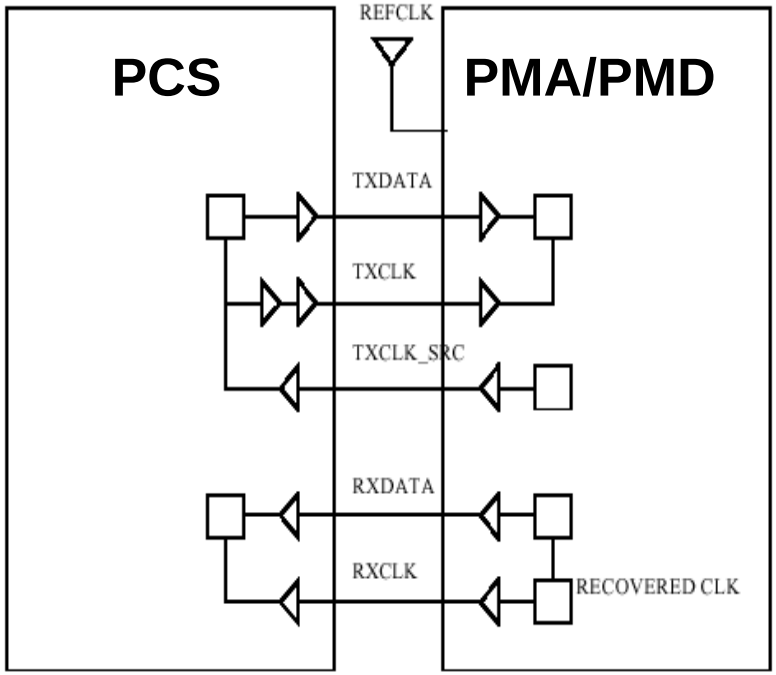
- 10 Gigabit Ethernet Serial LAN PHY
- 64B66B coder output is 66 bits wide.
- Gearbox solution to reduce pins to 16, a manageable number.



See Bhat IEEE Albuquerque

PMA Service Interface XBI Proposal

- Aggregate rate of 9.953 - 10.3 Gbit/s.
- 16 differential pairs with 622-645 MHz operation.
- LVDS I/O
- 622-645 MHz Source synchronous clocking.



PMA Interface for Serial Transmission

SFI-4 16 Bit SERDES Interface

- OIF SERDES interface for OC-192 (SFI-4)
  - Aggregate rate of 9.953 Gbit/s.
  - 16 differential pairs with 622 MHz operation.
  - LVDS I/O (IEEE Std 1596.3-1996).
  - 622MHz Source synchronous clocking.
  - SFI-4 Applicable to speeds up to 10.66 Gbit/s.
- Status:
  - Specification in final ballot now. (reference doc number OIF1999.102).
  - Interface has been demonstrated in working silicon.
- 10GE Serial LAN PHY Rate Accommodated by Existing Spec
  - "Other reference clock frequencies in addition to the 622.08 MHz are allowed"
  - We are within the bounds of SFI-4 as long as encoded bit rate is less than 10.6Gbit/s.
  - Use SFI-4 16x622 as base - set operating range 622 to 645 MHz for 10.3 Gbit/s.
  - Relaxation of SFI-4 may be necessary for Ethernet applications.

SFI-4 16 Bit SERDES Signals

- SERDES SFI-4 Signals
  - Change speed to accommodate rates up to 10.3 Gbaud.
  - REFCLK changes from 622MHz to range of 622 - 645 MHz.
- TX Clocking
  - TXCLK_SRC Source Clock (from REFCLK)
  - TXCLK at PCS derived from TXCLK_SRC
- RX Clocking
  - RXCLK - recovered clock.
  - Under LOS, uses REFCLK.

PIN NAME	I/O TYPE w.r.t. SERDES	DESCRIPTION
TXDATA[15:0]_P/N[1]	input, diff. LVDS	622.08 Mb/s per pin, transfers 16 bits of data from the SONET framer ASIC to the MUX device.
TXCLK_P/N[2]	input, diff. LVDS	622.08 MHz/311 Mhz, source synchronous clock for TXDATA. Frequency is mode selectable.
TXCLK_SRC_P/N	output, diff. LVDS	622.08 MHz, Reference clock from the SERDES to the SONET framer ASIC.
RXDATA[15:0]_P/N[1]	output, diff. LVDS	622.08 Mb/s per pin, Received data from the DEMUX to the SONET framer ASIC.
RXCLK_P/N	output, diff. LVDS	622.08 MHz, Received clock to qualify RXDATA. Maximum frequency is +2500ppm relative to REFCLK which is a minimum period of 1604 picoseconds.
REFCLK_P/N	input, diff. LV-PECL[4]	622.08 MHz, Board level reference provided.
PHASE_INIT[3]	input, LV-TTL	Optional. Asynchronous, low speed signal. Resets the SERDES clocking interface. Minimum active high pulse width is 5 microseconds.
PHASE_ERR[3]	output, LV-TTL	Optional. Low speed signal. Indicates that the phase of the TXCLK wrt the internal SERDES clock is out of spec.
SYNC_ERR	output, LV-TTL	low speed signal. Indicates RXCLK and RXDATA are not derived from the optical receive signal

Why Add XBI to the IEEE 802.3ae standard

- OIF SFI-4 16x622 work has been done.
- Current SFI-4 spec allows higher freq, but does not specify them.
  - Thus, it is not guaranteed that vendors will build LAN PHY rate in an interoperable fashion
- OIF not a standards body (they create specifications for implementor's agreements) thus the IEEE P802.3ae cannot reference the SFI-4 specification.
- IEEE P802.3ae needs to control the PMA Interface definition so that it is not changed by the OIF.

Summary

- An Optional Instantiation of the PMA Service Interface needs to be defined for the Serial PHYs in IEEE P802.3ae
  - Ensure interoperability between Serial WAN/LAN PCS and SERDES chips (in optical module).
  - Promotes multi-vendor chip interoperability.
- PCS-PMA Logical technology split.
- Builds on the precedent of Gigabit Ethernet TBI (Clause 36.3.3).
- Simply re-use OIF work to achieve Time to Market
  - SFI-4 16x622 specification is complete.
  - Cannot reference OIF SFI-4.
  - SFI-4 can accommodate both LAN & WAN PHY rates.
    - 622 – 645 MHz LVDS within current process capabilities
    - 622 – 645 MHz board implementation understood.
    - Relaxation may be necessary for Ethernet environments.