Derivation of Startup Mode Parameters

For IEEE 802.3af Standard Power over MDI

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General

The attached document includes the data and steps used to derive the Startup mode parameters.

In the May 2001 IEEE interim meeting, we set the following requirement:

“PSEs support inrush for PDs up to 50 uF. Above 50 uF, the PD must provide inrush limiting”.

We need to:

1. Specify the inrush current parameters for PSE and PD.
2. Optimize the 50uF value by checking if we can increase it.

List of System Objectives

The information that we have received from Dave Dwelly and others at May 2001 interim meeting and additional info during the last weeks was that the startup mode should allow meeting the following objectives:

1. To allow integration of Mosfets in a chip.
2. The max. energy allowed on a package is 1 joule max for SO-8 package, 2-3 joules for 36-pin SSOP and 5 joules for QFP.
3. Limit the burden on the PSE power supply during startup
4. To use numbers that we already agree upon in normal operating mode as well as for startup mode to simplify system definitions.
5. Startup mode is non-repetitive operation. It is not required that more than 1 port will startup simultaneously.

Derivation of Startup Mode Parameters

The following assumptions are made in the following paragraphs:

1. Startup mode is not a random phenomenon. It is a well-controlled and defined mode in the time domain.

2. Insertion of a PD to the system is done one at a time. It is not real situation that more than one PD will be simultaneously connected to multi-port system.
   If such scenario occurs, the startup mode for each port is controlled according to a pre-defined sequence.

3. During startup mode, the PSE is required to allow limited peak current for a limited time in order to allow charging of the PD input capacitor to the level which required to turn on the PD power supply.
   The current should be limited due to the fact that during startup mode the current limiting device faces a short load condition caused by the PD discharged input cap.

   Limiting the current causes a power loss on the limiting device that should be kept low enough to allow reliable operation. In addition, during normal powering mode, it is needed to ignore peak transient current caused by changes in PSE output voltage for a limited time in order to allow continuous operation without interruption.

Equations Derivation

In order to get worst case results, let's assume that N ports device periodically activates each port through the Startup mode at period T0, and Duty Cycle=Tc/T0.

Vport = Port voltage
Iport = Port current limit level
N = Number of active ports per device(active port at startup mode).
Tc = The time that the port is in current limit situation (i.e The PD capacitor charging time).
Emax= Max energy allowed on the device.

Peak power dissipated on each port: $$Ppeak = Vport \cdot Ip$$ Eq-1

Average power dissipated on each port assuming constant current source charging a capacitor.

Each port is activated at period T0: $$Pavg = 0.5 \cdot Vport \cdot Ip \cdot \frac{Tc}{T0}$$ Eq-2

Total average power for N ports device: $$Pavgt = 0.5 \cdot N \cdot Vport \cdot Ip \cdot \frac{Tc}{T0}$$ Eq-3

Total energy dissipated on N ports device accumulated over $t = T$, $T = N \cdot T0$:

$$E\max \geq 0.5 \cdot N \cdot Vport \cdot Ip \cdot Tc$$ Eq-4

Re-arranging Eq-4: $$Tc \leq \frac{E\max}{0.5 \cdot N \cdot Vport \cdot Ip}$$ Eq-5

The factor 0.5 at the denominator is true for current limiting device charging a capacitor.
During complete short at the PSE output the above factor is 1. Thermal protection in the chip will handle both cases allowing optimum utilization of the energy equation.

Assuming that in the N port device only one port is performing the startup mode (we can control the timing) and there is a time interval until the 2nd port will be in startup mode. In real life, start up mode is non-repetitive operating mode. Hence N=1.

Worst case numbers that we have for system parameters are:

Single Port Chip.

Vport max = 57V
Iport max = 0.5A peak
Emax ~ 1joule (SO-8 package)

Tc=1/(0.5*1*57V*0.5A) = 70.16mSec

Cin max is: $$Cin\max \leq \frac{Ip \cdot Tc}{Vp}$$ Eq-6.

Therefore Eq-6 yields: Cin max = 0.5A*70.16mSec/57V = 615uF

From Eq. 6 we can have 615uF instead of 50uF.

Since the above numbers are a worst case calculation, we have the following margin:
The PSE can be set to 0.4A min. (The calculation in Eq-4 was for 0.5A)
Tc max can be set to 50mSecmin (The result of Eq-4 was 70.16mS)

According to the above margin, Cin max would be: Cin max=0.4A*50mSec/57V=350uF

Multi-Port Chip

Vport max= 57V
Iport max=0.5A peak
Emax1~2.5 joules (36-pin SSOP package)
Emax2~5 joules (QFP package)

Due to the fact that in multi-port chip the Mosfets will be located around the package near the I/O pins, we can assume that the energy limit per port will be the same as the single port chip.
Hence we can turn on simultaneously 2 to 5 ports through startup mode.

We can use the above facts to use larger PD caps (>350uF) or using the same definitions suggested for single port and allow simultaneous startup mode for more than single port pending the package size.

How many margins do we have?

1. Energy limitation

   We have assumed that we are limited to 1 joule. This limitation is for SO-8 package. However, for having all the indications, controls and functions I/O we probably need 16 pin package hence more than 1 joule is allowed to be dissipated on the package.
   For 8 port device we are much above the 1-joule limitation due to the fact that we must have much larger package.

2. The calculations assumed repetitive operation with a period of T0. Actually it is non-repetitive operation hence the average power will be very low.

3. From the above calculations, we received 615uF capacitive load.
   Using the suggested numbers, results with 350uF, which is 75% margin minimum.

Suggested Specifications for Startup mode.

We can utilize the numbers that we have used for the normal powering mode and use them as a private case for the startup mode:

PSE specifications

During startup, the PSE will limit its output current to:

1. Ip min = 0.4; Ipmax = 0.45. (The max. level range of Ipeak)
2. For a current > 350mA and for time duration of 50mSec min.; 70mSec max. the PSE may/shall/must disconnect the port.
3. Time between consecutive startup mode is 1sec min. TBD max.
   (Single port insertion time will not be affected by the above parameter since it is defined for 1st time insertion and not periodically trial of single port insertions)

PD specifications

Under the above numbers of the PSE specifications, the PD will be specified as follows:

During startup, the PD allowed to consume 0.4A max. for a time duration of 50mS max.
After 50mS, the PD is restricted to the Normal Powering mode parameters.
For the above numbers, PD input capacitor should be limited to 350uF max.

The PD will limit the inrush current if larger than 350uF capacitor is used.
In this case, the peak current will be limited to be less than 0.4A.

See Annex A for the incentive to increase the capacitor value from 50uF to higher value

Annex – A. Why to increase the capacitor value from 50uF to higher value?

1. Low cost PD power supplies implementations works at 100KHZ.
   For 10-12W power supply, a max. 470uF is needed.
   For 5W power supply, a 220uF-270uF is needed.

   Capacitors lower than 50uF require a high frequency switching power supply (around 500KHZ) that costs much more.

2. 50-60% of the applications are 5-8 Watts. 30-35% are 10-12 Watts. This means that around 95% of the applications will require 220uF to 470uF.
   (Data is based on PD power requirement survey done during the last 6 months)

3. In order to meets system stability criteria as discussed over the reflector during the last 3 weeks, we need to keep low L/C ratio at the PD power supply input. Stability criteria requires that L/(ESR*C)<< Zin, L inductance, C=Capacitance of the EMI filter, ESR is the equivalent series resistance of the capacitor, Zin is the reflected PD power supply input impedance (There are additional stability criteria, however this one concerns the EMI filter connected to negative resistance network). This means that we need to allow low inductance for a given capacitor size or large capacitor for a given inductor size.
   In order to implement the EMI filter, we need the inductor to have 10-500uH (depending on topology, switching frequency and EMI requirements. In addition, we have the cable inductance which is 100uH max. as defined by the detection ad hoc draft). Therefore, larger capacitors are required.

Although (3) can be achieved when the inrush current limiting is in the PD, it will be cost effective to the system to allow for a larger capacitor in the PD. This will drive PD designers to design most of the applications with capacitors value that can utilize the PSE inrush current limiting function and reduce PD costs. For the unique applications that will require larger capacitor, adding inrush current limiter in the PD will be the best solution due to the fact that the impact on their cost will be negligible.

Worst case calculations							
	Vport	Iport	Emax	Tc/ Pulse width	Cin	N	Notes
Units	Vdc	Ap	Joule	msec	uF	Number of ports that simultaneously can be at startup mode.	
Single Port chip	57	0.5	1 (SO-8)	70.16	615	1	1. Actually may need SO-16 or eqv. 2. No need for N>1
Multi-Port chip	57	0.5	2.5 ÷ 5 (SSOP-QFP)	70.16	615	2 ÷ 5	1. Assuming Mosfets are spread around the pins 2. No need for N>1
Suggested Numbers for PSE							
	44÷57	0.4min 0.45max		50ms min			
Suggested Numbers for PD							
Cin<350uF (*) Cin<175uF (**) Cin<50uF (***)		0.4min 0.45max		50 max			Inrush C.L is in PSE
Cin>350uF (*) Cin>175uF (**) Cin>50uF (***)		0.4 max		50 max			Inrush C.L is in PD

(*) Cin=350uF requires thermal (or other type) protection in the chip to handle complete short and limiting to 1Joule.
(**) Cin=175uF doesn't requires thermal protection. After Tc the port may turn off.
(***) Cin=50uF is the preliminary number set in May/2001