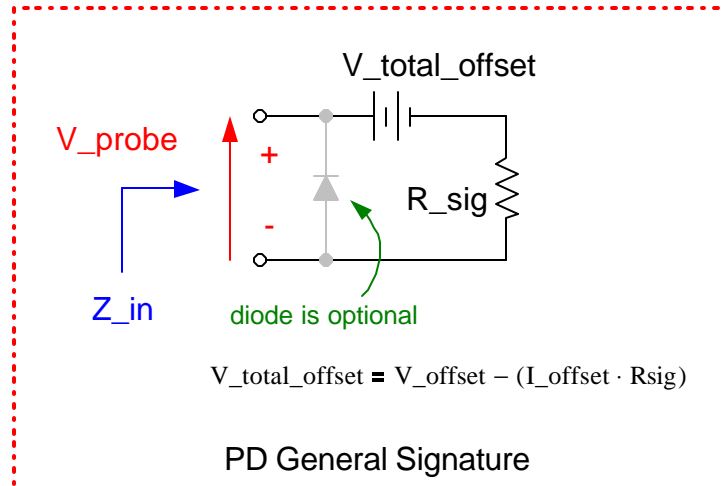


PD Signature Basic Specifications:



1.1. Valid PD Signature

1.1.1. **Discovery Probe Voltage Range (V_{probe}) driven from the PSE:**
2.8 VDC to 10 VDC with the polarity shown

1.1.2. **Valid Signature Impedance anywhere within the Discovery Probe Voltage Range with polarity shown:**

R_{sig} :	20K	minimum	25K +20%, these numbers may change
	30K	maximum	25K -20%, these numbers may change

Note that R_{sig} is defined as the slope dV/dI , with a DC bias applied anywhere within the discovery probe voltage range

C_{sig} : 150 nF maximum????

Note that C_{sig} is a combination of cable capacitance, parasitic and filter components, it is not part of the identity of the signature

L_{sig} : 1uH, maximum, or some such small number, again it is not part of the signature, but rather a parasitic effect of layout

1.2. PD Discovery and Power Polarity:

1.2.1. PSE Polarity Rule

The rule at the PSE is that the polarity of the probe voltage V_{probe} used for the discovery process must be the same as the polarity of the DTE power that is subsequently applied.

1.2.2. PD Auto Polarity

If the PD Signature resistor can be successfully detected at either polarity of probe voltage, i.e. with either a straight or a crossover cable, then the PD must be able to accept either polarity of DTE power.

This corresponds to the PD Signature (see figure above) with the back biased diode omitted. In this case, a bridge rectifier must be employed after the signature circuit in order to insure that either polarity will operate correctly.

1.2.3. PD Fixed Polarity

If the PD Signature resistor can only be successfully detected with a straight cable, which corresponds to the polarity as shown above, then the PD need only to accept that polarity of DTE power.

This corresponds to the PD Signature (see figure above) with the back biased diode included. In this case, the discovery will only be successful with the correct straight cable employed, and the probe voltage and DTE power polarity will be as shown above.

1.3. PD Offset:

1.3.1. PSE Total Offset Voltage Range

The total offset voltage, $V_{\text{total_offset}}$, includes both voltage offset from diodes, etc..., as well as the current offsets from constant leakage effects.

$V_{\text{total_offset}}$	2V	positive maximum value
	-0.5V	negative maximum value

where $V_{\text{total_offset}}$ is calculated as follows:

$$V_{\text{total_positive_offset}} = V_{\text{max_offset}} - (I_{\text{max_neg_offset}} \cdot R_{\text{sig_max}})$$

and

$$V_{\text{total_negative_offset}} = -(I_{\text{max_pos_offset}} \cdot R_{\text{sig_max}})$$