

IEEE 802.3af DTE Power via MDI PSE-PD Inter-operate - Stability Analysis

Presented by Yair Darshan, PowerDsine
yaird@powersine.com



Objectives

- Specify the requirements to ensure PSE - PD stability at Normal Powering Mode

- Strategy

- Using Impedance Design Criteria
 - Specify PD input impedance without input filter
 - Specify PD input filter output impedance
 - Specify PSE power supply output impedance



System Description at Normal Powering Mode

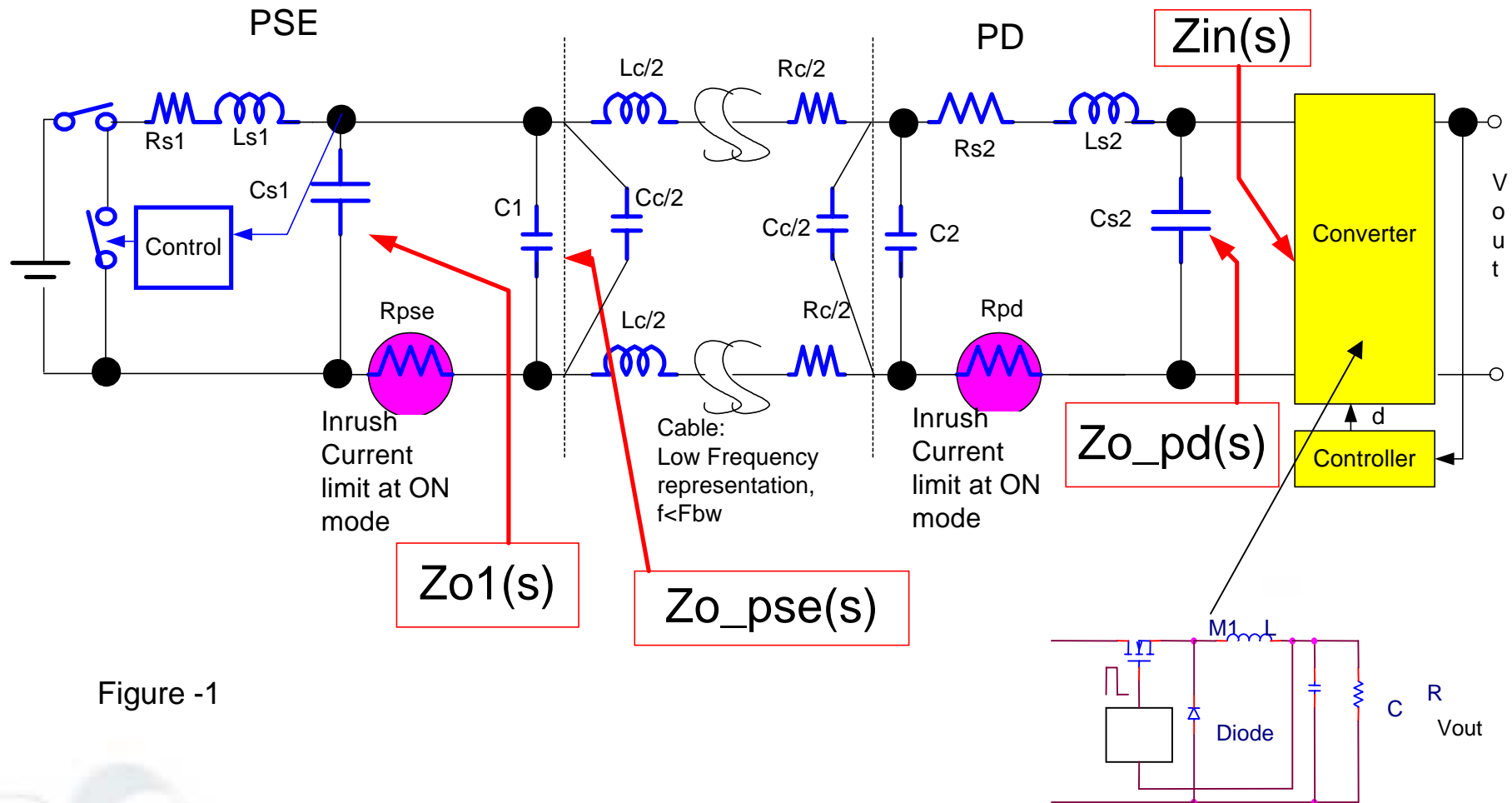
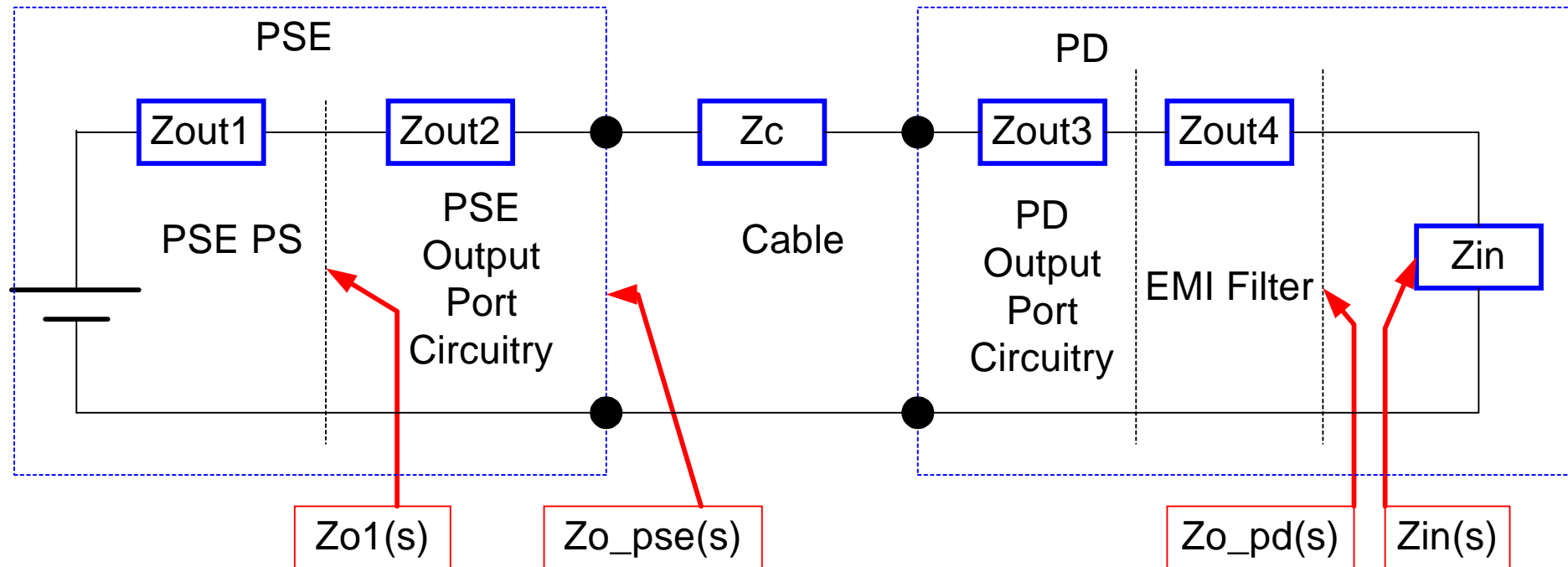


Figure -1



Simplified System at Normal Powering Mode



Problem Definition

- Under Specific Combinations of PSE output impedance and PD input Impedance
 - PSE - PD stability at Normal Powering Mode may be impaired
 - PD Power Supply Dynamic Performance will be changed

The reason:

- PD Power Supply Close Loop Transfer Function
May be Impaired if Additional Frequency Dependent Elements are Connected From the Power Source (PSE) to the Load (PD's DC/DC converter)



List of Possible Stability Problems

- At specific frequency the source Output Impedance will increase to a level that PD input voltage will drop below UVLO level.
 - Startup Problems
 - Stability Problems during Load Changes
- Due to impairment of the PD PS Open Loop Transfer Function, marginal stability at small signal is expected



Proposed Strategy - Worst Case Analysis

Pros

- Shortest way to get results
- Solves PSE-PD inter-operate problem
- Simple design rules for PD and PSE

Cons

- Required large design margin compared to case when PSE-PD system is designed by the same vendor.



Worst Case Analysis Assumptions

- Cable length = 0 (Cable length =100m effects is discussed in (5))
 - Higher Quality Factor of the LC filters

- Inrush Current Limiter In PSE and PD is ON.
 - Series Switch Resistance =0 (Higher Quality Factor of the LC filters)

- PSE contains LC filter at its output

- PD contains LC filter at its input

- PD DC/DC converter control method is Voltage Mode
 - Current Mode Control is easier case^(3,4)



Analysis Information

- Low frequency analysis , $f < 0.5F_s$. $F_s = \text{Converter Switching Frequency}$.
 - $F_s = 100\text{KHz}$ was used as a typical case.
- Cable is modeled as low frequency device
- System is at Normal Powering Mode
 - PD converter short circuit condition at output is ignored.
- PD:Full Load = 12.95W average at its input
- Min Load = 10mA

- Typical results were simulated by the system model elements presented in July 2001. The control scheme was modified to voltage mode control.



Design Criteria

- To keep PSE-PD system stable, we need to keep PD stable at the following design options (See Figure 1 and Annex A):
 - 1. PD with its EMI filter. Meeting $|Z_{o_pd}| \ll |Z_{in}|$ (See Annex A for Z_{in} details)
 - Cable length=0, $R_{pse}=0$, $R_{pd}=0$
 - PSE source without output filter
 - 2. PD with PSE PS output filter. $|Z_{o_pse}| \ll |Z_{in}|$
 - Cable length=0, $R_{pse}=0$, $R_{pd}=0$, $C1=0$, $C2=0$.
 - PD converter without input filter
 - 3. PD with PSE output filter and PD input filter. $|Z_{o_pd}| \ll |Z_{in}|$
 - Cable length=0, $R_{pse}=0$, $R_{pd}=0$, $C1=0$, $C2=0$.



PSE Power Supply Output Impedance - Z_{o1}
-Connected to resistive load (Min load= 10% of Full Load)
-Control method: Voltage Mode

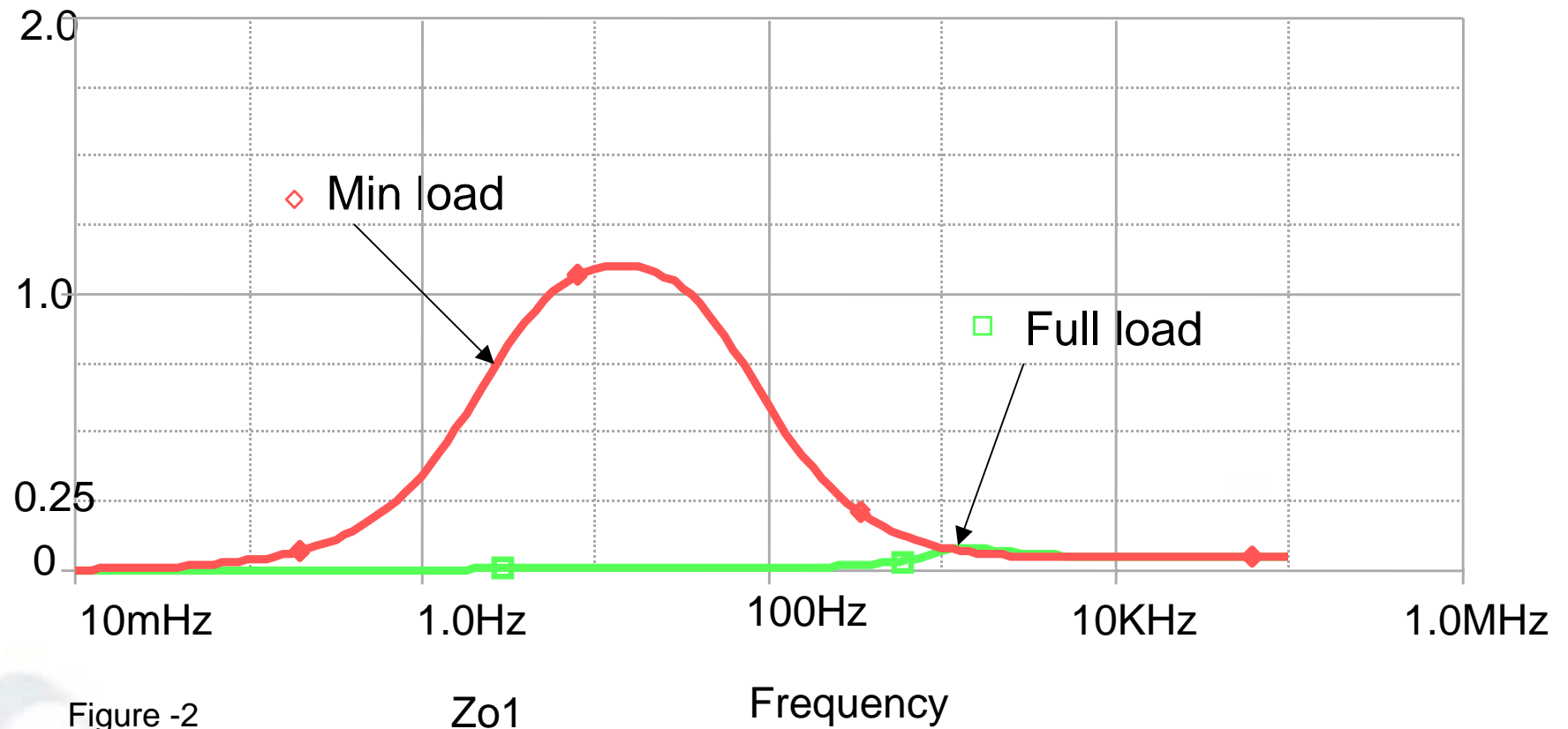


Figure -2

Z_{o1}

Frequency



PD Converter Input Impedance - $Z_i(f)$ at full load (12.95W,37V)

- Without input filter effect
- With zero output impedance DC source.
- Control method: Voltage Mode,

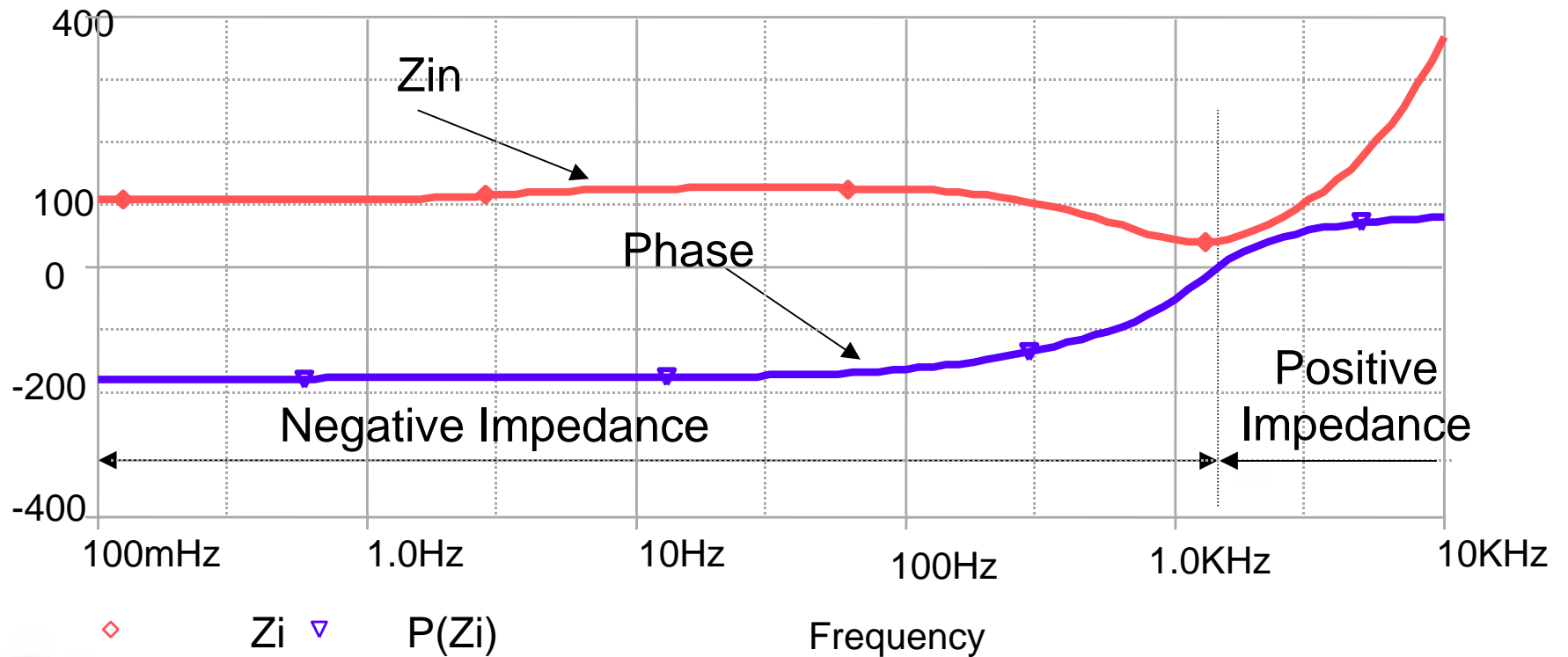
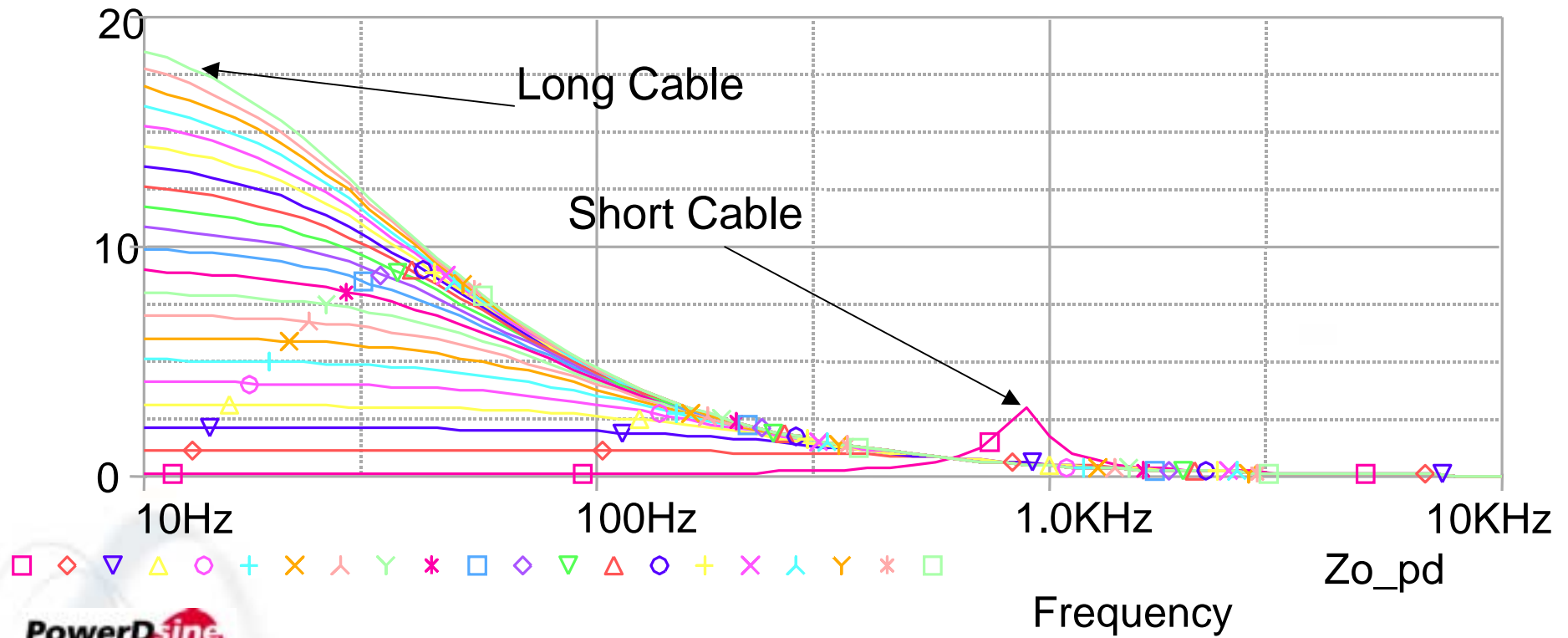
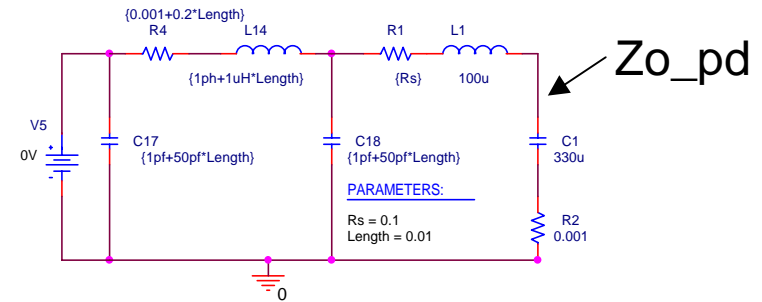


Figure -3



PD EMI Filter output impedance, Zo_pd vs. cable length.

EMI Filter: $L=100\mu H$, $C=330\mu F$, $R_s=0.1\ \Omega$



PD DC/DC Converter Open Loop Transfer Function

- Without input filter effect
- With zero output impedance DC source.
- Control method: Voltage Mode

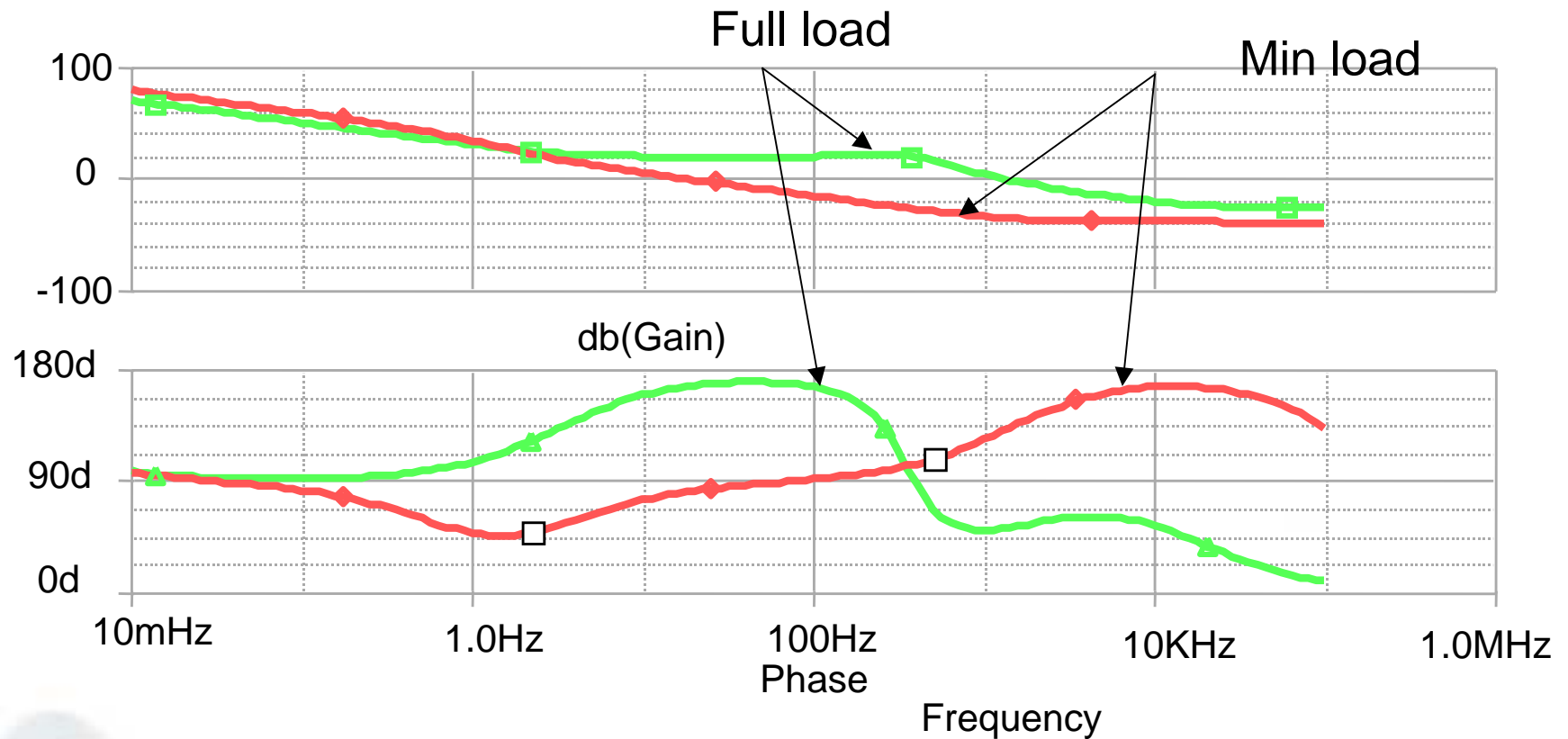
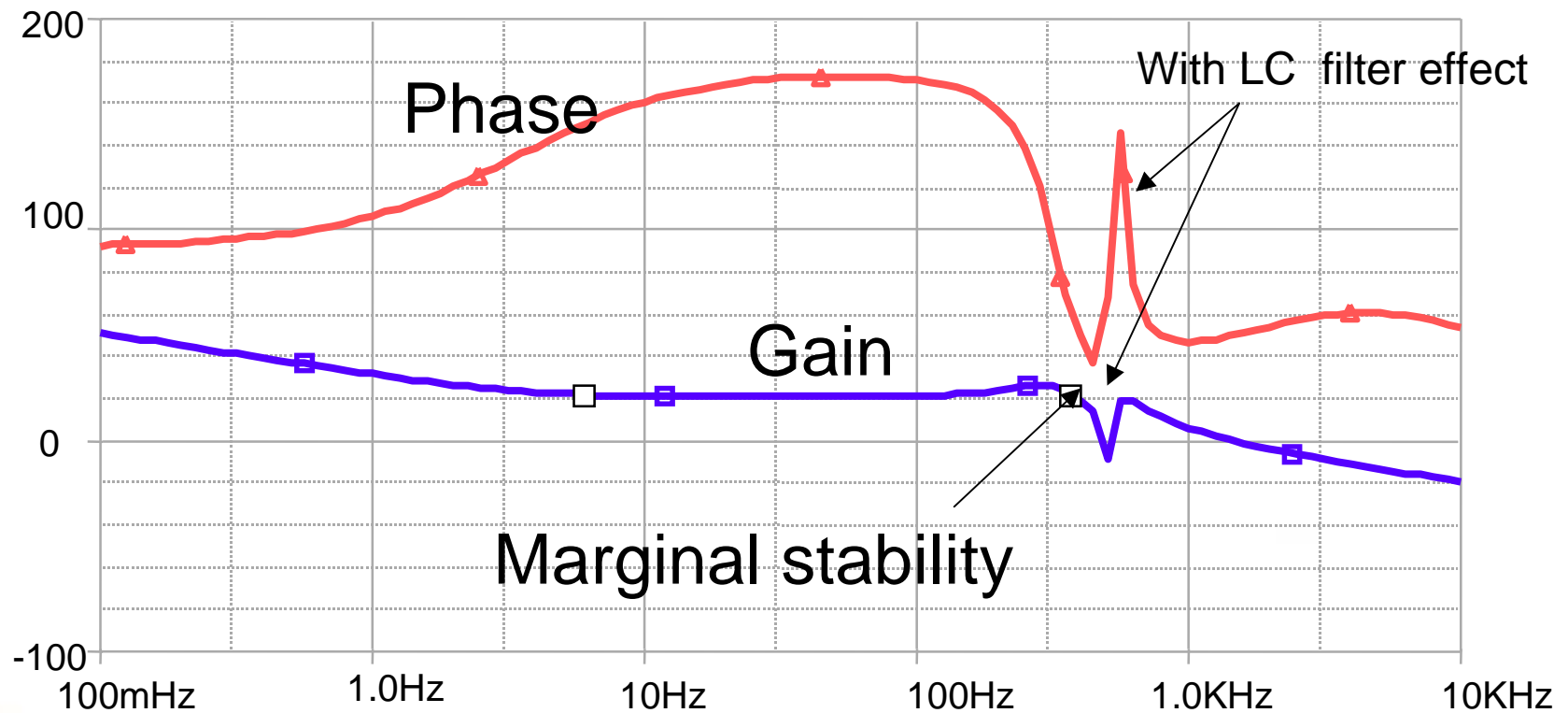


Figure -4



PD DC/DC Converter Open Loop Transfer Function

- With LC filter effect, Full load
- Control method: Voltage Mode



△ $P(V_{out}/V_c)$
 □ $db(V_{out}/V_c)$ Frequency



Impedance Allocation Map Measured from PSE PS to PD DC/DC converter input

Z_{in}, Z_o, Z_{o1}

$$R_a = \frac{(44V - 0.35A \cdot 20\Omega)}{0.35A} = 105.7\Omega$$

$$R_p = \frac{(44V - 0.4A \cdot 20\Omega)}{0.4A} = 90\Omega$$

$$Z_{in_min} = \frac{R_p}{3} = 30\Omega$$

(to allow design margin for PD
DC/DC output filter (L,C,R) effects)

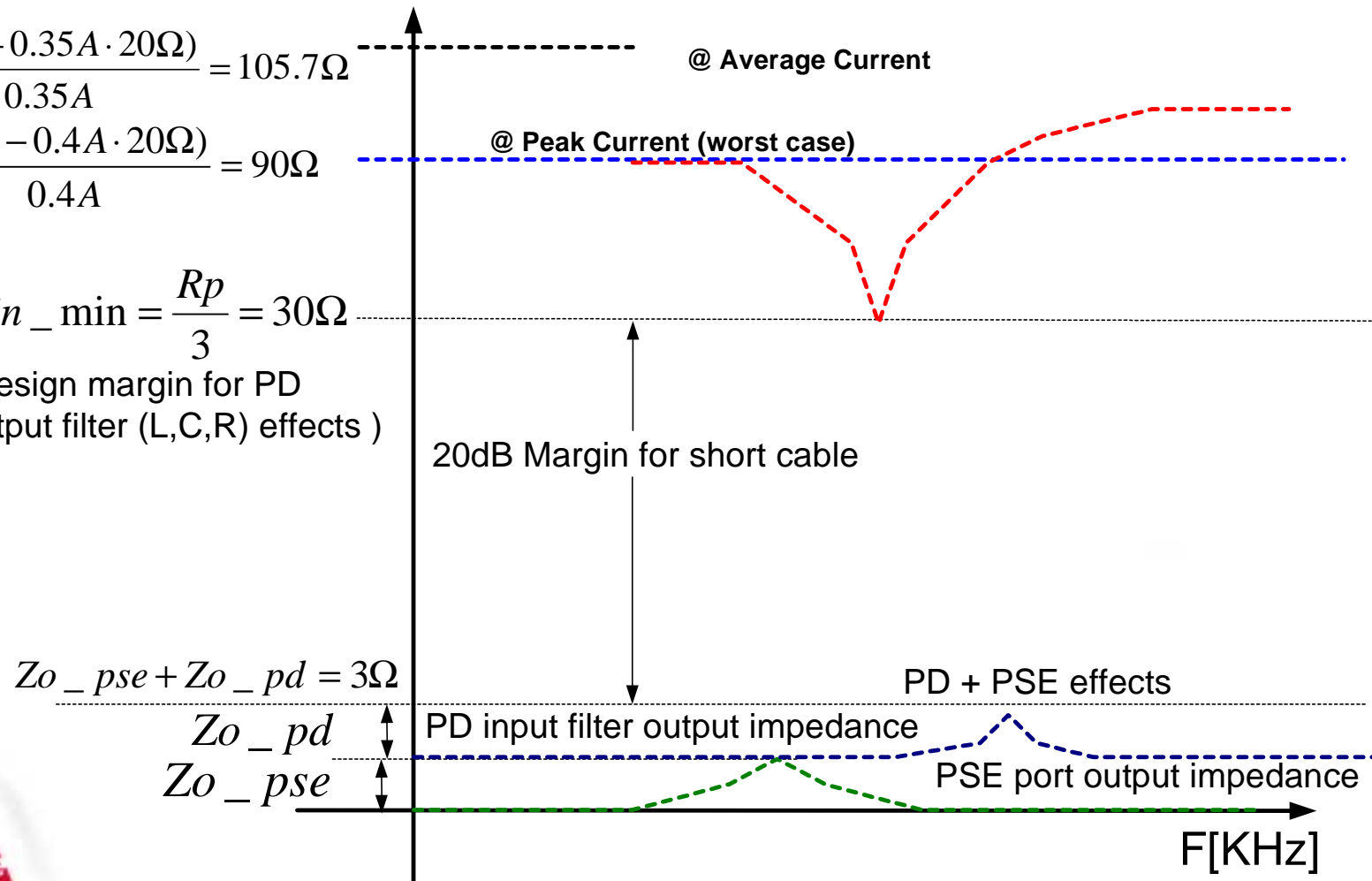


Figure -5

PowerDsine

Impedance Allocation Map Measured from PSE Port to PD DC/DC converter input

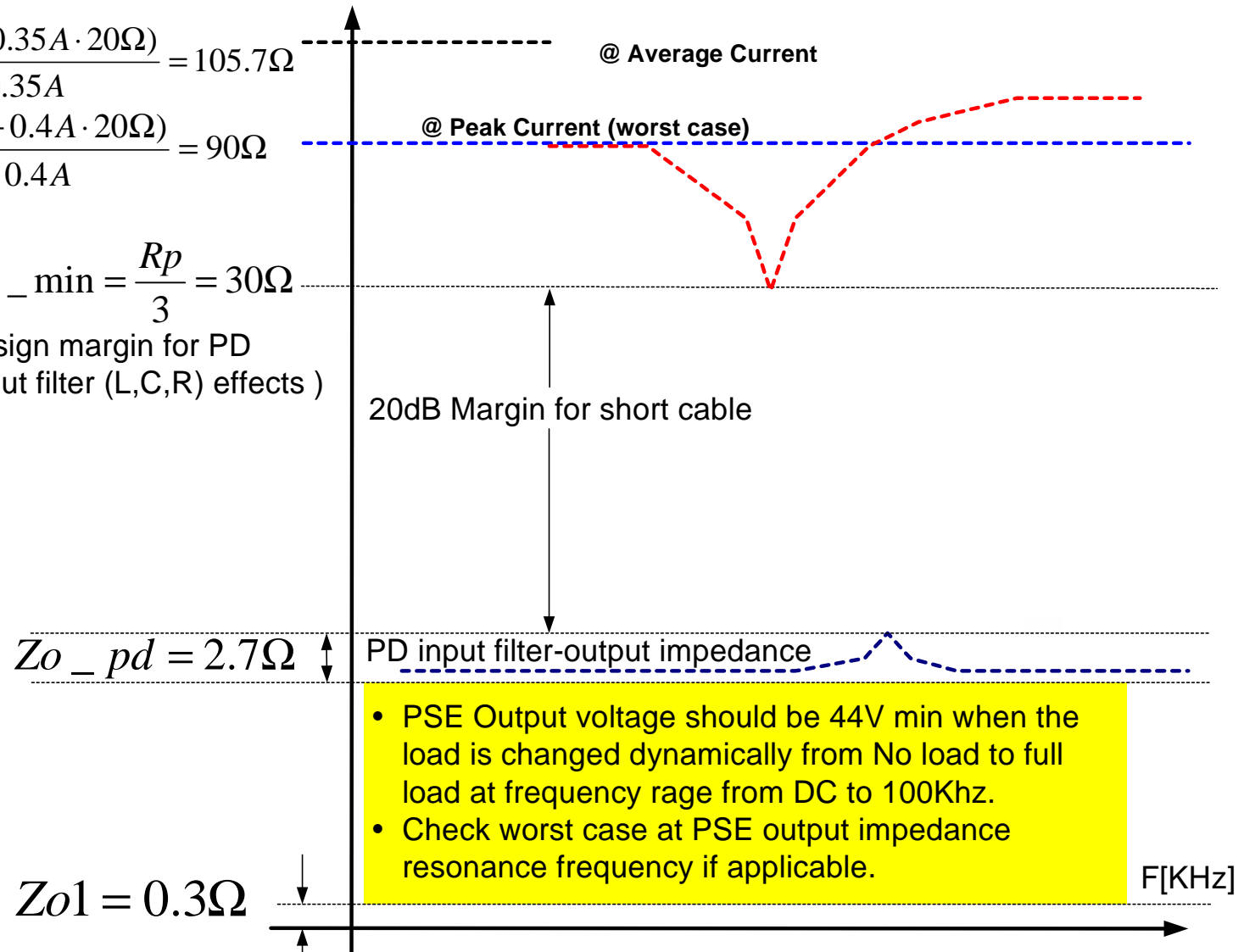
Z_{in} , Z_o , Z_{o1}

$$R_a = \frac{(44V - 0.35A \cdot 20\Omega)}{0.35A} = 105.7\Omega$$

$$R_p = \frac{(44V - 0.4A \cdot 20\Omega)}{0.4A} = 90\Omega$$

$$Z_{in_min} = \frac{R_p}{3} = 30\Omega$$

(to allow design margin for PD DC/DC output filter (L,C,R) effects)



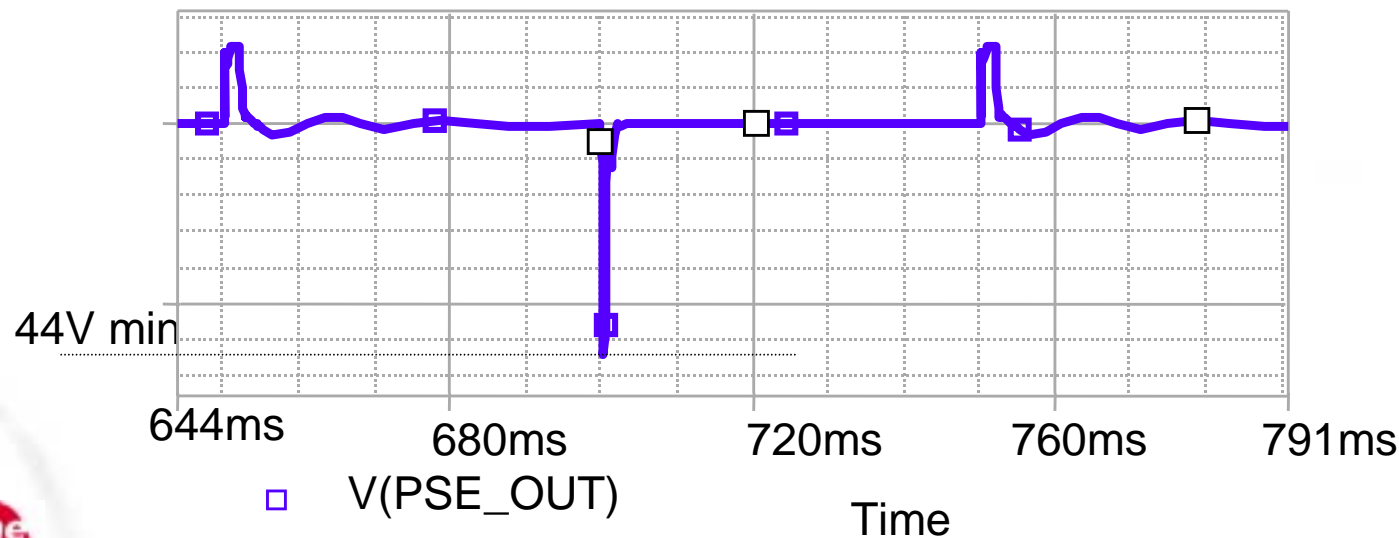
Proposed Requirements for PD

- PD converter input EMI filter or Cable inductance followed by capacitor
 - PD designer will ensure stable operation of its DC/DC converter in a presence of an input filter powered through short cable (<1m) and long cable (>100m).
 - Input filter cutoff frequency \ll Averaging LC filter cutoff frequency. (See Annex A)
 - The absolute value of the filter output impedance (Z_{o_pd}) will not exceed 2.7Ω with short cable (<1m) for $P_{max}=12.95W$ assuming PSE output impedance $<0.1\Omega$.
 - For $P_{max} < 12.95W$, Z_{o_pd} min will be $Z_{o_pd} = 2.7\Omega * 12.95 / P_{max}$.
- PD converter input impedance (without input-filter output impedance effect), Z_{in}
 - PD converter input impedance (Z_{in}) will be 30Ω min at max. load condition, P_{max} . (12.95W avg, 14.8W peak)
 - For loads $P_{max} < 12.95W$, Z_{in_min} will be $Z_{in_min} = 30\Omega * 12.95 / P_{max}$.
- All the above requirements should be met well above Fbw.
- Fbw=DC/DC converter closed loop cross over frequency.

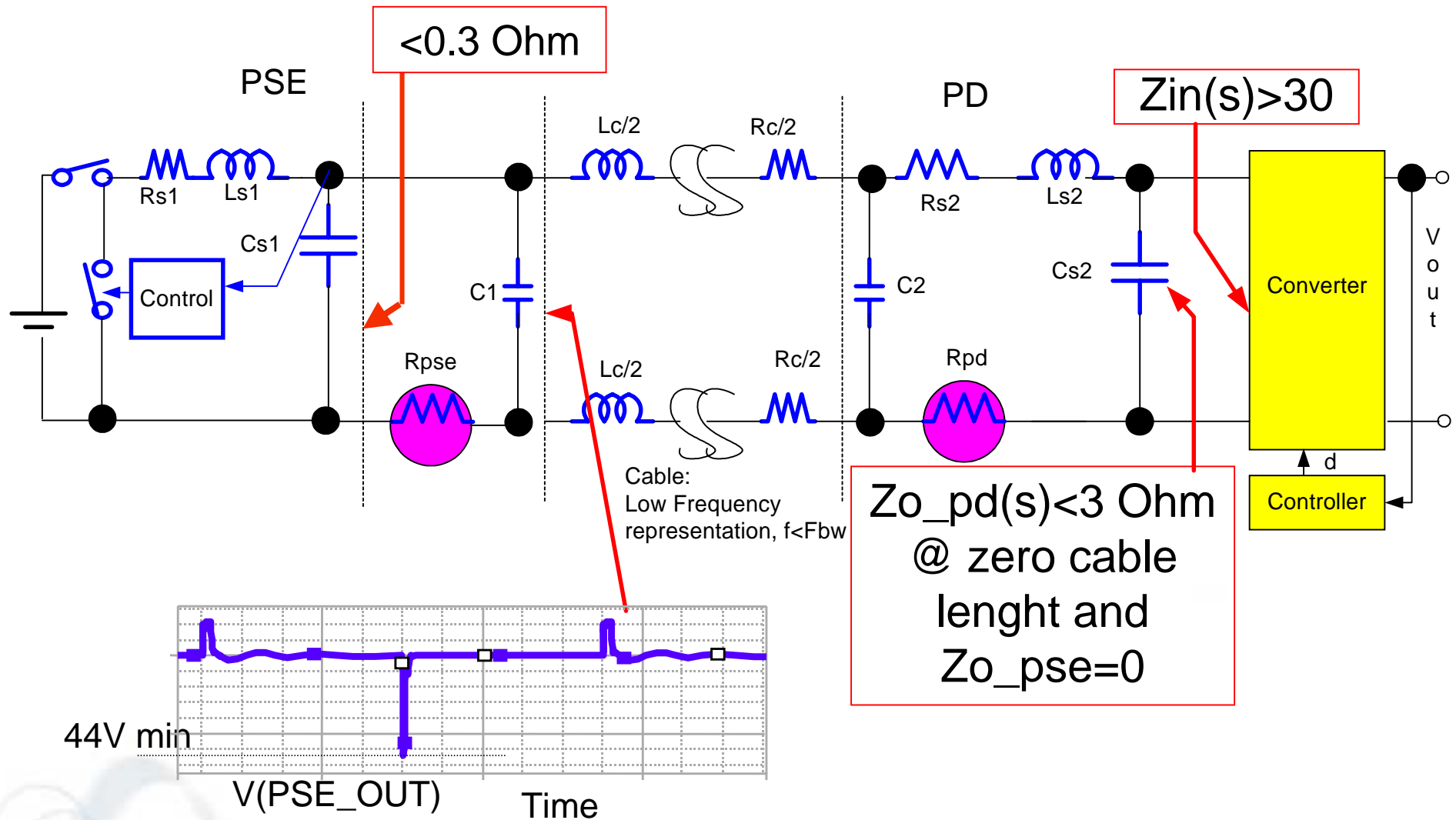


Proposed Requirements for PSE Output Port

- PSE PS output impedance (Z_{o1}) shall be 0.3Ω max from DC to 100KHz at full load ($P_{max}=15.4W$).
 - For $P_{max}<15.4W$, $Z_{o1}= 0.3\Omega * 15.4/ P_{max}$
- PSE Port Output voltage should be 44V min when the load is changed dynamically from No Load to Full Load at frequency range from DC to 100KHz. (Compensating for R_{pse})
- Check worst case at PSE output port impedance resonance frequency if applicable.



Proposed Requirements for PSE and PD - Summary



What's next?

Recommendations to IEEE802.3af group:

- PD and PSE requirements should be used as design guidelines.
- If easy test set-up is found to confirm the requirements at PORT level, it can be used as a requirement.
 - To be discussed with the group for the best option.



Annex A - Design Criteria

- Converter operating mode:
 - Continuous Current Conduction mode. Direct duty cycle control (voltage mode control).
- D = PWM controller duty cycle
- $D_{off} = 1 - D$
- R = Converter output load
- L = Converter Integrating Inductance
- C = Converter output capacitance
- $G_{vd}(s)$ = DC/DC converter transfer function from output to control variable, d .
- $Z_N(s) = Z_{in}(s) @ \frac{d(V_{out})}{dt} = 0$
- $Z_D(s) = Z_{in}(s) @ \frac{d(D)}{dt} = 0$
- $Z_e(s) = Z_{in}(s) @$ Converter output is shorted. (Not required to keep stability. It is required to keep converter output impedance unaffected by the presence of an input filter.)



Annex A - Design Criteria cont.

- Worst case analysis
 - Cable length = 0
 - $R_{pse}=0$
 - $R_{pd}=0$
- To keep PD converter control transfer function unaffected by the input filter and its associated circuits, the following inequalities should be met (2):

$$G_{vd}(s) = (G_{vd}(s)|_{Z_{o_pd}(s) \rightarrow 0}) \cdot \left(\frac{1 + \frac{Z_{o_pd}(s)}{Z_n(s)}}{1 + \frac{Z_{o_pd}(s)}{Z_d(s)}} \right)$$

- Hence, the following inequalities should be met:
- $|Z_{o_pd}(s)| \ll |Z_N(s)|$
- $|Z_{o_pd}(s)| \ll |Z_D(s)|$



Annex A - Design Criteria cont.

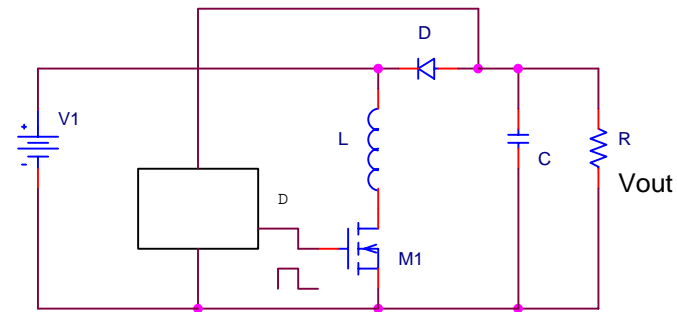
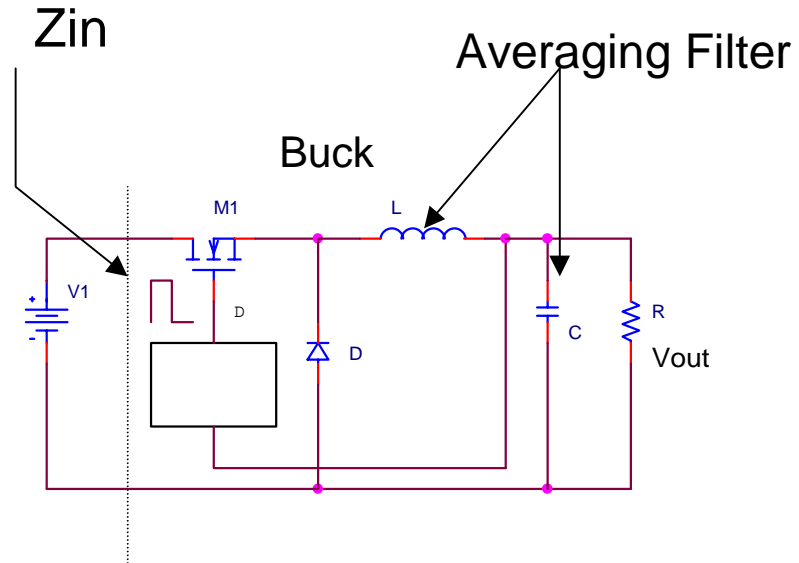
Converter	$Z_N(s)$	$Z_D(s)$	$Z_E(s)$
Buck	$\frac{-R}{D^2}$	$\frac{R \left(1 + s \frac{L}{R} + s^2 LC \right)}{D^2 (1 + sRC)}$	$\frac{sL}{D^2}$
Boost	$-D_{off}^2 \cdot R \left(1 - s \frac{L}{D_{off}^2 R} \right)$	$\frac{D_{off}^2 R \left(1 + s \frac{L}{D_{off}^2 R} + \frac{s^2 LC}{D_{off}^2} \right)}{(1 + sRC)}$	sL
Buck-Boost (Flyback)	$-R \frac{D_{off}^2}{D^2} \left(1 - s \frac{D \cdot L}{D_{off}^2 R} \right)$	$\frac{D_{off}^2 R \cdot \left(1 + s \frac{L}{D_{off}^2 R} + \frac{s^2 LC}{D_{off}^2} \right)}{D^2 (1 + sRC)}$	$\frac{sL}{D^2}$

Analytical expressions for Z_n , Z_d , Z_e .

Design Requirement: Plot Z_n , Z_d , Z_e as function of frequency vs. Z_{o_pd} and keep $Z_{o_pd} \ll Z_n, Z_d, Z_e$ values.



Annex A - Design Criteria cont.



Buck-Boost (Flyback)

(Can be implemented with coupled inductor to have positive output)

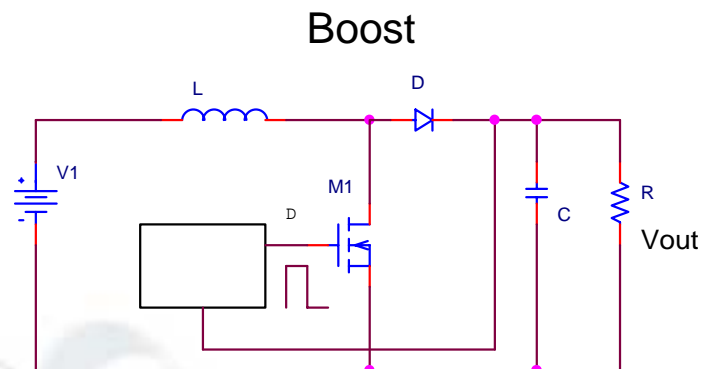


Figure -7

References

- (1) R.D. Middlebrook, Slobodan C'uk , “Input filter considerations in design and application of switching regulator” Advances in Switched-Mode Power Conversion Volumes 1 and 2, Pp. 91-107.
- (2) Robert W. Erickson, Dragan Maksimovic', Fundamentals of Power Electronic 2nd edition pp 377-405, 843-861
- (3) Sandra Y. Erich and William M. Pollvka, “Input Filter Design for Current-Programmed Regulators” IEEE 1990.
- (4) Yungteak Jang and Robert W. Erickson. “Physical Origins of Input Filter Oscillations in Current Programmed Converters” 1991 IEEE Applied Power Electronics Conference.
- (5) Yair Darshan, “IEEE 802.3af Remote Powering Considerations” presented at May 2000 Interim.

