10GBASE-T *PAM5* Line Signaling

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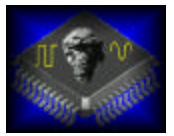
PAM signal requirement at BER = 10^{-12}

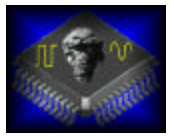


Line Code	bits/Baud	Signal bandwidth (MHz)	Baud rate (MS/s)	Detection SNR (dB)
PAM4	2	780	1560	24.00
PAM5	2	625	1250	26.05
PAM8	3	500	1000	30.24
PAM10	3	416	833	32.21
PAM12	4	405	810	33.81

$$\mathbf{SNR = 6\log_2(M) + Gap - Coding\_Gain + Margin}$$

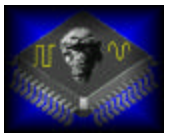
Gap = 12.25dB Coding_Gain = 6dB Margin = 6dB

Channel Capacity for BW=625 MHz



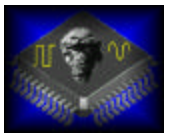
	Capacity (Gbps) Power = 7 dBm NEXTcanc=50 ECHOcanc=65 FEXTcanc=50	Capacity (Gbps) Power = 8 dBm NEXTcanc=40 ECHOcanc=60 FEXTcanc=30	Capacity (Gbps) Power = 7 dBm NEXTcanc=40 ECHOcanc=60 FEXTcanc=30
Model #1	17.31	17.26	17.19
Model #2	18.38	18.38	18.37
Model #3	16.90	16.83	16.74

Transmitter Assumptions for Stated Performance



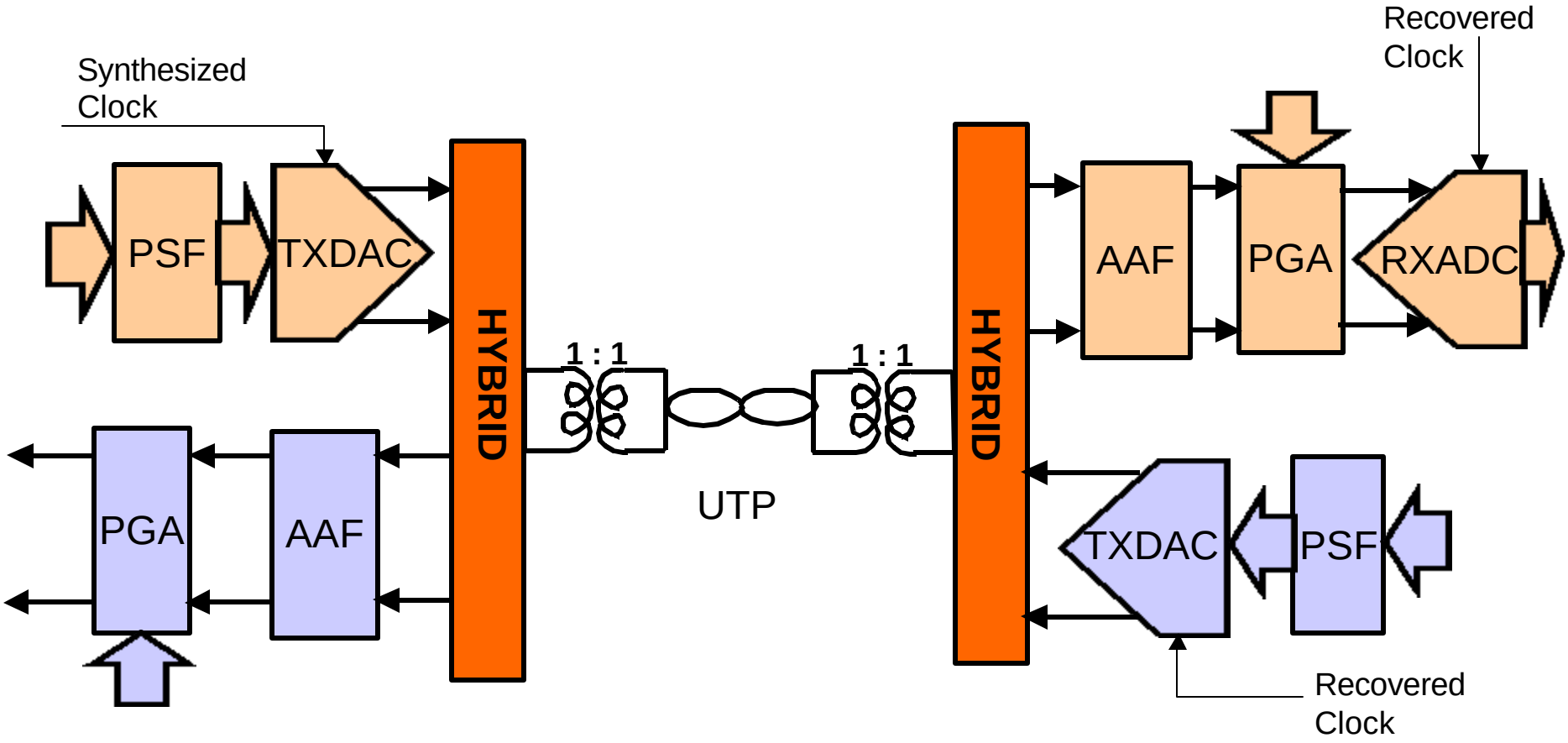
Modulation	PAM5
FEC Code	TCM
Symbol Rate	1250 MS/s
Transmitter Equalization	POSSIBLE
Digital Transmit Filter	YES (1000BASE-T like)
Assumed DAC resolution	10-bit
Assumed DAC speed	1250 MHz
Analog transmit filter	YES (Critically damped 2nd order at 625 MHz)
Max transmit launch voltage (differential)	$2V_{pp}$
Transmit peak voltage	1V

Receiver Assumptions for Stated Performance



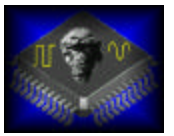
Assumed ECHO suppression	65 dB
Assumed ECHO canceller length (assumes no echo cancellation prior to ADC)	760
Assumed NEXT canceller length	180
Assumed FEXT canceller length	80
Assumed equalization approach & parameters	DFE + FEC
Assumed ideal ADC speed	1250 MS/s
Min required resolution of ADC	7-bit
How much echo cancellation required prior to ADC?	20 dB
Assumed additive Gaussian noise of receiver	-150 dBm/Hz
Assumed analog receive filter prior to ADC	4^{th} order
Maximum voltage on PHY side of transformer	$5V_{pp}$

Analog Front End (AFE) model for DSP Solution



AAF can also provide partial equalization/cancellation in analog

Assumptions for AFE Linearity Analysis



- 2 V_p peak-to-peak PAM-M launch signal
- Analog differential blocks have only odd non-linearity
- Analog blocks are characterized by:

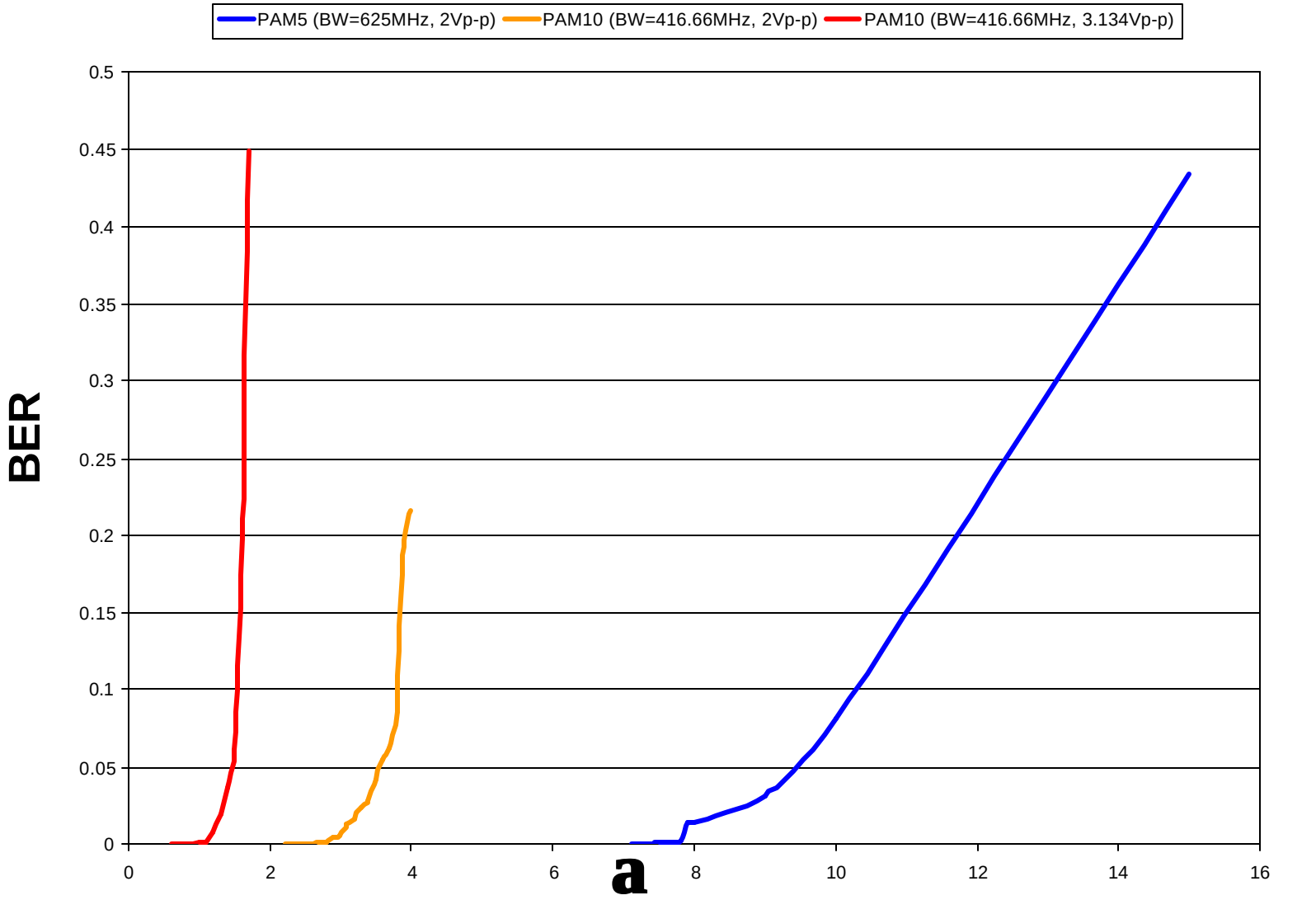
$$Y = \mathbf{b}X(1+\mathbf{a}X^2)$$

- **b** block gain
- **a** 3rd order non-linearity coefficient

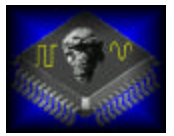
AFE Linearity Requirement (Normalized) vs. Line-Signal

Line Code	Peak-to-Peak (V)	Launch Power (dBm)	|a| (%)
PAM-5 (Plato Labs)	2.000	7.00	6.90
PAM-10 (Solar Flare)	3.134	10.00	1.00
PAM-10 (MRVL/BRCM)	2.000	6.10	2.41
PAM-17 (Cicada 1/00)	2.000	5.74	1.30

BER vs Non-linearity



Non-linearity Analysis Conclusions



- For a given PAM-M line-signal the 3rd order non-linearity coefficient (**a**) inversely depends on M and *square* of peak launch signal
- Smaller the **a** higher the AFE complexity (area and power)
- 3.134V_{p-p} PAM-10 line-signal requires AFEs that are 5.7X more linear than that of 2V_{p-p} PAM-5
- Let's maintain 2V_{p-p} launch voltage (used in 100BASE-T and 1000BASE-T)
- Let's maintain PAM-5 line-signal (used in 100BASE-T2 and 1000BASE-T)

AFE Power & SNDR

The power consumption according to (65nm CMOS):

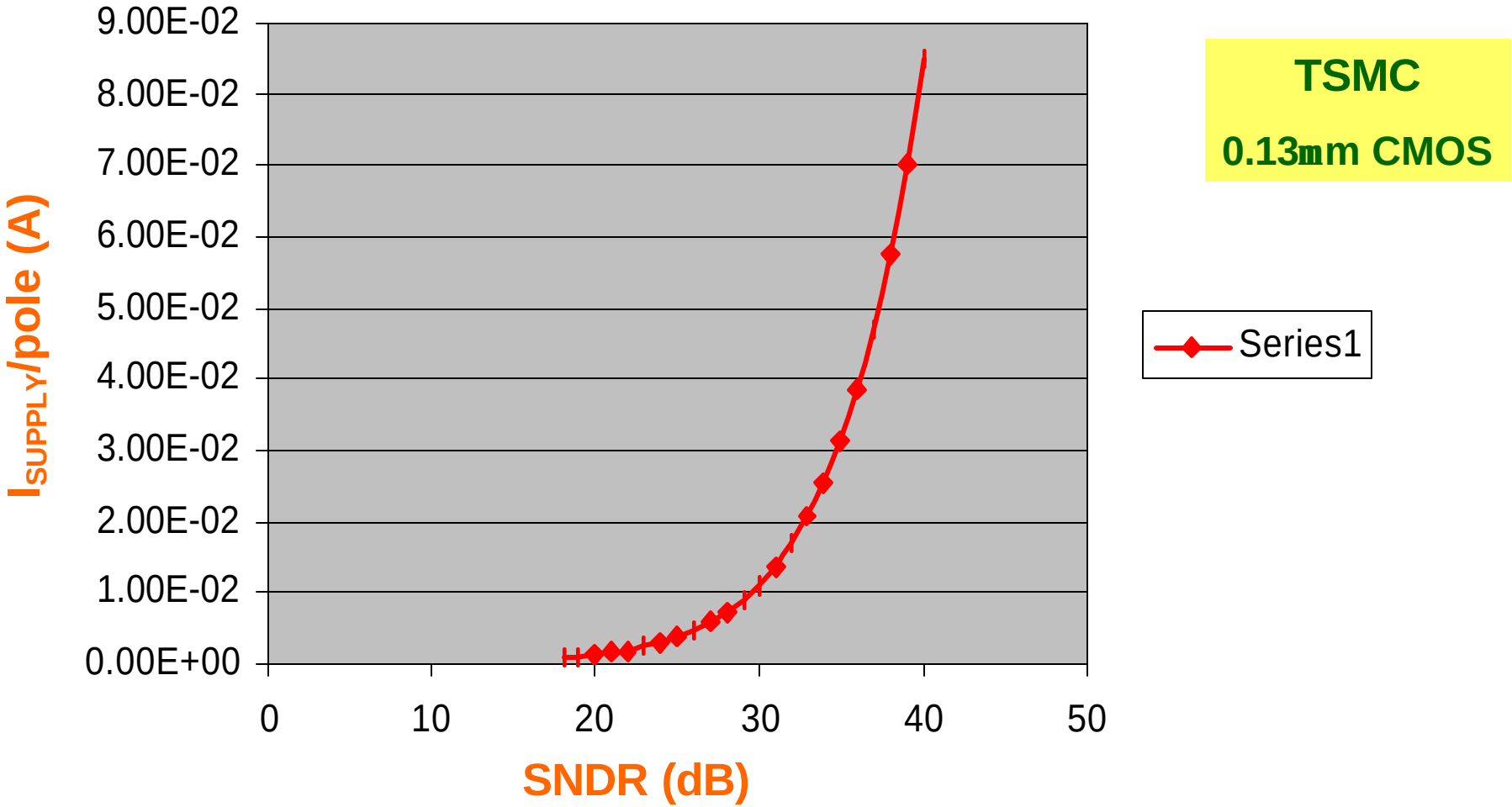
http://www.ieee802.org/3/10GBT/public/nov03/10GBASE-T_tutorial.pdf

$$P_{TOTAL}=8\text{-}16W\ (AFE)+2.2W\ (DSP)=10\text{-}18W$$

AFE power is related to its SNDR

$$SNR^2=\frac{S^2}{N^2_{AFE}+D^2_{AFE}+SR^2_{impairment}}$$

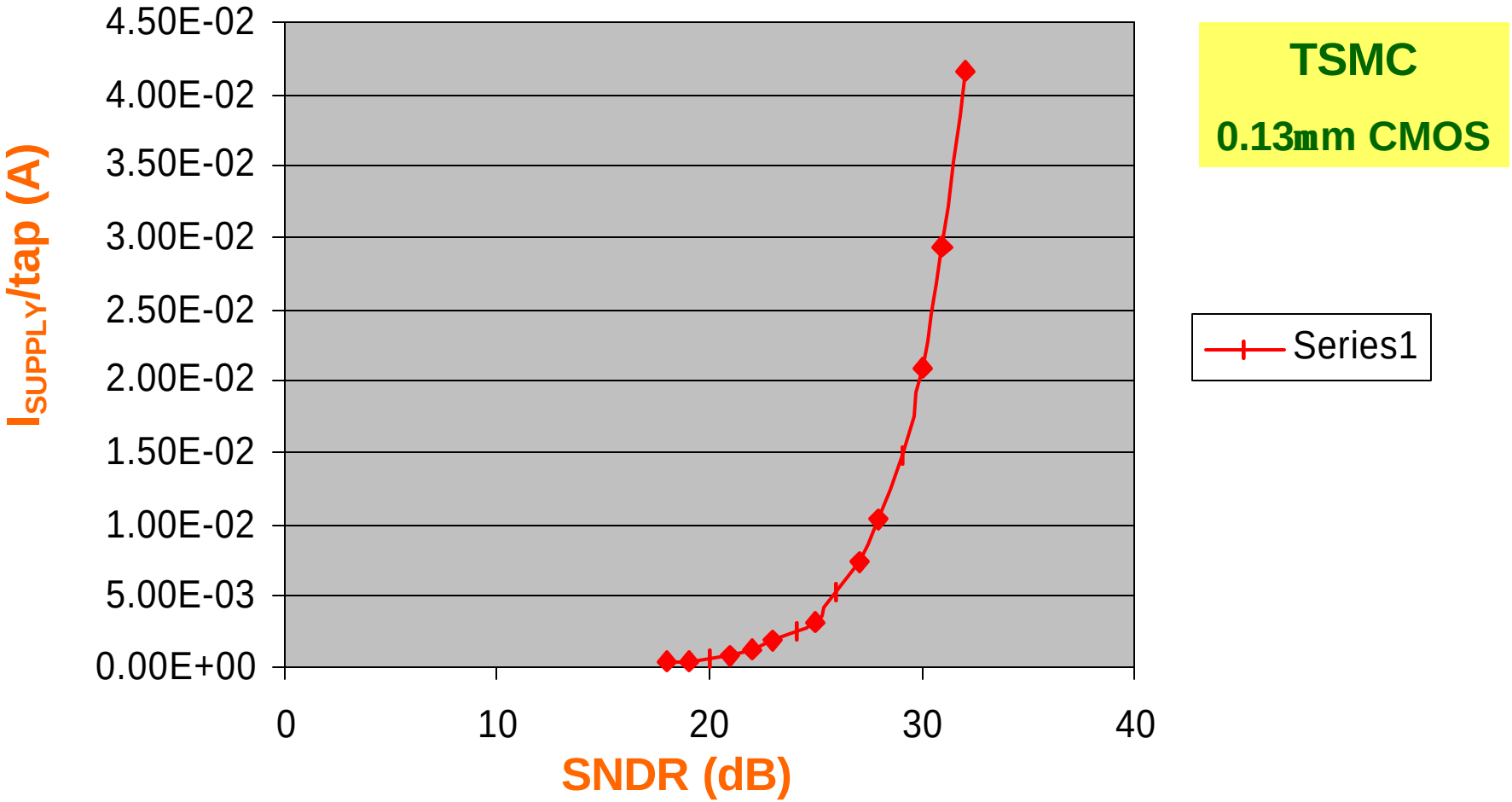
Supply Current vs. SNDR for a g_m-C Biquad Filter [1]



TSMC

0.13mm CMOS

Supply Current/tap vs. SNDR for a Rotating MUX Analog Equalizer/Canceller [2]



Examples of Prior Art

Block	*Process*	*Key Spec.*	*Power*
170 Mb/s analog FIR equalizer [2]	1.2mm	SNR=22.1dB(PR4) SNR=25.8dB(EPR4)	70 mW
10-bit, 1GS/s Current-Steering CMOS DAC [4]	0.35mm	INL<0.2LSB DNL<0.15LSB	110 mW
Continuous-time 7th order, g_m-C filter [5]	0.25mm	THD=1%@455mV$_{pp}$ BW= 30-100 MHz	210 mW
8-bit, 1.6GS/s folding CMOS ADC [6]	0.18mm	ENOB=7.26-bit@800MHz	1.27 W

Power Consumption of an OTA in Different CMOS Processes With Constant SNDR [3]

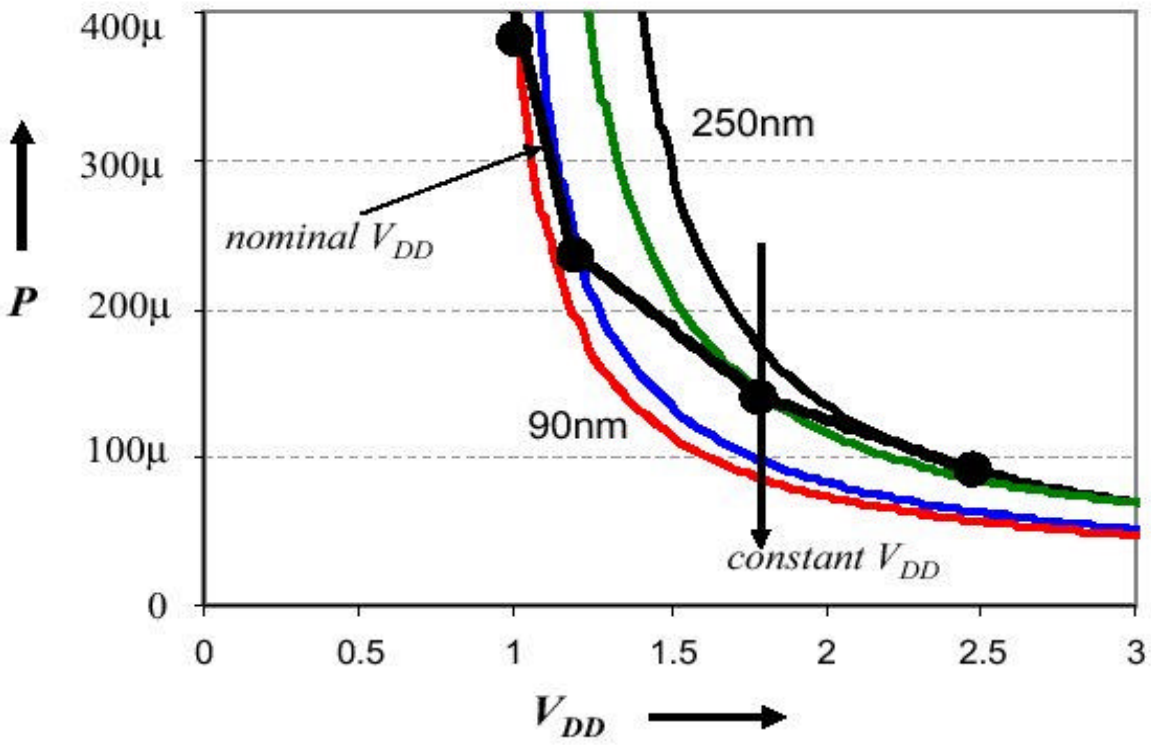
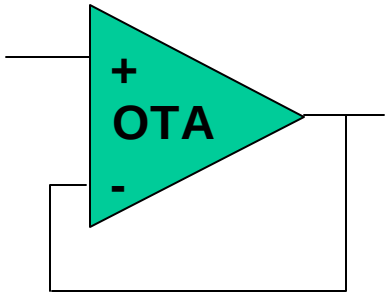


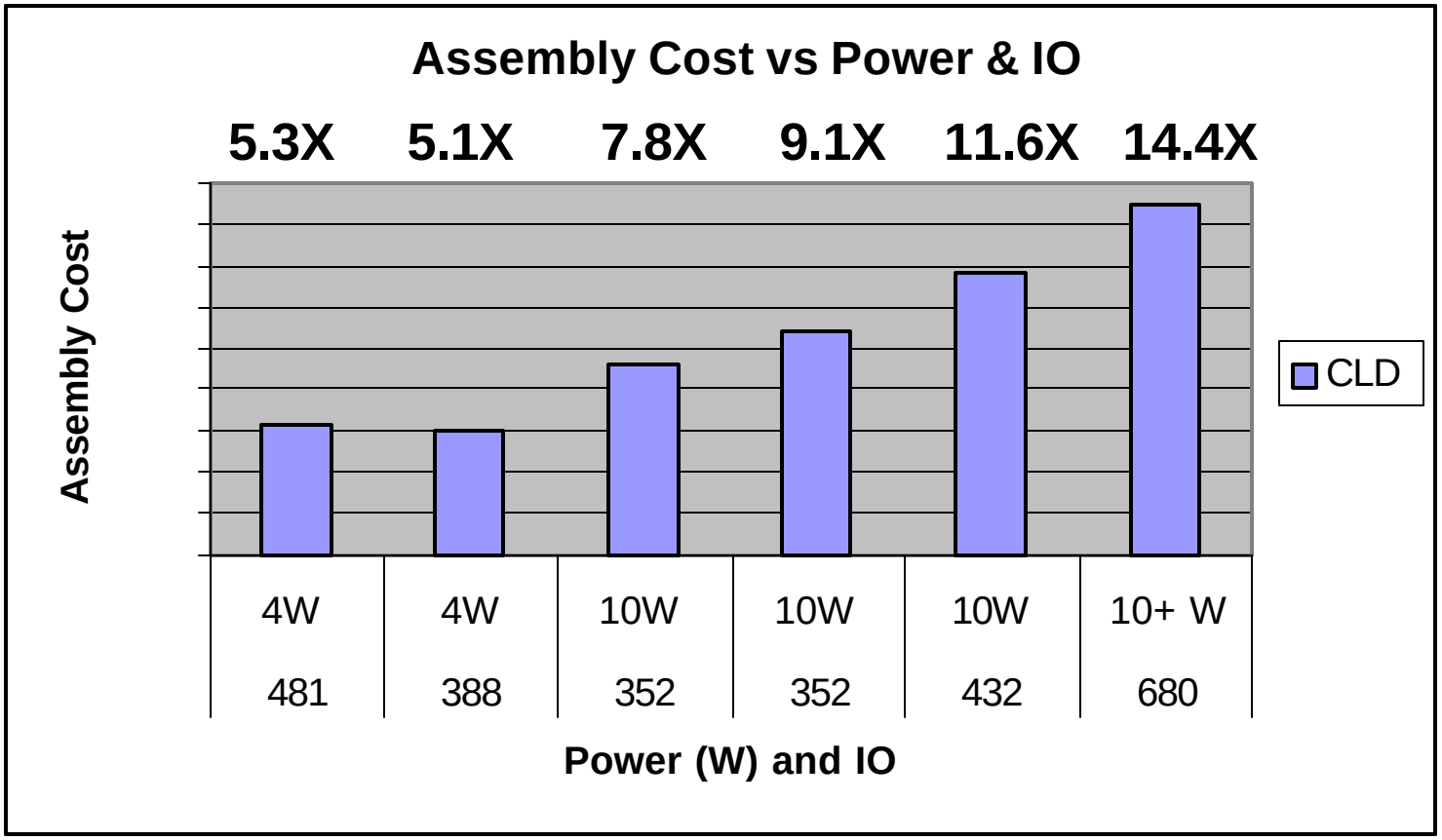
Figure 1: Simulated typical Vdd-P relation for analog circuits: fixed topology, optimized settings, 60dB SINAD @ 15MHz; in 90, 120, 180 and 250nm CMOS. Reliability issues ignored for comparison reasons.

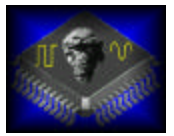


OTA: The most common analog building block

Process migration does not *necessarily* result in lower power for AFE

Assembly Cost vs. 1000BASE-T PHY Package





Implementation Feasibility

- 10Gb/s over provided channel models
- Single-chip CMOS implementation (0.13μm)
- PAM5 line-signaling
- $2V_{pp}$ launch voltage
- Low-power implementation
- Interface to MAC via XGMII

References

[1] Y. P. Tsividis and J. O. Voorman, *Integrated Continuous-Time Filters*, IEEE PRESS 1992, pp.3-14

[2] X. Wang and R. R. Spencer, "A low-power 170-MHz disctrete-time analog FIR filter," IEEE *JSSC* vol. 33, NO.3, March 1998 pp. 417-426.

[3] A. J. Annema *et al*, "Designing outside rail constraints," in *ISSCC, Dig. Tech. Papers,* Feb. 2004, pp.134-135

[4] A. V. Bosch, *et al*, "A 10-bit 1-Gsample/s Nyquist current-steering CMOS D/A converter," IEEE *JSSC*, March 2001, pp. 315-324

[5] V. Gopinathan, *et al*, "Design considerations and implementation of a programmable high-frequency continuous-time filter and variable-gain amplifier in submicrometer CMOS," IEEE *JSSC*, Dec. 1999, pp. 1698-1707.

[6] R. Taft, *et al*, "A 1.8V 1.6GS/s 8b self-calibrating folding ADC with 7.26 ENOB at Nyquist frequency," in *ISSCC, Dig. Tech. Papers,* Feb. 2004, pp.252-253 and 526.