Teranetics

10GBase-T PHY proposal

Jose Tellado, Dariush Dabiri
jtellado@teranetics.com

Teranetics

IEEE 802.3an, May 2004

Teranetics

Overview

- Main parameters of PHY proposal
- Performance
- Transmitter assumptions
- Receiver assumptions

Teranetics

Main parameters of PHY proposal

- FEC code: LDPC(845,1024)
- Modulation: 12PAM.
- Symbol rate: 810MHz
- Equalization: Tomlinson-Harashima precoding (THP)
- Framing and control

Teranetics

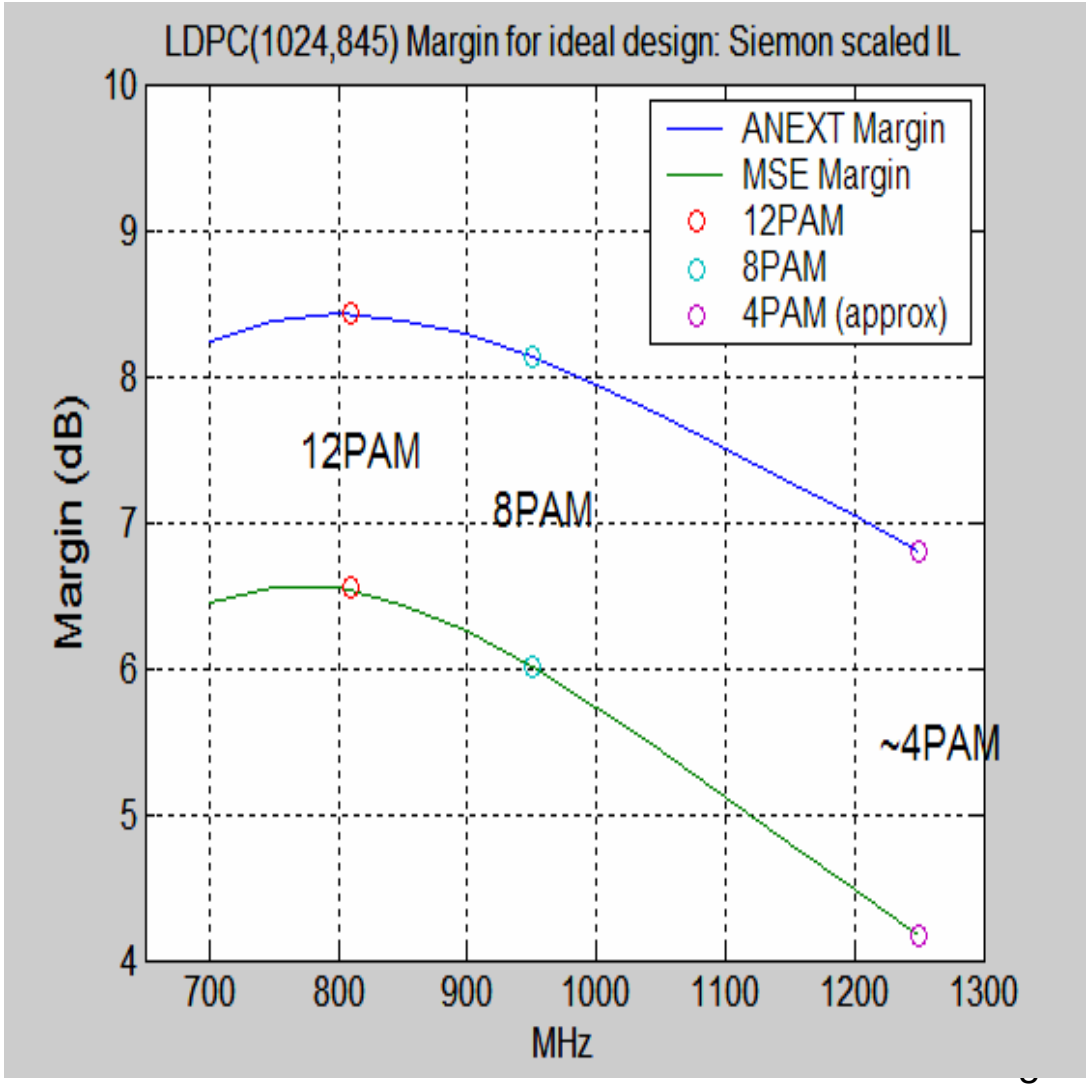
LDPC FEC

- FEC code: LDPC(845,1024)
  - High coding gain: ~8dB
    - Required for 10G objectives w/ enough margin
    - 12dB set partition, 2 coded+1.5 uncoded bit per 1D
    - 3.15bit/PAM symbol
  - Low intrinsic latency: ~160ns
  - Detailed LDPC to 12PAM mappings described in Teranetics March'04 presentation: http://www.ieee802.org/3/an/public/mar04/dabiri_1_0304.pdf

Teranetics

12PAM at 810MHz

- Largest Margin close to 800MHz
- Assumptions:
  - Siemon Matrix data scaled to Model 1 plus WGN=-145dBm/Hz
  - 4dBm Tx Power (2V pk-pk)
  - LDPC 8dB gain
  - Ideal EC, NC, FC, EQ, ADC, DAC,…



Teranetics

12PAM at 810MHz (cont)

- 12PAM at 810MHz has largest margin
  - Multiple presentations confirm largest margin close to 800MHz
  - Broadcom~800MHz, NEC~820MHz, Solarflare~833MHz, KeyEye~833 (uncoded 8PAM)
- 12PAM has lower symbol rate
  - Reduced complexity of analog and digital design
- 12PAM can be combined efficiently with THP
- Allows for Control overhead:
  - MAC control/framing (64/66B)
  - LDPC framing
  - THP coefficient updates, etc.

Equalization

- Equalization:
  - Transmitter: Tomlinson-Harashima precoding (THP)
  - Receiver: FeedForward (MMSE) equalizer
- Enables larger margin FEC
- Details in Multi-vendor Agreement on THP proposal
  - http://www.ieee802.org/3/an/public/may04/powell_1_0504.pdf

Teranetics

Framing and control

- Based on 64B/66B code (see clause 49)
  - 64B/66B supports data and XGMII control characters
  - 64B/66B code aligned with LDPC frame to eliminate one sync bit
- LDPC codeword: 1792bits = 128 4D symbols
- LDPC bit-frame: 397*64/66B blocks + 3 pad bits
- LDPC symbol-frame: 16 codewords + sync word of 6 4D symbols
- Use pad bits to update THP (if necessary)
  - Can exchange 32 coefficients with 16bits in <1ms

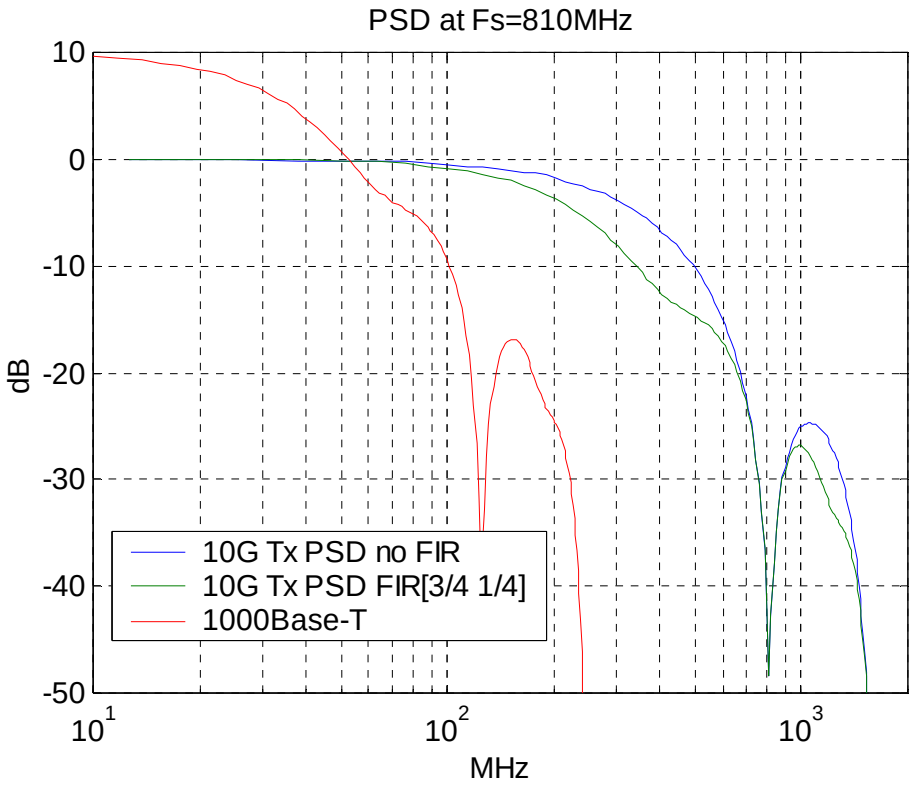
Teranetics

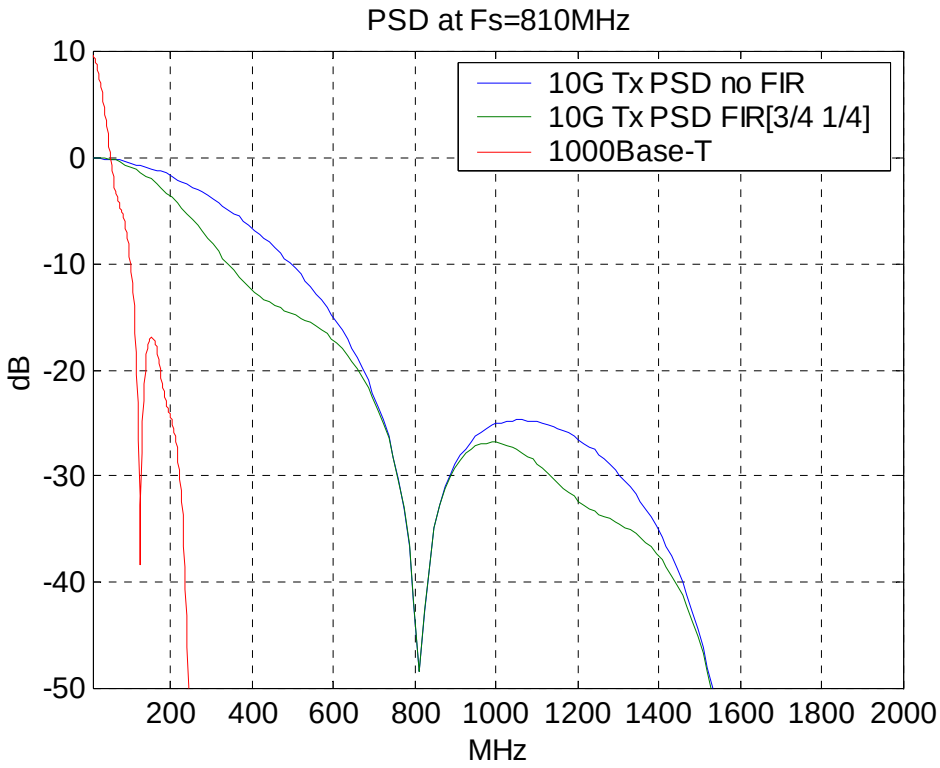
Performance

- 12PAM LDPC requires 24dB input SNR
- Link Margin
  - Model 1: 6.1dB
  - Model 2: 5.3dB
  - Model 3: 6.2dB
  - Model 4: 120m with 3dB ANEXT margin
- Intrinsic latency: 160ns (plus ~500ns of cable)

Teranetics

Performance (cont.)





- Transmit PSD:
  - Plotted above in linear and log frequency scale

Teranetics

Transmitter assumptions

- Modulation: 12PAM
- FEC code: LDPC(845,1024)
- Symbol rate: 810MHz
- Transmitter equalization: THP, 20-32 coefs
- DAC resolution: 10bits
- DAC speed: 810MHz
- Analog transmit filter: One pole LPF at 400MHz
- Max transmit launch voltage: 2volt pk-pk

Teranetics

Receiver assumptions

- Echo suppression: 60dB
- NEXT suppression: 40dB
- FEXT suppression: 20dB
  - FeedForward FEXT Matrix canceller with 50 coefs
  - Matrix FEXT data from Siemon scaled to PSELFEXT limit
- Equalization approach and parameters:
  - FeedForward (MMSE) equalizer with 50 coefs
- ADC speed: 810MHz
- ADC resolution: 9bits
- PAR at input to ADC: 14dB
- Echo cancellation prior to ADC: 15dB
- Additive Gaussian noise at receiver: -150dBm/Hz

Teranetics

PHY Proposal Summary

- Achieves 5-6dB of margin
  - Required to meet 10G objectives with sufficient margin
- Low Intrinsic latency of ~160ns
- Very similar parameters to other PHY proposals (THP, LDPC, Symbol rate ~800MHz)