Update on the LDPC 4D-PAM8 Proposal

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Agenda

- Recap of the LDPC 4D-PAM8 proposal.
- Other LDPC codes based on the Djurdjevic construction.
- Latency vs. Coding gain
- Next Steps

Recap

Four main ingredients of the LDPC 4D-PAM8 proposal:

- 1 Gs/s 8-Level Pulse Amplitude Modulation (PAM) signaling.
- 12dB Coset Partitioning.
- Tomlinson-Harashima pre-coding.
  - supported by multiple PHY vendors*
- (2048, 1723) RS-LDPC block encoding.

* Scott Powell, et. al., "Multi-Vendor Agreement on Precoder Proposal," IEEE P802.3an Interim, May 2004.

Improvement requested in March plenary

The (2048,1723) LDPC code uses 256-symbol block encoding

- Intrinsic latency of the receiver is > 256ns.
- Even with unlimited silicon resources, intrinsic Tx+Rx latency will be ~0.5us.
  - Will be ~1us for current practical implementations.
- System vendors would like to see lower latency solutions*

* Shimon Muller, "Latency Considerations for 10GBASE-T PHYs," IEEE P802.3an Plenary, Mar 2004, muller_1_0304.pdf

Lower Latency LDPC codes

The Djurdjevic construction allows for a plethora of LDPC codes of varying block lengths and code rates*

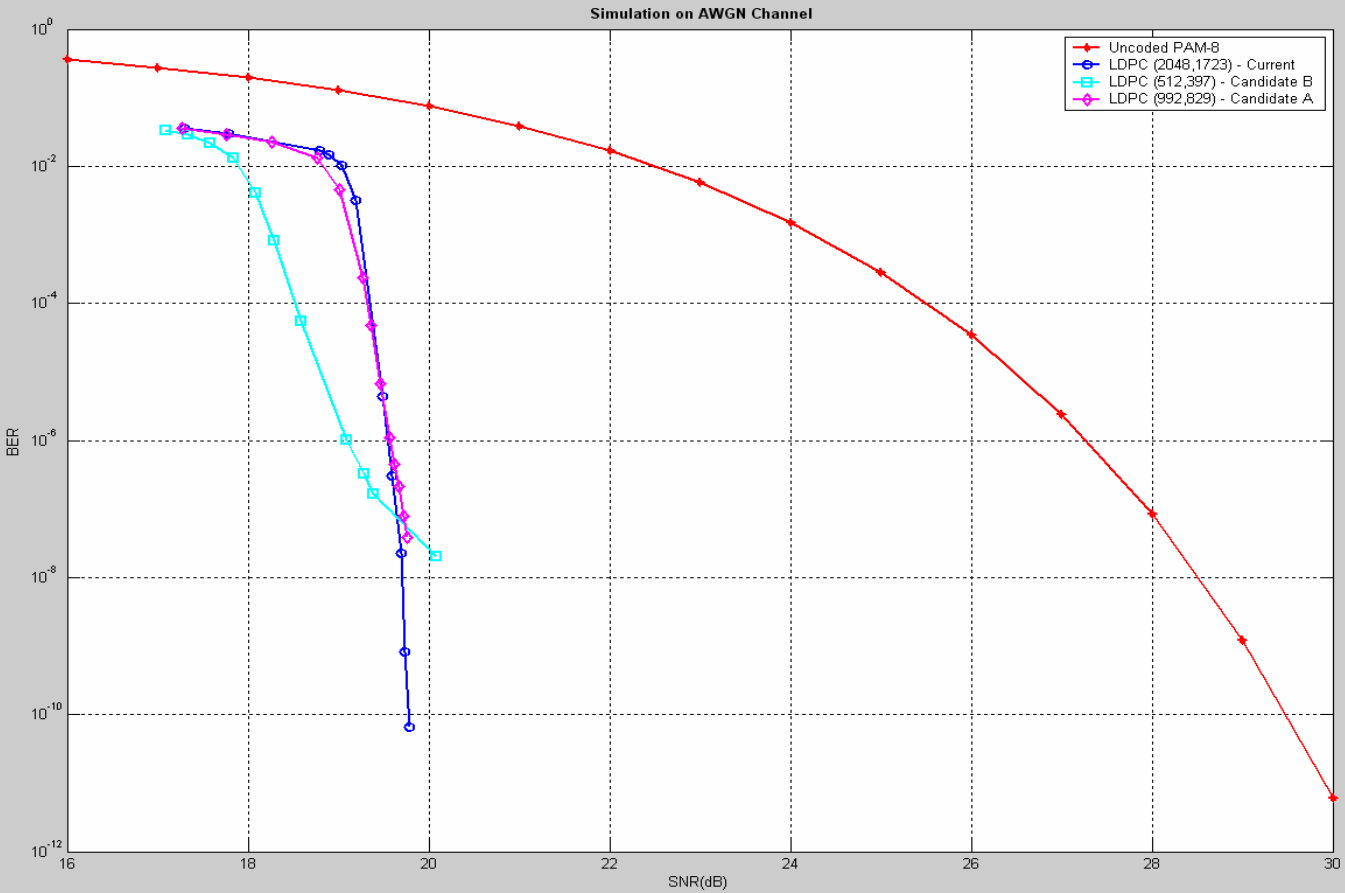
- Restrict codes to block lengths that are a power of 2
  - ~1024 block code and ~512 block code.
- Select code rate sufficient to allow for PCS Encoding of 10GBASE-T
  - ~0.8 is needed

* I. Djurdjevic, et. al., "A Class of Low Density Parity Check Codes Constructed Based on Reed-Solomon Codes with Two Information Symbols," IEEE Communications Letters, Vol. 7, No. 7, July 2003, pp. 317-319

Studied LDPC Codes

Properties/Code	Current	Candidate A	Candidate B
Block Length	2048	992	512
# Information Bits	1723	829	397
Min. Distance	>= 8	>= 8	>= 6
Intrinsic Tx+Rx Latency	~0.5us	~0.25us	~0.13us
Code Rate	0.84	0.84	0.78

Performance of the LDPC Codes



Observations

Candidate A: (992, 829) RS-LDPC Code:

- Performs almost as well as the original (2048, 1723) RS-LDPC Code.
- Need longer simulations to establish performance at 1E-12 error rate.

Candidate B: (512-397) RS-LDPC Code:

- Has an error floor at an unacceptable error rate.
- Is not a strong candidate for the 10GBASE-T application.

Next Steps

- Simulate the (992,829) LDPC block code longer to establish performance at a 1E-12 Bit Error Rate or better.
  - The (2048, 1723) LDPC block code would be a fallback in case of unexpected problems with the (992,829) LDPC simulations.
- Fill in the spreadsheet entries using the specific channel models determined by the task force.
  - Establishes the cogency of the LDPC 4D-PAM8 proposal in all respects.