

# IEEE P802.3at Task Force Power Via MDI Enhancements

## ALT A Midspan requirements - updating the spec

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# Objectives

- Updating the specification to integrate all latest changes in OCL requirements and ALT A 100BT Midspan.



# Background -1

- The current spec requires that:

33.4.8

Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1  $I_{unb}$  (see Table 33–11).

- Rational

Reducing  $I_{unb}$  to Type 1 levels increase PD Type 2 OCL to 350uH minimum i.e make the system as 350uH system.



## Background -2

- Prior to changing OCL from 350uH to 120uH we define a Transfer Function (Eq 33-19 in 33.4.9.2) that 100BT ALT A Midspans has to meet.
- This equation was built for 350uH system.
- It was approved and supported by a motion by David Law and Yair Darshan.
- See motion in: [http://www.ieee802.org/3/at/public/2008/05/minutes\\_0508.pdf](http://www.ieee802.org/3/at/public/2008/05/minutes_0508.pdf)
- See technical data attached to the motion in : <http://www.ieee802.org/3/at/public/2008/05/index.html>



# Background -3

- Both requirements 33.4.8 and 33.4.9.2 are equivalent alternatives i.e. both of them supporting 350uH system.
- As a result 33.4.8 can be updated as follows:  
"Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1  $I_{unb}$  (see Table 33–11) **or meet 33.4.9.2.**"

The rest is implementation that we don't care.



# Discussion



# References

- For complete analysis, model building, model validation techniques and lab test results see:

[http://www.ieee802.org/3/at/public/2008/05/darshan\\_2\\_0508.pdf](http://www.ieee802.org/3/at/public/2008/05/darshan_2_0508.pdf)



Short Summary of Previous Midspan ad hoc work when  $OCL=350\mu H$   
in the System Channel Model.

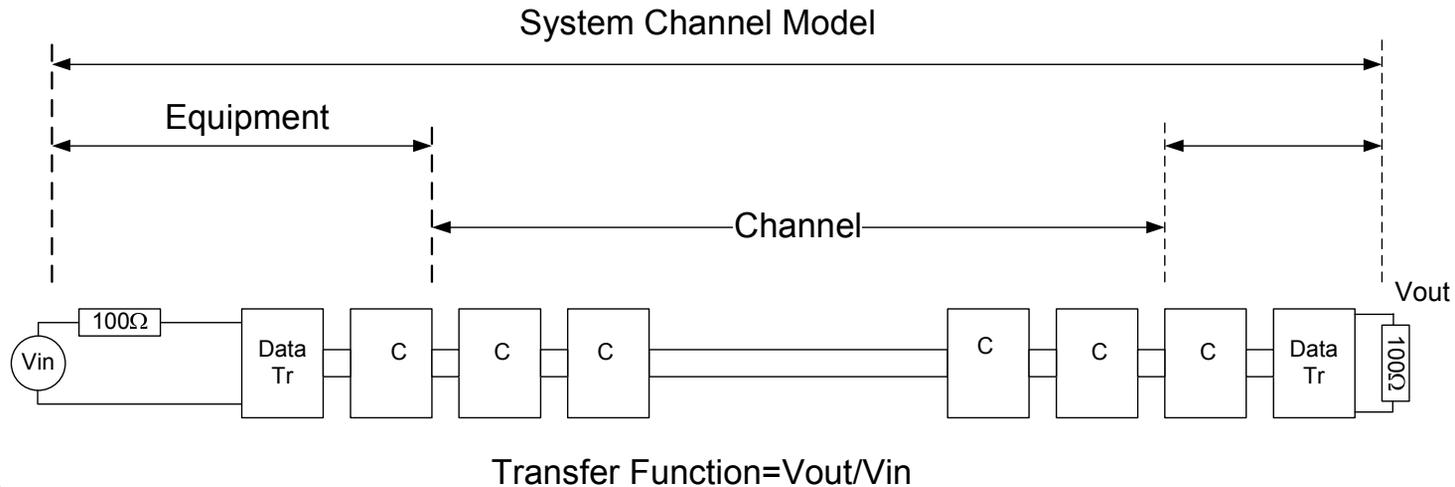
See complete work at:

[http://www.ieee802.org/3/at/public/2008/05/darshan\\_2\\_0508.pdf](http://www.ieee802.org/3/at/public/2008/05/darshan_2_0508.pdf)



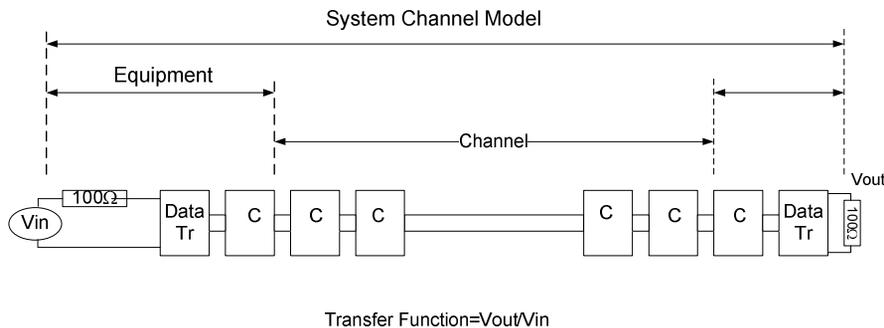
# Terms and abbreviations

- **Channel Model =CM** : Cable + 4 Connectors forming 25 Ohms at 100m round loop on data pairs
- **System Channel Model = SCM**: Channel + 2xData 100BT Transformer connected to signal source with 100 ohm series impedance and loaded with 100 ohm termination
- **Transfer Function =TF**: The ratio between the voltage at the load termination to the signal source as function of frequency. The TF includes the effect of the source and load impedance for simulating the droop effect as function of the inductance of the data transformers
- **Low Frequency Model=LFM**: The System Channel Model used for derivation of the Transfer Function is limited to frequencies <1MHz
- **LM, Magnetizing Inductance**: Data transformer inductance
- **Idc**=The total dc bias current that the transformer is exposed too as a results of the data and the channel imbalance during PSE operation.

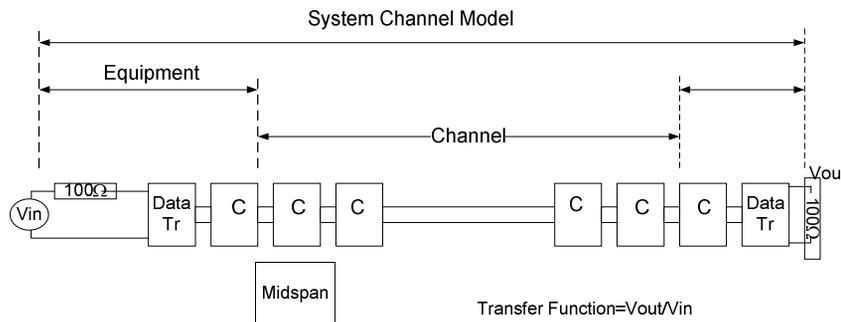


# Objectives

- (1) To define the requirements for a **System Channel Model** at the signal path for 100BT operation at frequencies below 1MHz



- (2) To define the requirements for a Midspan at the signal path for 100BT operation at frequencies below 1MHz as a result of (1)

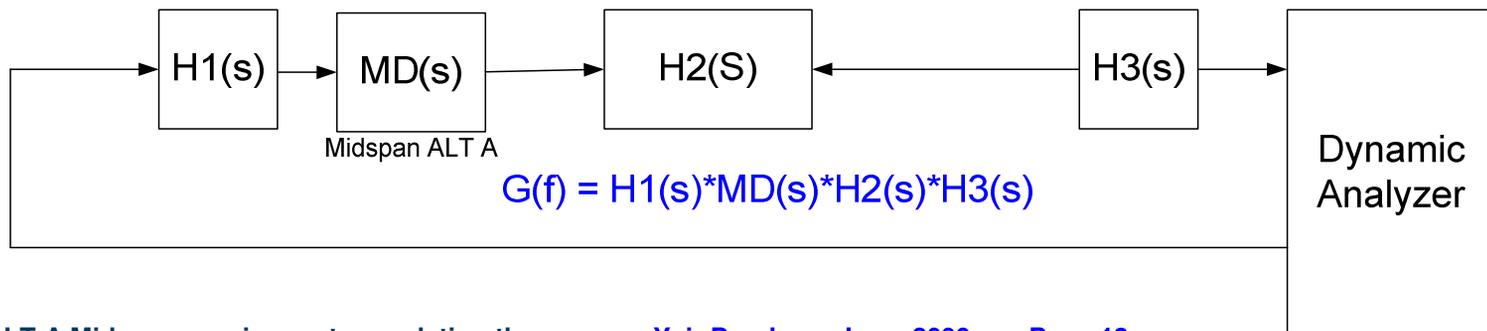
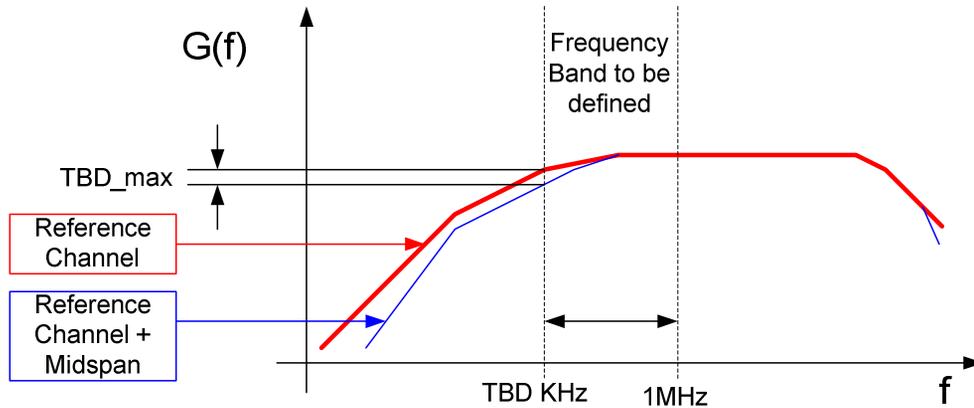
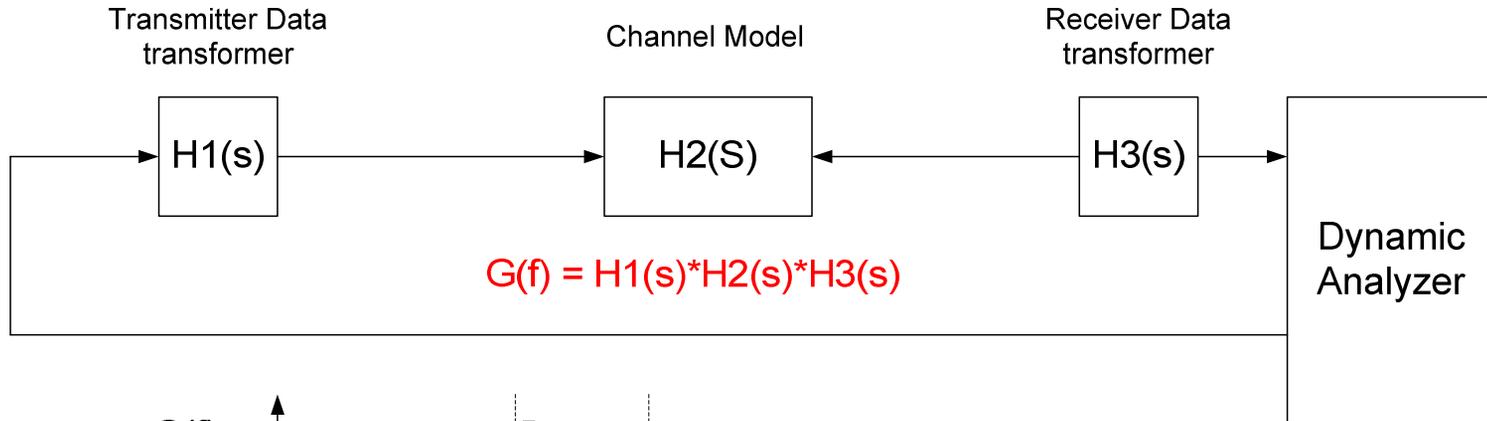


# Background

- The IEEE802.3at task force approve using ALT A Midspan.
  - Powering the PD through the signal path
- The IEEE802.3 requires that when a Midspan is inserted in the channel it shall not alter the channel performance.
  - The channel performance is defined from 1MHz and up by 33.4.8
  - The 802.3 doesn't not define requirements for the channel below 1MHz.
- In addition, there is the inductance requirements as specified in ANSI X3.263-1995 (TP-PMD) subclause 9.1.7 which may be affected when a ALT A Midspan is used in the channel for 100BT
- As a result, the droop of the signal may increased which may affect the BER
  - In addition, the effect of BLW on the BER may increase as well
- All of the above may further affected by the presence of DC bias due to the cabling imbalance



# Proposed Solution

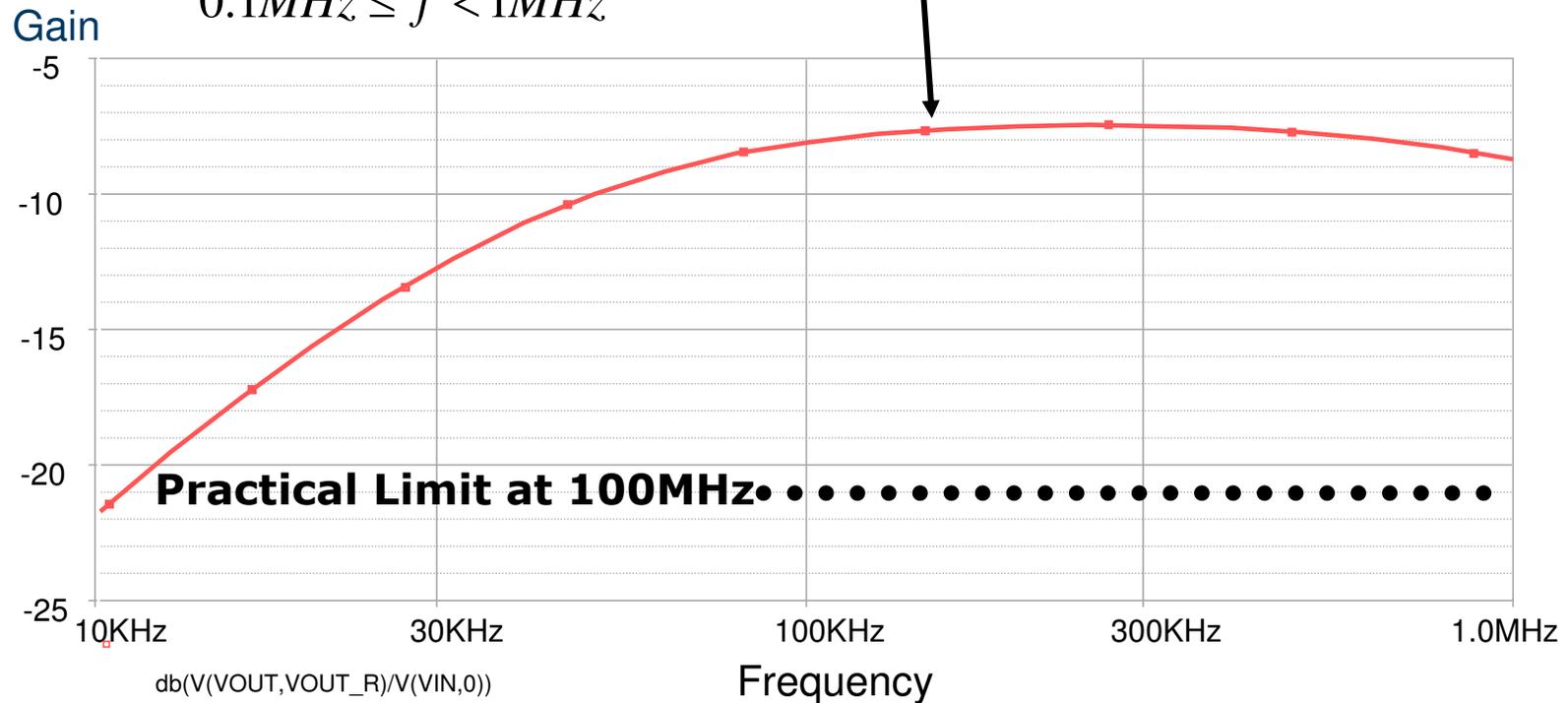


# SCM: without Midspan at 350uH, 100m. W.C analysis

- A compliant System Channel Model Gain w/o Midspan, must be higher than this curve per current standards and standard components specifications

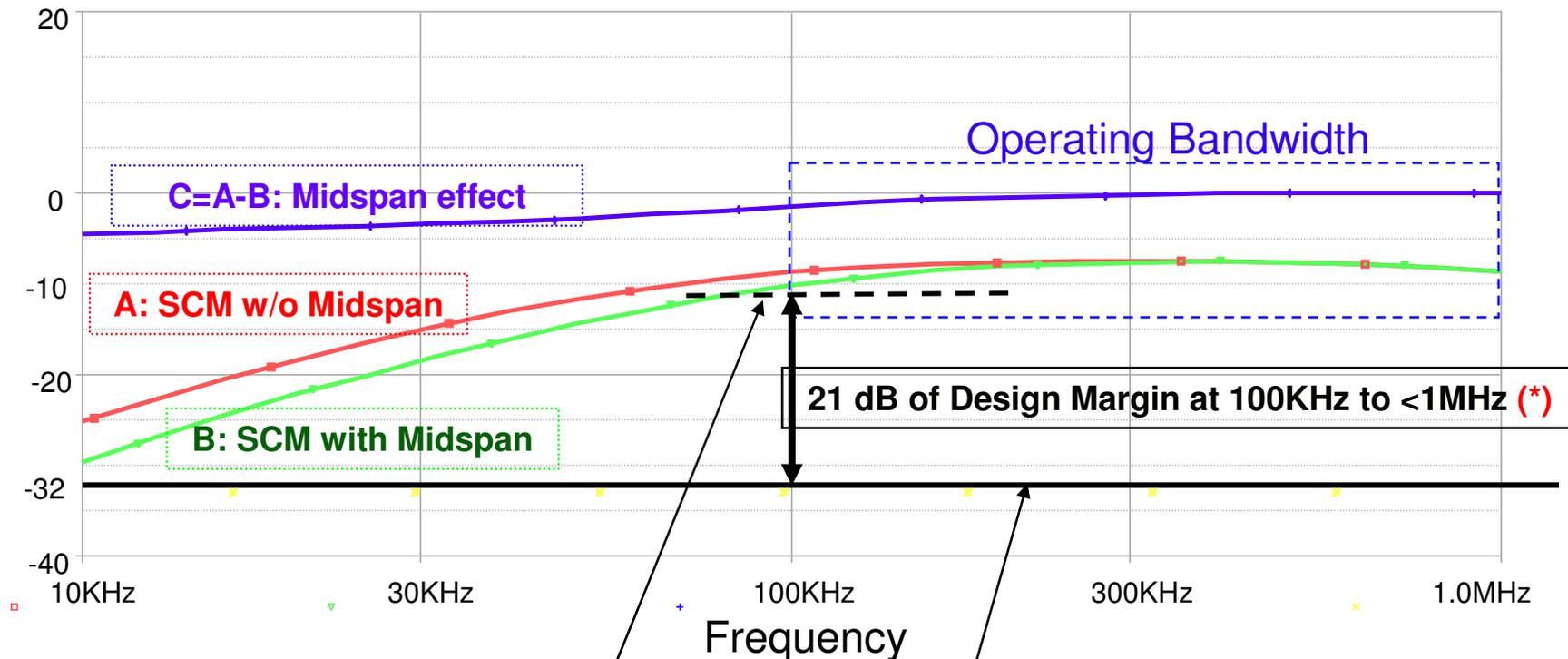
$$\text{Gain} = -9.075 + 14.419 \cdot f - 41.781 \cdot f^2 + 45.759 \cdot f^3 - 18.075 \cdot f^4$$

$$0.1\text{MHz} \leq f < 1\text{MHz}$$



# SCM: with and without Midspan at 350uH, 100m. W.C analysis

Gain[dB]



**E: D at 1MHz. Gain/ Attenuation/ Insertion Loss = -11dB**

**D: SCM PHY to PHY minimum Gain/ Attenuation/ Insertion Loss requirements at 100MHz= -32dB**

(\*) Actually margin is higher by additional 3dB due to the fact that Channel IL is ~1dB at f<1MHz and not 4dB



# How to distribute the design margins that we have in the system at frequencies below 1MHz?

- At 100KHz, the system gain is:
  - ~-8dB w/o Midspan (-8.7dB at 1MHz, -7.5dB at 300KHz)
  - ~ -9dB with Midspan (-8.7dB at 1MHz, -7.5dB at 300KHz)
  - Which is practically negligible difference.
- The SCM is required by various system components specifications to work with gain as low as
  - -32dB at 100MHz
  - -11dB at 1MHz
  - Hence the PHY is capable to work with System Channel Gain as low as -32dB
  - However the inductance issue is relevant at the low frequency range which is 21dB higher than the worst case conditions.
- Since the Midspan has negligible effect on the SCM it is recommended to assign most of the Margin to the Switch according to the following ratio:
  - Midspan: 1dB max. as function of frequency from 100KHz to 1MHz
  - Switch: 20dB min. as function of frequency from 100KHz to 1MHz



# Generating Midspan TF

- Steps:
- 1. Generating System Model w/o Midspan, **SCM**.
- 2. Generating System Model with Midspan ALT A, **SCMM**.
- 3. Finding w.c analysis results and update the model. .
- 4. Finding Midspan TF=SCM -SCMM (Gain[db] vs Frequency plot). Note that TF is not SCM/SCMM (as the conventional definition) due to the fact that we are looking for worst case template that allows at least 20dB margin to the Switch i.e. we are defining the worst case effect of the Midspan on the SCM gain.
- 5. Finding the best regression function structure to build the TF. *(3, 4 and 5 order polynomial regression vs. Logarithmic regression were evaluated.)*
- 6. Logarithmic structure showed best accuracy for the operating bandwidth under discussion (100KHz to 1MHz) for Midspan.
- 7. Adding margin function to cover Test Equipment errors and design.
- 8. Getting Final Equation.



# Midspan TF and test setup for compliance.

Including w.c analysis, Test Equipment Error and design Margin

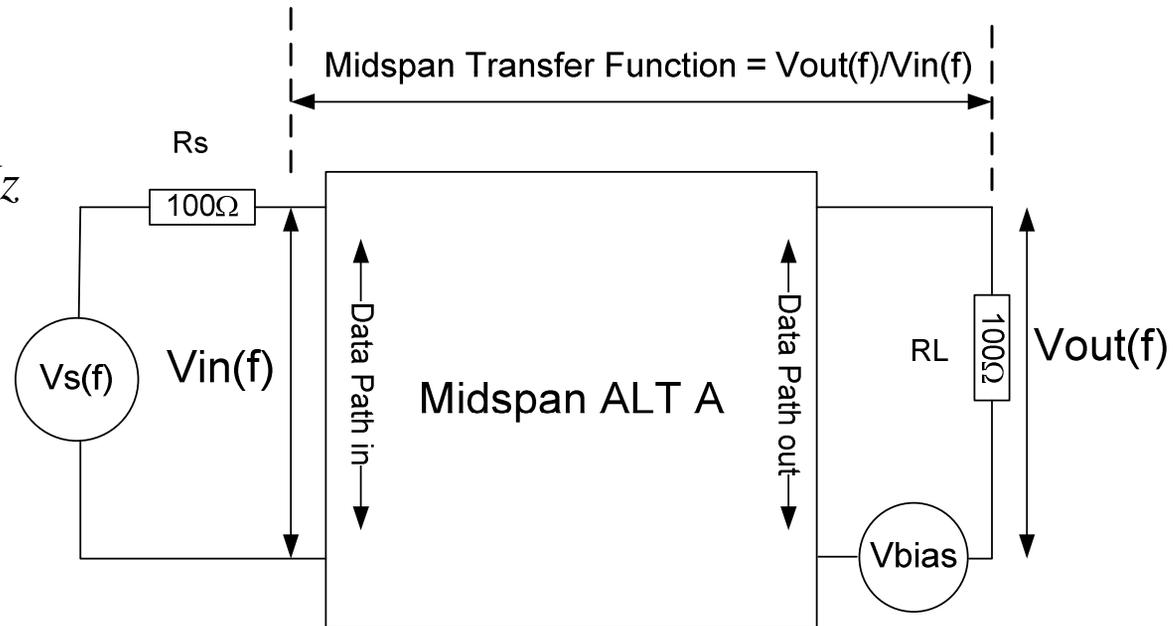
$$\left\{ -c + 37.5 \cdot \text{LOG}_{10} \left( \frac{a \cdot f}{\sqrt{1 + b \cdot f^2}} \right) \right\}$$

$$a = 22.40$$

$$b = 520.5$$

$$c = 0.1000$$

$$0.1\text{MHz} \leq f < 1\text{MHz}$$



- $V_{in}(f)$  is the Sine wave signal to be used to measure the Midspan TF.
- $V_{bias}$  is the DC offset voltage to be applied in series to  $R_L$  in order to generate  $I_{bias}$ .
- $V_{out}(f)$  is the Midspan response to  $V_{in}(f)$

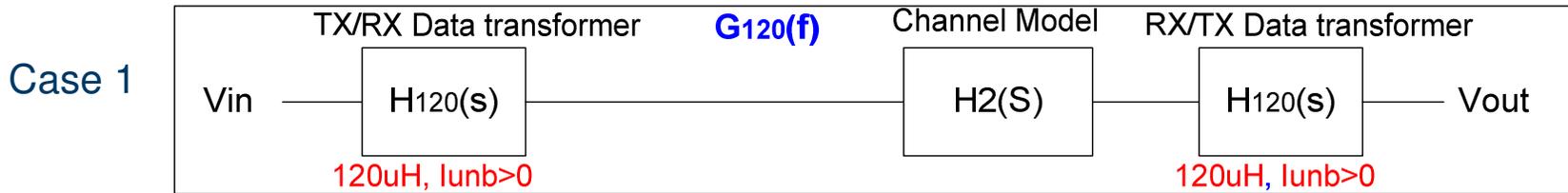


Material from Jan 2009 meeting regarding the difference in system dynamics when channel contain Midspan and as a result only the PD has 120uH OCL.

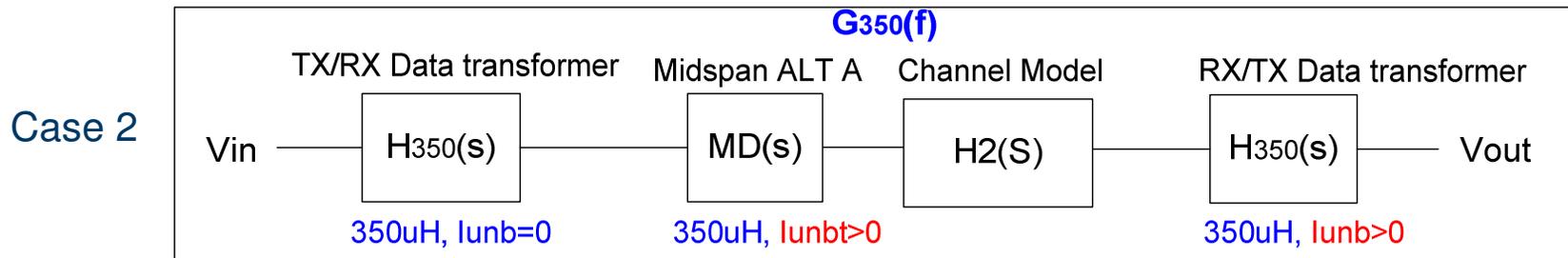


# Type 2 100BT ALT A Midspan System 350uH vs 120uH system comparison

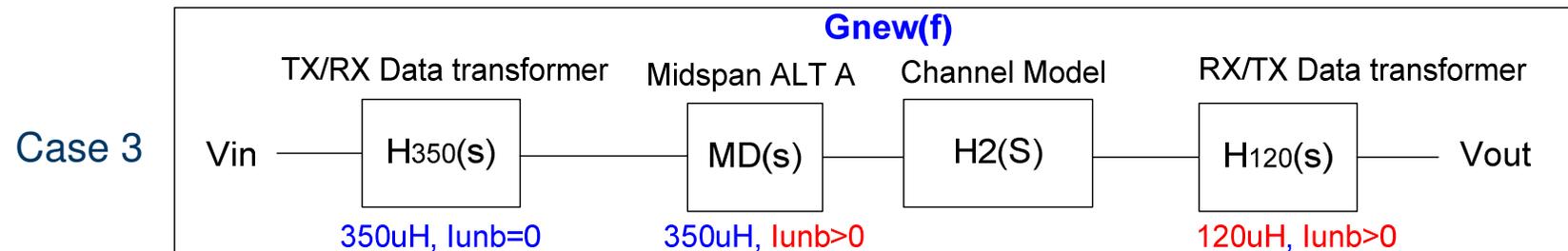
The system performance represented by  $G_{120}(f) = H_{120}(s) * H_2(s) * H_{120}(s)$  approved by Draft D3.3



The system performance represented by  $G_{350}(f) = H_{350}(s) * MD(s) * H_2(s) * H_{350}(s)$  approved by Draft D3.3 as well (Eq-33-19)



What is the difference in system performance between  $G_{new}(f) = H_{350}(s) * MD(s) * H_2(s) * H_{120}(s)$  and  $G_{120}(f)$  which is actually Eq 33-19 when  $OCL = 120\mu H$  only at the PD side?

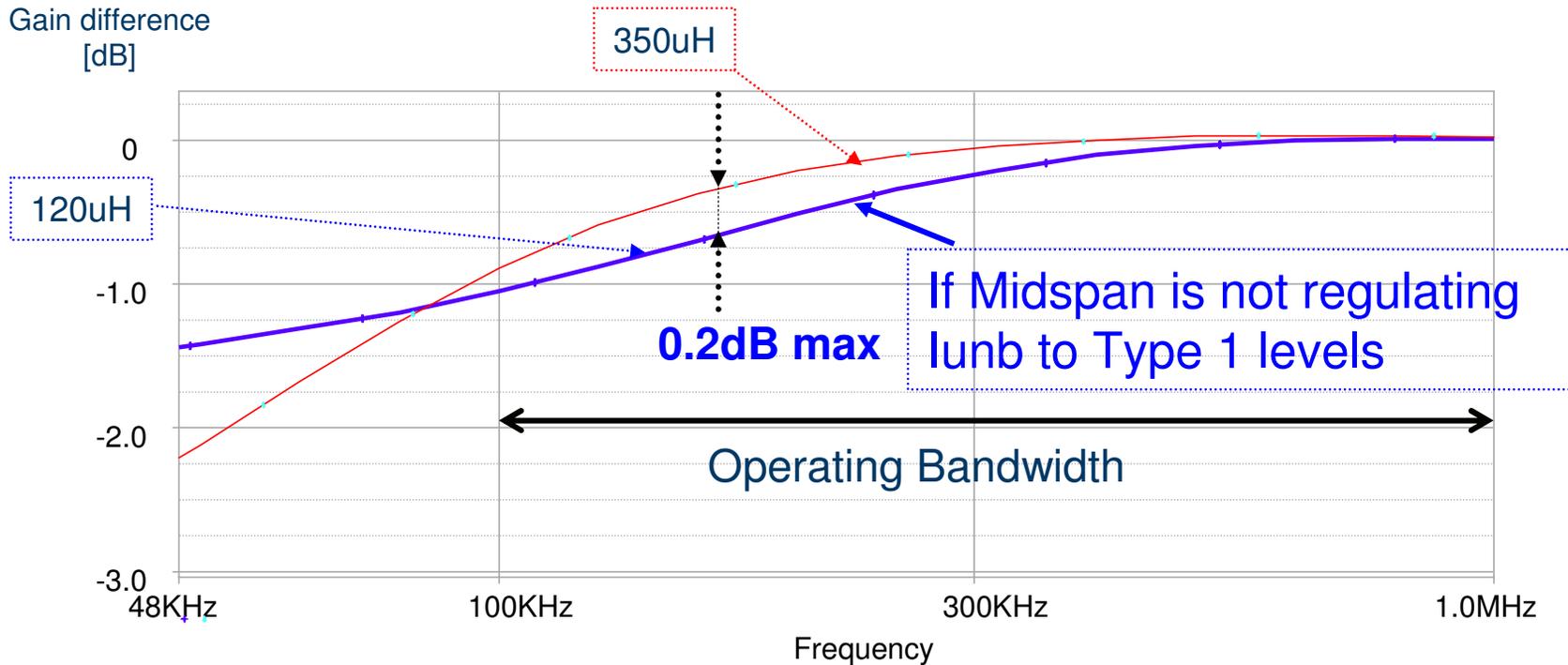


## OCL value vs Midspan Presence

- Case 1: No Midspan.  $I_{unb}=3\%I_{peak}$ . OCL=120uH in Switch and PD.
- Case 2: Midspan is inserted and all OCLs are 350uH for worst case  $I_{bias}$
- Case 3: Midspan is inserted and is not regulating  $I_{unb}$  to Type 1 levels:
  - Switch side is without PoE current hence its OCL is 350uH min hence will not affect Eq-33-19.
  - PD side works with  $3\%I_{peak}$  hence PD OCL may be 120uH minimum and will affect Equation 33-19. The question is if the effect is negligible or important?



# Eq 33-19 worst case gain difference between PD OCL= 120uH vs 350uH Midspan TF comparison: Simulation Verification

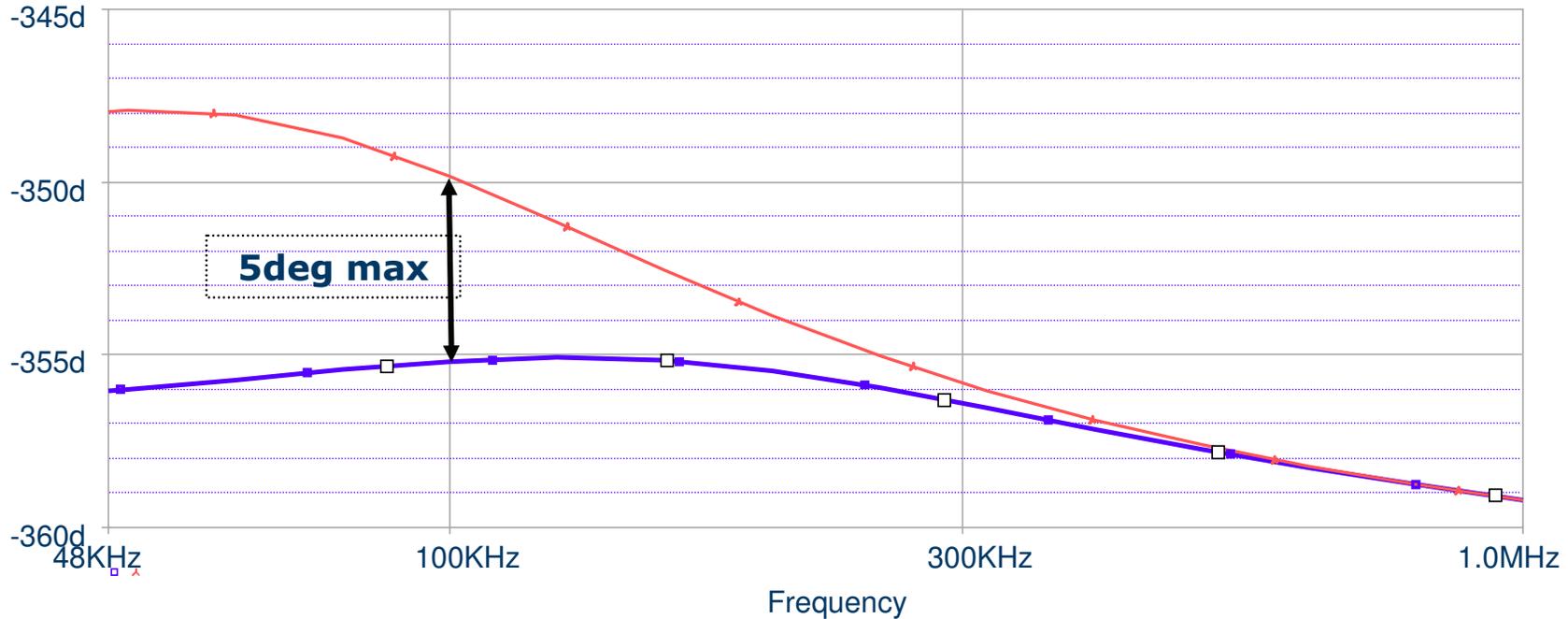


$$-db(V(VOUT,VOUT\_R)/V(VIN,0)) + db(V(VOUT\_2,VOUT2\_R)/V(VIN,0))$$

The worst case difference is 0.2dB and varies with frequency



# Eq 33-19 worst case phase difference between PD OCL= 120uH vs 350uH Midspan TF comparison: Simulation Verification



$$P(V(VOUT\_2,VOUT2\_R)/V(VIN,0))-P(V(VOUT,VOUT\_R)/V(VIN,0))$$

5deg max /270deg potential =1.75% max i.e. Dynamics are kept w/o significant change.



# Summary

- Eq 33-19 is not affected due to the requirement that Midspan need to regulate  $I_{n(b)}$  to Type 1 levels hence OCL in PD and Switch stays as in Type 1 systems i.e. 350uH minimum.
- At the worst case that Midspan is not regulating  $I_{n(b)}$ , it will change Eq 33-19 by 0.2dB max / 5deg (1.75%) as function frequency over the operating frequency range due to the 120uH minimum at the PD.
- Recommendations for Draft D3.3
  - When ALT A Type 2 Midspan is regulating  $I_{n(b)}$  to Type 1 levels, Eq 33-19 is not changed since it is a 350uH approved system.
  - When ALT A Type 2 Midspan is not regulating  $I_{n(b)}$  to Type 1 levels, Eq 33-19 need to be met as alternative.

(Rational: Eq 33-19 still covers the difference of OCL=120uH in the PD only.)



## Recommendation for modifying the existing text:

Change from:

"Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 I<sub>unb</sub> (see Table 33–11).

To:

"Alternative A Type 2 Midspan PSEs that support 100BASE-TX shall enforce channel unbalance currents less than or equal to Type 1 I<sub>unb</sub> (see Table 33–11) **or meet 33.4.9.2.**

